

TM 11-5840-219-35

DEPARTMENT OF THE ARMY TECHNICAL MANUAL

FIELD AND DEPOT MAINTENANCE

COORDINATE DATA SET AN/TSQ-36



HEADQUARTERS, DEPARTMENT OF THE ARMY
APRIL 1959

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working on any units of the equipment, the 115-volt ac line connections, and the reference voltage line connections.

EXTREMELY DANGEROUS VOLTAGES

EXIST IN THE FOLLOWING UNITS:

Power Supply PP-2236/G----- ± 300 -volt circuits.

Coordinate Data Encoder KY- ± 300 -volt circuits.
278/TSQ-36.

Coordinate Data Decoder KY- ± 300 -volt circuits.
277/TSQ-36.

DON'T TAKE CHANCES

COORDINATE DATA SET AN/TSQ-36

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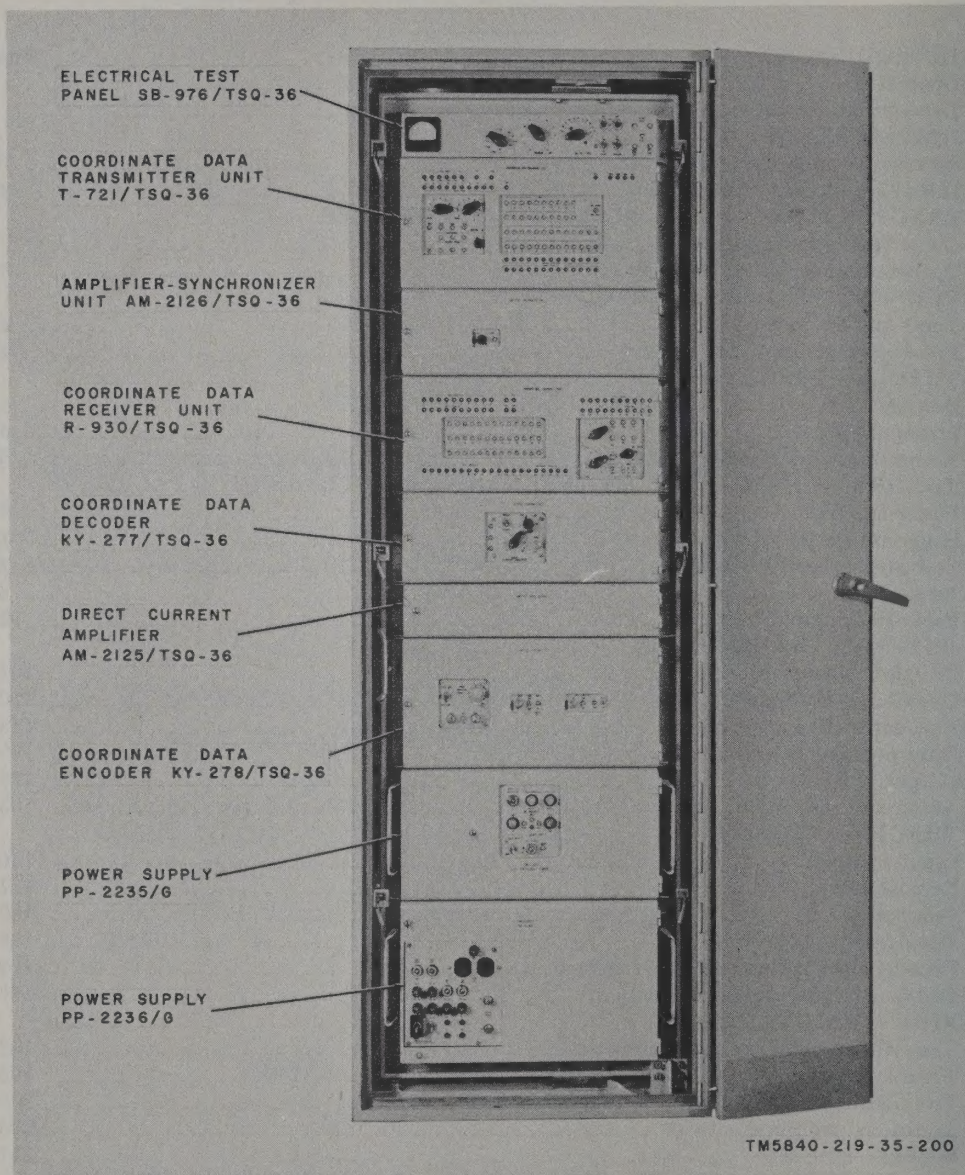


Figure 1. Coordinate data set AN/TSQ-36.

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1. Scope

a. This manual contains instructions for installation requirements, preoperational and starting procedures, theory, maintenance, and repair of Coordinate Data Set AN/TSQ-36 (fig. 1). In addition, there are five appendixes which should be reviewed before reading the theory chapters. Appendix I contains a discussion of binary arithmetic as it applies to this equipment; appendix II describes the basic control elements of the equipment; appendix III contains a discussion of the operation of transistors and their applications as related to their use in the equipment; appendix IV presents sample problems in solving for parallax quantities; and appendix V gives a method for determining correction for distortion due to the earth's curvature. Also appearing at the end of this manual is a glossary: section I contains abbreviations of terms peculiar to this equipment, and section II contains definitions of unusual terms.

b. Coordinate Data Set AN/TSQ-36 has various applications in Air Defense System AN/MSQ-18. Details regarding the applications of the equipment in the AN/MSQ-18 system are covered in the AN/MSQ-18 literature (to be published as TM 11-5820-313-10; TM 11-5820-313-35; TM 11-5820-315-35; and TM 11-5820-318-35). The AN/MSQ-18 literature refer-

ences applicable portions of this manual for specific information regarding theory, and maintenance of the AN/TSQ-36.

c. Forward comments on this publication directly to: Commanding Officer, United States Army Signal Publications Agency, Fort Monmouth, N. J.

2. Forms and Records

The following forms will be used for reporting unsatisfactory conditions of Army materiel and equipment and in performing preventive maintenance:

a. Unsatisfactory Equipment Report. Fill out and forward DA Form 468 (Unsatisfactory Equipment Report), to Commanding Officer, U. S. Army Signal Equipment Support Agency, Fort Monmouth, N.J.

b. Damaged or Improper Shipment. Fill out and forward DD Form 6 (Report of Damaged or Improper Shipment), as prescribed in AR 700-58.

c. Preventive Maintenance. Department of the Army Form 11-238 Maintenance Check List for Signal Corps Equipment (Sound Equipment, Radio, Direction Finding, Radar, Carrier, Radiosonde, and Television) will be prepared in accordance with instructions on the front of the form (fig. 19(1)).

Section II. DESCRIPTION AND DATA

3. Purpose and Use

a. In the usual application of the data set, the primary purpose is to receive radar-originated analog data which defines the position of an aerial target on three coordinates, and to reproduce this data at a point up to several hundred

miles distant without appreciable loss in accuracy.

b. Through the use of this equipment and equipment associated with it, data from several radar stations, outlying from a central control point, may be exchanged continuously. This en-

ables efficiently coordinated action within a large defense area.

4. Features of Operation

a. The data set sequentially monitors three analog voltages from a single source by sampling the changing coordinates at a repetition rate of up to about 15 times per second.

b. The information fed to the transmitter from a local data source usually represents the source position with respect to the local radar. Since it may be desirable to refer this data to a point common to both the transmitter and receiver, the data set has means of adding parallax and earth curvature corrections at both ends of the circuit, and provisions for converting ground range coordinates to slant range coordinates through associated equipment. In addition to the coordinate data, the system transmits auxiliary information which can be represented by ON-OFF signals or by binary numbers.

c. The data set is able to operate over ordinary wire communication circuits which need not be phase or amplitude equalized, or especially engineered in any manner. Most military and commercial circuits, both voice frequency and carrier, are suitable.

d. Standard voltages are used as a reference from which are derived the dc analog coordinate positional voltages and the encoding and decoding voltages. Reference voltages used in the data set are taken from the same source as that used in equipment associated with the data set. Since the same reference voltages are used throughout the system locally, no translation errors result from slight changes in the reference voltages.

e. The data set accepts dc analog voltages at the transmitting location and reproduces these voltages at a distant point with an accuracy of 1 part in 1,024. Initially, each of these voltages lies within the range of either ± 50 volts or ± 100 volts, and represents one positional coordinate of an aerial target in space. Each input voltage is encoded into a specific binary number which is proportional to the voltage. A given binary number represents the corresponding input voltage level which most closely approximates it out of 1,024 levels. Ten binary digits are required to distinguish 1,024 separate levels. These digits form a binary "word" consisting of ONE's and ZERO's. Each digit in the word is allotted a

specific time slot in the transmitted message. A ONE is represented by a spurt of carrier tone one time slot in duration, and a ZERO is represented by the absence of carrier for one time slot. Each time slot is 1.33 milliseconds long. The digit rate is, therefore, $1 \div 1.33 \times 10^{-3}$ or 750 digits per second. Two complete cycles of 1,500-cps carrier thus are transmitted for each ONE in the binary word.

f. Figure 2 illustrates a typical message as it appears on the transmission line. The message consists of a synchronizing word (ready interval), which is a group of special signals used for synchronizing the receiver, followed by the message proper, which is a series of binary digits. The synchronizing word consists of six time slots of 1,500-cycle tone followed by a blank time slot (sync guard interval) and a single time slot (sync interval) of 1,500-cycle tone. To distinguish this pattern from ordinary data signals, a 600-cycle tone lasting for three time slots is transmitted simultaneously with the 1,500-cycle tone at the start of the synchronizing pattern (or word). This dual frequency tone is known as the ready signal, and the single digit of 1,500-cycle tone is known as the sync digit.

Figure 2. Typical cycle of transmitted message.
(Contained in separate envelope)

g. The message proper consists of five binary words, the first and last of which are auxiliary words. Although the auxiliary digits are transmitted in a group as 10-digit and 2-digit binary words, they may be used singly or in small groups to represent any predetermined information. The other three words represent the positional coordinate data H, X, and Y, respectively. Each of the coordinate data words represents a single assigned number. A 10-digit word is transmitted for the H coordinate. Thirteen-digit words, instead of 10-digit words, are transmitted for the X and Y data to permit the addition of parallax, as explained in paragraph 39b. The complete message is known as a "frame," and requires a transmission time of $77\frac{1}{3}$ milliseconds.

h. The binary words representing coordinate data are detected at the receiver and, by means of the decoder in the receiver, are reconverted to analog voltages. The voltages then are stored temporarily in the output section and are presented on three separate output leads.

i. A generalized block diagram of the data set transmitter is given in figure 3, and one of the receiver is shown in figure 4. These diagrams describe the functions of the various sections of the equipment and their relationship to each other.

j. Parallax corrections are applied to the data in both the transmitter and the receiver to permit interpreting all target positional data with respect to a master reference point. These corrections amount to adding preset binary numbers to each of the three positional coordinates. Groups of toggle switches are provided for pre-setting these corrections. The process of addition then is performed automatically on a digital basis. These parallax settings are constant for a given system installation, and are changed only when the master reference point is redefined or when the equipments are moved to new locations.

k. The X and Y coordinates initially are straight-line vectors. Distortion of these vectors due to the curvature of the earth's surface becomes appreciable when the distance between a transmitter and the master reference point is sufficiently large (in the order of 200 or 300 miles). Under these conditions, an additional modification of the data to be transmitted is required. Paragraph 39d and appendix V show how this earth curvature correction can be approximated by changing the original X and Y voltages by a small percentage, since this correction is a function only of the distance between the transmitter and the master reference point. This correction is made by modifying the parallax correction slightly, and by adjusting a calibrated potentiometer in the encoder. A similar earth curvature correction may be made to the decoder analog voltages in the receiver. The H vector represents the altitude of the target (height above sea level) rather than the Z dimension of a true linear Cartesian coordinate system, and as such, requires no earth curvature correction.

l. The data set receiver reproduces ground range X and Y coordinate data. Ordinarily, this data is diverted to associated equipment where it is converted to slant range coordinates. After conversion to slant range data, it is returned to the receiver and is processed in the same manner as ground range data.

m. In the usual system application, the data set transmitter is started and stopped by signals from

associated equipment. This is known as the remote start mode of operation, and upon receipt of a remote start signal, the transmitter sends a complete frame of data and then stops until a new start signal is received. The data set can also be used in the continuous mode of operation whereby the analog data connected to its input terminals is transmitted as digital data in a continuous succession of frames.

Figure 3. Coordinate data transmitter unit T-721/TSQ-36, functional block diagram.
(Contained in separate envelope)

Figure 4. Coordinate data receiver unit R-930/TSQ-36, functional block diagram.
(Contained in separate envelope)

5. Technical Characteristics

a. General.

Accuracy-----	1 part in 1,024.
Input and output line impedances.	600 ohms.
Transmitter output level.	Variable from maximum down to 10 db below maximum in ½ db steps (maximum is between 0 and +6 dbm*).
Receiver sensitivity:	
CDG/TAC operation.	-20 dbm ± 5 db.
OC operation-----	-4 dbm ± 1 db.
Line frequencies-----	1,500 cycles and 600 cycles.
Pulse rate-----	750 pps.
Input voltages (dc):	
Analog, H, X, Y---	± 50 volts or ± 100 volts.
Transmitter reference.	± 250 volts or ± 300 volts.
Receiver reference.	± 250 volts or ± 300 volts.
Analog output (dc)-----	± 50 volts into a minimum resistance load of 50,000 ohms. Load must be constant.
Ambient operating temperature.	25° to 125° F.

b. Power Requirements.

Voltage-----	105 to 130 volts.
Frequency-----	60-cycle, single-phase.
Power-----	Approximately 620 watts.

6. Physical Characteristics

a. Cabinet.

Height-----	72 inches.
Width-----	23 15/16 inches.
Depth-----	16 1/2 inches.
Door swing-----	11 13/32 inches.
Weight-----	525 pounds (fully equipped).
Connections-----	Access through rear.

* 0 dbm = 1 milliwatt in 600 ohms.

b. Rack.

Type of construction-----	Enclosed frame.
Cross section-----	19-inch T.
Mounting-----	Off-center swivel (for rear access).
Securing method-----	6 clamp fasteners.

c. Panels.

Type-----	Standard 19-inch aluminum.
Covers-----	Hinged-front, protective covers with Dzus fastener. (There is no front cover on the test panel.)
Functional layout-----	Wiring side at front, apparatus side at rear.

d. Ventilation.

Two axial fans at the top of the cabinet for air intake from the trailer air conditioner and one centrifugal blower above the power supplies as a hot spot fan. Exhaust is from the bottom of the cabinet into the trailer air conditioner.

e. Mounting.

Six holes at the bottom of the cabinet and two holes at the upper rear corners for attaching the cabinet to shock mounted pads.

Trailer-----	2 additional shock mounts on rear for attaching to wall.
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7. Common Names

A list of common name assignments for the components of the data set is given in *a* below. The common name of the data set assembly and the listing of the units within this assembly are given in *b* below.

a. Components.

Common name	Nomenclature
Cabinet-----	Electrical Equipment Cabinet CY-2560/TSQ-36.
Test panel-----	Electrical Test Panel SB-976/TSQ-36.
Transmitter unit-----	Coordinate Data Transmitter Unit T-721/TSQ-36.
Amplifier synchronizer-----	Amplifier-Synchronizer Unit AM-2126/TSQ-36.
Receiver unit-----	Coordinate Data Receiver Unit R-930/TSQ-36.
Decoder-----	Coordinate Data Decoder KY-277/TSQ-36.
Automatic zero set-----	Direct Current Amplifier AM-2125/TSQ-36.
Encoder-----	Coordinate Data Encoder KY-278/TSQ-36.
Low voltage power supply-----	Power Supply PP-2235/G.

Common name

Nomenclature

High voltage power supply-----	Power Supply PP-2236/G.
T/R Package-----	Transmitter Unit Subassembly MX-2688/G.
T/S Package-----	Transmitter Unit Subassembly MX-2689/G.
R/T Package-----	Receiver Unit Subassembly MX-2685/G.
R/V Package-----	Receiver Unit Subassembly MX-2686/G.
R/W Package-----	Receiver Unit Subassembly MX-2687/G.
R/LC Package-----	Receiver Unit Subassembly MX-2684/G.
A Package-----	Gated Flip-Flop TD-210A/G.
C Package-----	Pulse Generator SG-257A/G.
D Package-----	Gated Flip-Flop TD-211A/G.
B Package-----	Gated Flip-Flop TD-212A/G.
J Package-----	Pulse Generator SG-258A/G.
K Package-----	Gated Flip-Flop TD-213A/G.
L Package-----	Pulse Generator SG-259A/G.
M Package-----	Pulse Generator SG-260A/G.
E Package-----	Pulse Generator SG-261A/G.
T/J Package-----	Transmitter Unit Subassembly MX-2341A/G.
T/K Package-----	Transmitter Unit Subassembly MX-2342A/G.
T/N Package-----	Transmitter Unit Subassembly MX-2344A/G.
AS/A Package-----	Amplifier-Synchronizer Unit Subassembly MX-2345A/G.
AS/B Package-----	Amplifier-Synchronizer Unit Subassembly MX-2346A/G.
AS/C Package-----	Amplifier-Synchronizer Unit Subassembly MX-2347A/G.
AS/D Package-----	Amplifier-Synchronizer Unit Subassembly MX-2348A/G.
AS/E Package-----	Amplifier-Synchronizer Unit Subassembly MX-2349A/G.
R/K Package-----	Receiver Unit Subassembly MX-2351A/G.
Modulator-----	Coordinate Data Modulator MD-323A/G.

b. Assembly.

Common name	Description
Data Set-----	The assembly, consisting of the cabinet and all the units normally mounted in the cabinet (<i>a</i> above), is called the data set (fig. 1).

8. Description of Coordinate Data Set AN/TSQ-36

The units of the data set are mounted on a swinging frame in the cabinet, with the front panels of the units exposed when the cabinet door is open (fig. 1). The frame can be swung around to expose the rear of the units. The units are secured to the swinging rack by means of 4, 6, or 10 panel screws. The low voltage

power supply has an additional support mounted on the inside rear of the cabinet which secures the power supply to the cabinet when the frame is in the normal position. Each unit, with the exception of the test panel, has a hinged dust cover secured in place by a single fastener. Controls and indicators of the units are mounted on subpanels so they are not disturbed when the covers (which have appropriate openings) are opened or removed. Access to the wiring of the units is provided at the front (behind the dust covers), and access to the parts is provided at the rear side of the units.

a. *Electrical Equipment Cabinet CY-2560/TSQ-36* (fig. 5). The cabinet consists of a magnesium angle frame enclosed within a riveted sheet magnesium skin. The hinged doors are made of extruded magnesium. They are equipped with sponge-rubber air seals and a rotary lock. Cables carrying the wires for external connections are terminated in four connectors. These connectors mate with an assembly of connectors attached to the rear wall of the cabinet at the access hole. The mating connectors and a framework for supporting the connectors are equipped with a rubber hood which provides an air seal for the opening. The mating connectors, the framework, and the rubber hood are not furnished with the data set.

b. *Electrical Test Panel SB-976/TSQ-36*. The test panel is the top unit on the rack. It provides means for measuring the internal power supply voltages, the transmitter and receiver reference voltages, and the transmitter output level. Switches provide means for operating the encoder and the decoder from either the external reference voltages or, if needed for test purposes, from the internal power supply voltages. Two step attenuators on the test panel facilitate the adjustment of the transmitter output level and the receiver input level. Test jacks and switches enable connections to be made to the meter on the test panel for external use.

c. *Coordinate Data Transmitter Unit T-721/TSQ-36*. This is the second unit from the top of the rack. The transmitter unit contains data processing circuits and test circuits with associated controls and indicators. These test facilities are used to check the transmitter as outlined in table VII. Operating controls mounted on the front of the panel include the auxiliary digit input switches, H, X, and Y parallax switches, and

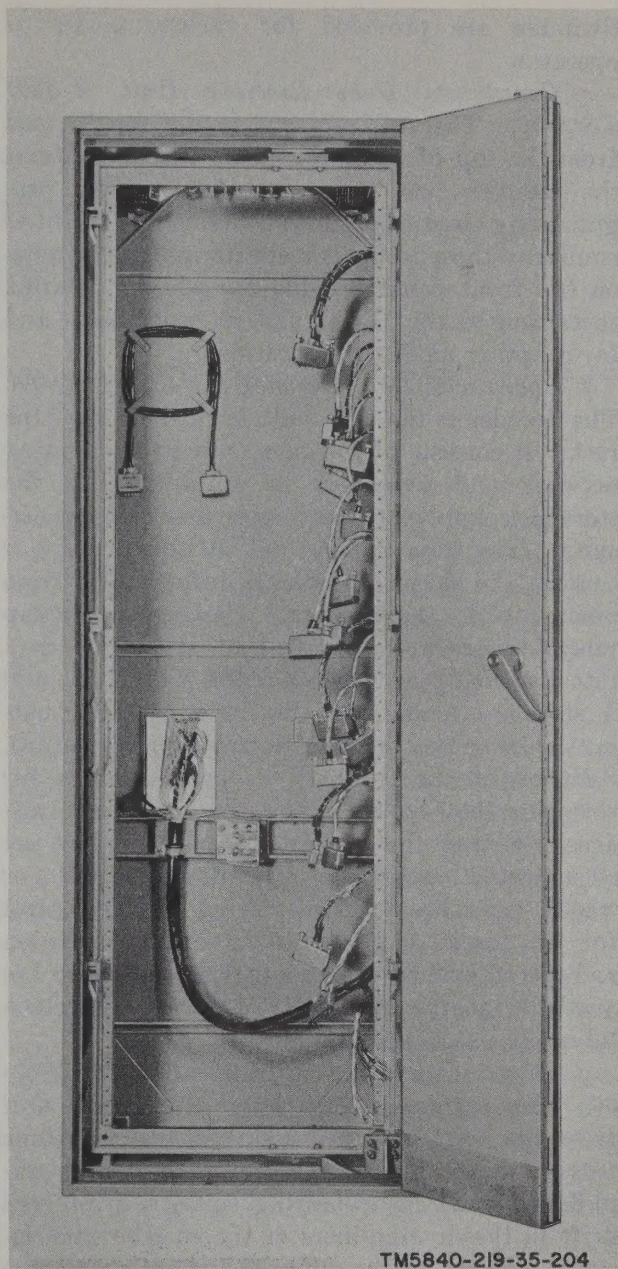


Figure 5. Electrical equipment cabinet CY-2560/TSQ-36.

switches for various modes of operation. The data transmitter modulator is a separate plug-in unit mounted on the apparatus side of the chassis.

d. *Amplifier-Synchronizer Unit AM-2126/TSQ-36*. The amplifier synchronizer is the third unit from the top of the rack. It amplifies and demodulates the incoming tone pulses for use in the receiver data processing circuits, supplies sampling pulses and program-start pulses to the receiver programming circuits, and provides a start pulse during remote start operation.

Switches are provided for various modes of operation.

e. Coordinate Data Receiver Unit R-930/TSQ-36. The receiver unit is the fourth unit from the top of the rack. This chassis contains the receiver data processing and receiver programming circuits. It also contains test facilities similar to those in the transmitter unit. Switches on the front panel provide for adding parallax correction to the H, X, and Y coordinates and for selecting modes of operation.

f. Coordinate Data Decoder KY-277/TSQ-36. The decoder is the fifth unit from the top of the rack. It consists of the data relays, the decoding network and associated dc amplifier, and the storage lockup relays and associated storage circuits. The data relays and decoding network convert the target coordinate information from binary to dc analog data. The storage lockup relays separate the single-lead sequential data into the three-lead parallel data. The H, X, and Y storage circuits store the three dc analog outputs during the inactive portions of the frame. Switches on the front of the panel provide for reversing the polarity of the reference input voltages, shorting the amplifier input for zero set adjustment, and selecting either $\pm 250\text{V}$ or $\pm 300\text{V}$ reference voltages. A calibrated control for the insertion of earth curvature correction and an adjustment for manual zero set also are available at the front of the panel. Electron tubes are used in the decoder.

g. Direct Current Amplifier AM-2125/TSQ-36. The automatic zero set is the fourth unit from the bottom of the rack and contains four automatic zero set control amplifiers. These amplifiers furnish compensating voltages to prevent drift in the dc amplifiers of the encoder and decoder. Three are used for the encoder and one for the decoder. There are no controls on the front of the panel.

h. Coordinate Data Encoder KY-278/TSQ-36. The encoder is the third unit from the bottom of the rack. Front panel controls of the

encoder include the earth curvature correction control, three zero-set adjustments and associated switches, an adjust switch used in delay adjustments, a slope trimmer adjustment, and reference voltage transfer switches. Behind the front cover are two threshold adjustments and a reset level adjustment. The encoder converts incoming dc coordinate data voltages proportionate to a number of 100-kc pulses. These pulses are converted to binary coordinate data in the transmitter data processing circuits. As in the decoder, electron tubes are used as active circuit elements.

i. Power Supply PP-2235/G. The low voltage power supply is the second unit from the bottom of the cabinet. It provides the +4.5-volt, -20-volt, -70-volt, and regulated +150-volt dc power for functional units of the data set. It also provides unregulated filament power. The fuses, their associated indicator lamps, and the control switches for the low voltage power supply are mounted on the front panel.

j. Power Supply PP-2236/G. This unit is the bottom unit in the rack. Front panel facilities of this power supply include the AC ON and DC ON switches, primary-power and dc-power indicator lamps, primary-power and dc-power fuses, +300-volt and -300-volt adjustments and associated test points, and a double ac-power convenience receptacle. This unit receives the ac primary input power (60-cycle, 105 to 130 volts) and furnishes +300-volt, -300-volt, and +75-volt dc power for the functional units in the system. It also controls the primary power to the low voltage power supply and blowers.

9. Additional Equipment Required

No cables are supplied with the equipment. The recommended wire types and sizes for external connections are listed in paragraph 19. Cable connectors to mate with the data set connectors and rubber hoods to seal the cabinet openings are not furnished with the data set, but are furnished with the associated equipment for application to the data set.

CHAPTER 2

INSTALLATION

Note. This chapter covers general and typical procedures incident to the installation of Coordinate Data Set AN/TSQ-36. For installation in a particular system, refer to the applicable system manual.

Section I. SERVICE UPON RECEIPT OF DATA SET

10. Siting

The data set is normally installed in a trailer. The specific situation and local conditions will dictate the general area where the trailer will be located. When selecting the general area, observe the following: the need to place the trailer where it will not be seen; the terrain; and the conditions for installing communication facilities.

11. Trailer Requirements

The trailer for housing the equipment must meet the following requirements:

a. The ceiling must be high enough to permit the installation of a ventilating duct at the top of the cabinet. Sufficient space must be allowed for the installation of a ventilating duct at either the lower right-hand or lower left-hand side of the cabinet. Enough room must be left for repair work and for door swing. Dimensions of the cabinet and the door swing are given in figure 7.

b. A supply of filtered air, capable of maintaining the internal temperature within the range of 25° and 125° F., must be available.

c. A suitable ac source of 115 to 130 volts, 58 to 62 cycles, capable of furnishing approximately 620 watts, must be available. A system ground connection near the operating location of the cabinet is required.

12. Packaging Data

(fig. 6)

When packed for shipment, the data set is wrapped in grade A and corrugated paper, and packed in a modified Federal Specification TPB601 case with two skids. A typical crate

packed for shipping weighs approximately 565 pounds, is 76 inches long, 27 inches wide, 20 inches deep, and has a volume of 23.4 cubic feet. Technical manuals are wrapped separately.

13. Unpacking Equipment

(fig. 6)

Perform the steps outlined below when unpacking the equipment. The cabinet is not fastened to the packing case, but floats on the rubber pads.

a. Place the packing case with the skid side down as near the operating position as is convenient.

b. Cut and fold back the two metal straps.

c. Remove the nails from the top of the case with a nail puller. Do not attempt to pry off the top or the equipment may become damaged.

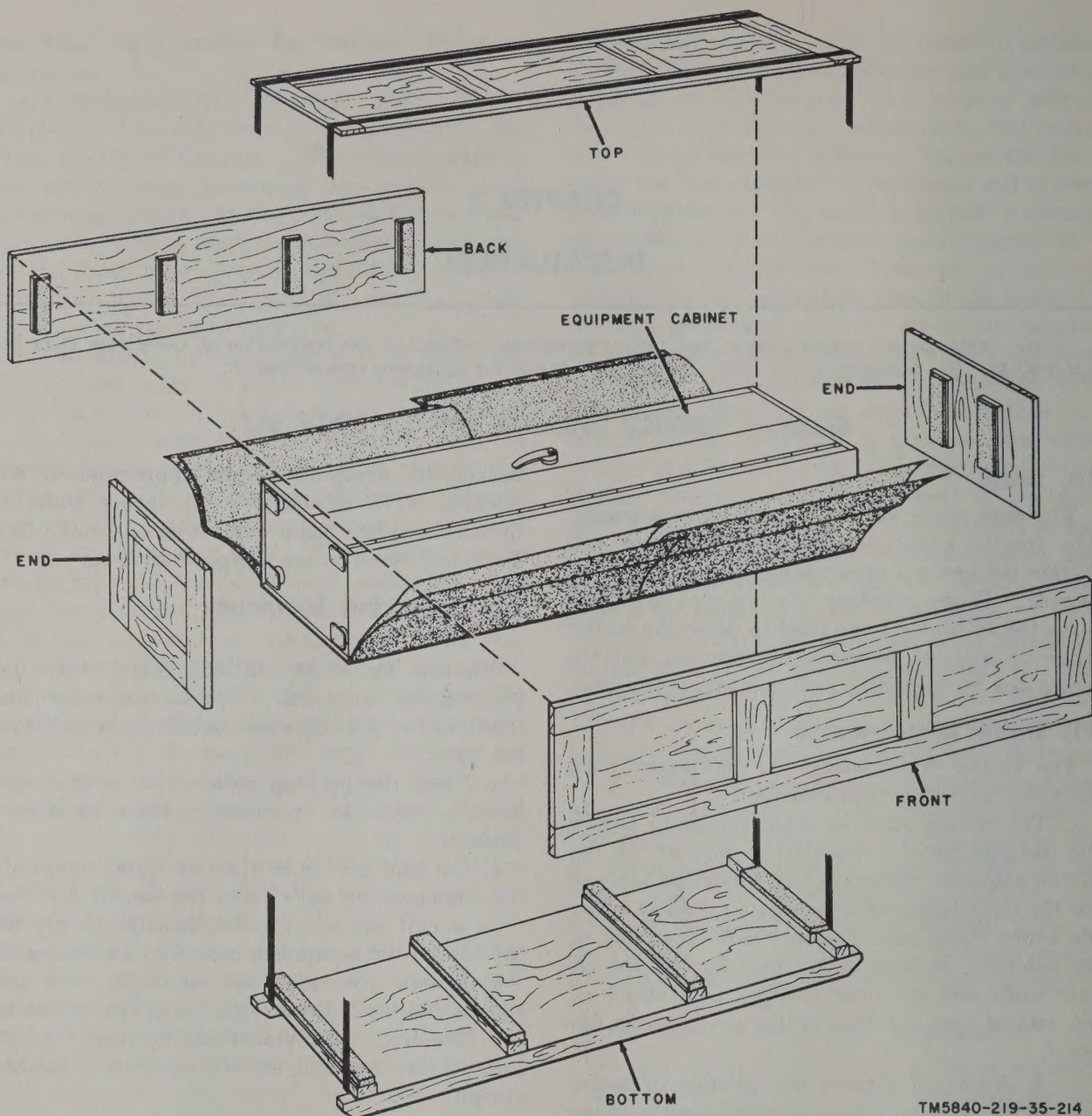
d. Remove the nails that secure the sides and ends of the case. Remove the sides, top, and ends.

e. Remove the equipment cabinet from the bottom of the case and set the equipment cabinet upright.

f. Remove the paper wrapping from the equipment cabinet.

14. Checking Unpacked Equipment

a. General. After the equipment is uncrated, make a thorough inspection for damage incurred during shipment. If the equipment has been damaged or is incomplete, refer to paragraph 2. Paragraphs *b* through *h* below give detailed instructions. Before the rack within the cabinet can be swung on its top and bottom bearings, a latch supporting the rear of the low voltage power supply must be released, and the six latches around the frame of the rack must be released.



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Figure 6. Packaging of coordinate data set AN/TSQ-36.

Perform the following steps to release these latches:

- (1) Release the Dzus fastener on the dust cover of the low voltage power supply by turning it one-quarter turn to the left, and open the dust cover.
- (2) On the low voltage power supply, slide the two slide fasteners located directly above the filter capacitors to release the capacitor panel. Lower the panel on its hinges.

- (3) Reach through the opening and swing the handle (fig. 7, section DD), upward to release the latch (see *note* below).

Note. On the low voltage power supply, open front cover ($\frac{1}{4}$ -turn fastener), drop control panel (3 slide fasteners), and turn handle to horizontal position.

- (4) Close and secure the capacitor panel. Close and latch the dust cover.
- (5) At each of the frame latches, swing the latch lever upward 90° , and toward the

center of the cabinet. This withdraws the bolt fastening the rack frame to the cabinet. The rack can now be swung on its bearings.

b. Complete Equipment. Check that the equipment is complete as listed on the packing slip. Use the table of components in paragraph 7 and the packing data in paragraph 12 to check items not listed on the packing slip.

c. Used or Reconditioned Equipment. If the equipment has been used or reconditioned, see if it has been changed by a modification work order (MWO). If the equipment has been modified, the MWO number will appear near the nomenclature plate. Check to see that this MWO number also appears on the applicable schematic diagrams in this manual. If not, add a note to the applicable schematic diagrams.

d. Cabinet and Panels. Check that the cabinet was not damaged in shipment. Check all panel covers, handle, equipment rack latches, and other hardware for damage. Check that the blowers turn freely. The cabinet door should fit snugly against the sponge rubber stripping.

e. Front Panel Components. Check for broken, bent, loose, or missing front panel components such as controls, switches, fuse holders, lamps, dials, and meters.

f. Rack. Check the rack for mechanical operation. Swing it open slowly and check that it turns smoothly. Check for excessive play in bearings. The frame should not contact the cabinet or blowers while swinging. Latches should line up when the rack is in place.

g. Cables and Connectors. Swing the rack and check that cables move freely in and out of cable guides. Check all visible cables for damage, such as frayed covering, and ends pulled from connections. Check all visible connectors, including terminals at the rear of the cabinet, for damage.

h. Functional Components. Check all visible components at the front and rear of the rack. Open all front panel covers and inspect the wiring sides. Turn the rack and check the visible components on the rear side. Check that all holddowns remain secure in the equipment. If any is discovered to be loose, secure the packages first, then fasten the holddown. Check that all plug-in components, including electron tubes, are properly seated.

15. Special Tools and Test Equipment Required for Installation

No special tools or test equipment are furnished with the data set. Tools required for making interconnections are furnished with the associated equipment and are listed below. Refer to literature on the associated equipment for instructions for the use of the tools.

- 1 Crimping tool; used for crimping wire to the connector pins.
- 1 Removal tool; used for removing the pins from the connector blocks.
- 1 Electronic Multimeter ME-30A/U; used for measuring ac voltage.

16. Installation of Equipment

(fig. 7)

a. General. The following installation procedures are necessarily general because of the many conditions under which the data set may be installed. General mounting information is given for trailer installation. Before the installation procedure is started, the equipment location must be determined as outlined in paragraph 10. Figure 7 is a drawing of the cabinet showing pertinent installation details such as overall dimensions, mounting centers, door swing, and cabinet details.

Caution: While making the following installation, have enough help on hand in order to avoid accidental injury to personnel or damage to equipment.

b. Cabinet. The trailer in which the data set is to be installed is equipped with shock mount plates for securing the data set in place. Perform the following steps when installing the cabinet:

- (1) Use a hand truck, or similar device, and set the cabinet on the floor-mounted shock mount plate.
- (2) Open the cabinet door. Open the front cover on the low voltage power supply. Swing down the hinged assembly on the low voltage power supply by releasing the three slide fasteners near the top of the unit. Turn the metal handle near

Figure 7. Coordinate data set AN/TSQ-36, installation drawing.

(Contained in separate envelope)

the center of the power supply chassis one-quarter turn to release the chassis from the rear cabinet support. Swing the rack frame about 90°.

- (3) Visually align the holes in the bottom of the cabinet with the threaded holes in the shock mount plate. Secure the cabinet to the shock mount plate using bolts furnished with the plate.
- (4) If the cabinet is to be secured to one side of the trailer, secure it to the shock mount plate (part of the trailer) by bolts passed through the two elongated holes at the rear of the cabinet near the upper right-hand and upper left-hand corners.

c. Ventilation. The trailer is equipped with a duct formed to fit at the top of the cabinet for the entrance of filtered air through the cabinet openings. The end of the duct is flanged and

equipped with O-rings to prevent leakage of air. A second duct is formed to fit over the cabinet opening at either side of the cabinet near the bottom. Only one of these openings is used, depending on the arrangement of equipment in the trailer. Cover the unused opening with the cover plate which is shipped in place over the left-hand side opening. Check that the two ducts fit tightly against the cabinet at the openings to ensure that the O-rings make a tight seal. Set the AC ON switch on the high voltage power supply to the off position (down).

17. Tubes

All electron tubes are shipped in their sockets. The following table lists all electron tubes by major units, and refers to the appropriate illustration showing the location of each tube. Check that all tubes are in their correct sockets by using table I and the referenced illustrations.

Table I. *Electron Tubes*

Tube type	Encoder (fig. 137)	Amplifier synchronizer (fig. 143)	Decoder (fig. 138)	Automatic zero set (fig. 145)	Low voltage power supply (fig. 154)	High voltage power supply (fig. 136)	Total each type
5651WA						1 (V1)	1
5687	4 (V3, 6, 13, 16).		1 (V3)		1 (V2)		6
5726/6AL5W	1 (V14)						1
5755	3 (V1, 4, 11)		1 (V1)				4
5963	3 (V9, 10, 17)						3
5R4GY						4 (V9-12)	4
6336						2 (V6, 8)	2
6AK6	1 (V15)						1
6AQ5				2 (V2, V3)			2
6AS6		1 (V1)					1
6AU6	3 (V2, 5, 12)		1 (V2)			2 (V4, 14)	6
12AT7		2 (V2, 3)	3 (V4, 5, 6)				5
12AX7	2 (V7, 8)			5 (V1, 4-7)		2 (V3, 5)	9
OA2					1 (V1)		1
OA3/VR75						1 (V7)	1
OB2WA						2 (V2, 13)	2
Total	17	3	6	7	2	14	49

18. Fuses

All fuses are shipped in place. Be sure that the proper fuses are inserted in the fuse holders

of all components in the power supplies. Table II lists all fuses by major units and refers to the appropriate illustrations showing the location of each fuse.

Table II. Fuses

Unit	Circuit designation	Designation	Rating	Circuit
Low voltage power supply (fig. 20).	F1	F02D2400B	2 amp	Ac input +4.5 and -20 volts.
	F2	F02G3R00A	3 amp	+4.5-volt dc output.
	F3	F02G4R00A	4 amp	-20-volt dc output.
	F4	F02D1R50B	1.5 amp	Ac input to unregulated filament and lamp supply.
High voltage power supply (fig. 17).	F1	SM-B-130562	7 amp	Convenience receptacles.
	F2	SM-B-130562-3	3 amp	Ac input filament transformer.
	F3	SM-B-130562-2	5 amp	Ac input plate transformer.
	F4	SM-B-130562	7 amp	Ac output to low voltage power supply and blowers.
	F5	SM-B-130562	7 amp	Ac output to low voltage power supply and blowers.
	F6	SM-B-130563	0.4 amp	+300-volt rectifier.
	F7	SM-B-130563	0.4 amp	-300-volt rectifier.

19. Preliminary Connections

(fig. 162)

a. Cabling. All units of the data set are interconnected by the internal cabling. Wires of the internal cables are terminated in connectors which mate with connectors on the individual chassis. Wires for connection to circuits external to the data set are terminated in four connectors secured by a cable clamp at the inside rear of the cabinet below the access hole. All external connections to the data set are made to these four connectors by means of mating connectors not furnished with the data set. A rubber hood at the outside of the cabinet at the access hole provides an airtight seal. The hood is not furnished with the data set.

b. Cables. No cables for external connections are furnished with the data set. The recommended wire type and size for the various external circuits are listed below. The external circuits must be terminated with Burndy type PD35F-1 connectors to mate the plugs on the data set.

Terminal	Circuit	Recommended Wire (AWG)
P18A-1-10	Auxiliary digits input	18.
P18A-11-20	Auxiliary digits output	18.
P18A-21	Receiver TSG 14	18.
P18A-22	All data present	18.
P18A-23	Transmitter TSG 58	18.
P18A-24	Transmitter TSG 1	18.
P18A-25	RTC indicator	18.
P18A-26	Transmitter TSG 53	18.
P18A-27	Ready tone control start	18.
P18A-28	Ready tone control stop	18.
P18A-30	Receiver TSG 0	18.

Terminal	Circuit	Recommended Wire (AWG)
P18A-32	Acknowledge remote start receiver pulse.	18.
P18A-33	S01-2	18.
P18A-34	S01-1	18.
P18A-35	Receiver TR 00	18.
P18B-1	-6-volts control bias	18.
P18B-2	Receiver UR 1 or UR 0	18.
P18B-3	-300-volt reference	18 shielded.
P18B-7	Receiver auxiliary common	18.
P18B-8, 9	Transmitter line out	18 double shielded.
P18B-10	Receiver CP	18 shielded.*
P18B-11	Transmitter CP	18 shielded.*
P18B-12	Receiver CP	18 shielded.*
P18B-13	G/S data out	18 shielded.
P18B-14	G/S data in	18.
P18B-15	Acknowledge transmission	18.
P18B-16, 17	Receiver line input	18 double shielded.
P18B-18	Receiver TSG 51	18 shielded.
P18B-19	Reference common	18.
P18B-26	+300-volt reference	18 shielded.
P18C-1, 2	X and Y analog	18 double shielded.
P18C-5, 6	115V ac input	14.
P18C-7	Receiver CP	18 shielded.*
P18C-8	Start transmitter pulse	18 shielded.
P18C-9	Remote start receiver pulse	18 shielded.
P18C-12, 13, 14	Y, X, H coordinate output	18 triple shielded.
P18C-15, 16, 17	Y, X, H coordinate input	18 triple shielded.
P18D-1	Height unknown pulse	18.
P18D-2	Receiver TSG 23	18.
P18D-3-10	Height comparator detector data.	18.

* These wires should be RG-122/U coaxial cable if the run is greater than 10 feet.

Terminal	Circuit	Recommended Wire (AWG)
P18D-11----	Receiver TSG 29-----	18.
P18D-13----	Transmitter TSG 7-----	18.
P18D-14----	Transmitter TSG 40-----	18.
P18D-16----	ACQ reference common----	18 triple shielded.
P18D-17----	ACQ +reference-----	
P18D-18----	ACQ -reference-----	
P18D-19----	Transmitter auxiliary 11--	18.
P18D-20----	Transmitter auxiliary 12--	18.
P18D-21----	Serial data-----	18.
P18D-22----	Receiver auxiliary 11 gate-	18.
P18D-23----	Receiver auxiliary 12 gate-	18.
P18D-31----	Comparator reference com- mon.	18 triple shielded.
P18D-32----	Comparator -reference---	
P18D-33----	Comparator +reference---	
P18D-34, 35.	Chassis ground-----	18.

c. *Terminals.* Connections are made to the pins of the connectors as follows:

- (1) Remove the pin to which the connection is to be made. A removal tool and instruction for its use are furnished with associated equipment.
- (2) Insert the wire to be connected into the pin.
- (3) A crimping tool to crimp the pin to the wire and instructions for their use are furnished with associated equipment.
- (4) Insert the pin into the proper hole in the plug and apply pressure until the pin snaps into place.
- (5) Determine that the pin is properly seated by pulling lightly on the wire. The pin should remain in place.

d. *Power and Ground Connections.* Connect the 115-volt external primary source wires to pins 5 and 6 of P18C. Connect power line protective ground (conduit or ground wire) to pin 34 or 35 of P18D. Connect pin 34 or 35 of P18D to the cabinet ground terminal E2, and connect E2 to the building or system ground.

20. Wiring Options

a. *General.* After the preliminary connections have been made, wire the encoder for the operating target voltage range and the low voltage power supply for the average line voltage.

b. *Encoder.* Three options are available for the encoder: Option A for operation with a target voltage range of ± 100 volts, and option B for operation with a target voltage range of ± 50 volts. The encoder is prewired for option B. If option A is used, unsolder the wire from terminal 5 of Z2 (fig. 136) and solder it to terminal 4 of Z2. Check that pins 6 of V1, V4, and V11 are

not grounded if automatic zero set (AZS) is used (option C). If AZS is not used, connect pin 6 of these three tube sockets to ground (fig. 136).

c. *Low Voltage Power Supply.* The low voltage power supply has been wired for operation from a nominal line voltage of 117 volts. Taps on the primary winding of transformer T1 (fig. 152 and 182) permit adapting the power supply to the existing nominal line voltage. The transformer is shipped with the option lead connected to terminal 3. Using VTVM(ac), measure the line voltage. If the measured line voltage is nearer 122 volts than 117 volts, unsolder and remove the wire from terminal 3 and solder it to terminal 4. If the measured line voltage is nearer 111 volts, connect the lead to terminal 2.

d. *Automatic Zero Set Options.* The automatic zero set has four circuits, three of which are used with the encoder and one with the decoder (par. 133). Check on the rear of the cabinet to see that the cables between the automatic zero set and the encoder and decoder are connected to the jacks as shown in the following chart:

AZS-----	J2	J3	J4	J5	J6	J7	J8	J9
Encoder-----	J4	J3	J6	J5	J8	J7		
Decoder-----							J4	J5

21. Exercising Data Relays

Caution: It is very important that the mercury data relays are exercised properly before the reference voltages are applied to the data set. This is necessary so that any mercury that may have collected between contacts during shipment or replacement is shaken free. Damage to the equipment probably will result if this precaution is not taken. The procedure for exercising these relays is outlined below.

a. Set all controls as directed in table III, except as indicated below.

b. Set all 10 H parallax switches on the receiver unit at 1 (up).

c. Set AC ON switch on high voltage power supply on (up).

d. Allow the equipment to run continuously for at least five minutes.

e. Set the AC ON switch off (down).

f. Set the 10 H parallax switches on the receiver unit at 0 (down).

Section II. INITIAL ADJUSTMENT OF EQUIPMENT

Note. The procedures described in this section should be performed by an installer or equipment repairman.

22. Extent of Initial Adjustments

This section covers initial adjustments which must be made at the data set location as soon as the set is installed. The system line level adjustments (par. 26) should be performed after the initial adjustments have been completed.

23. Test Equipment Required for Adjustment

The test equipment required for initial adjustment of the data set is listed below. A common usage name is indicated after each item.

<i>Nomenclature</i>	<i>Common name</i>	<i>Technical manual</i>
Oscilloscope, AN/USM-81.	Oscilloscope..	
Voltmeter ME-30A/U...	VTVM (ac)'	TM 11-5132.
Electronic Multimeter TS-505/U.	VTVM (dc)	TM 11-5511.

24. Preliminary Setting of Controls

The preliminary control settings described in table III should be made before power is applied to the equipment. The specific settings and selections should be made in accordance with the information presented in the table. Controls that are not listed in the table may be left in any position at this time.

Table III. Preliminary Control Settings

Unit	Control	Position
Test panel (fig. 8).	REC LINE.....	EXT (up).
	ENC REF *.....	EXT (down).
	DEC REF *.....	EXT (down).
	XMTR AT (db)...	0.
Transmitter unit (fig. 9).	CONTINUOUS-REMOTE START.	Continuous.
	PC.....	Up.
	IND LP.....	Up.
	AUX (10 switches).	Down.
	P _H , P _X , P _Y	Down.
	DBL SCALE-SGL SCALE.	Depends on mode of operation desired (par. 37).
	CDG/TAC-OC...	Depends on location and associated equipment.

See footnote at end of table.

Table III. Preliminary Control Settings—Continued

Unit	Control	Position
Amplifier synchronizer (fig. 11).	NORM-RS.....	NORM (up).
	CDG/TAC-OC...	Depends on location and associated equipment.
Receiver unit (fig. 12).	P _H , P _X , P _Y	Down.
	TDC.....	Up.
	DBL SCALE-SGL SCALE.	Depends on mode of operation desired (par. 37).
	IND LP.....	Up.
	DATA.....	NORM (up).
	PC.....	NORM (up).
	READY.....	NORM (up).
	TPC.....	NORM (up).
	GROUND-SLANT.	GROUND.
	NORMAL-REVERSE.	NORMAL (up).
Decoder (fig. 13).	REF.....	Set to agree with reference voltage used.
		0.00.
Encoder (fig. 14).	EARTH CURVATURE CORRECTION.	0.00.
	EARTH CURVATURE CORRECTION.	0.00.
	OPR-ADJ (sweep generator).	OPR (up).
	OPR-ADJ (target comparator amplifier).	OPR (up).
	OPR-ALIGN.....	OPR (up).
	250V REF-300V REF.	Set to agree with reference voltage used.
High voltage power supply (fig. 16).	DC ON.....	On.
	AC ON.....	Off.
Low voltage power supply (fig. 15).	+4.5V & -20V SUP.	ON (up).

*If system reference voltages are not available, operate these switches to INT. Encoding and decoding while using the internal plus and minus 300 volts will be inaccurate. Set encoder and decoder REF switches at 300V before putting switches in INT position (par. 20).

25. Adjustments for Operation

Table IV describes the procedure for adjusting controls which require a single setting. (See pars. 29-36 for the function of the control settings.) Table IV is used in the initial installa-

tion procedure, or when a unit is found to function improperly, as indicated by the equipment performance checklist (table V). Unless otherwise directed, preset all operational controls as specified in table III.

Table IV. Adjustments for Operation

Step	Unit	Control	Function	Method of setting
1	High Voltage Power Supply (fig. 16).	-300 VOLTAGE ADJUST. +300 VOLTAGE ADJUST.	Adjusts -300-volt output. Adjusts +300-volt output.	Connect the VTVM (dc) between -300 and COM test jacks. Adjust -300 VOLTAGE ADJUST for -300 volts. Connect the VTVM (dc) between the BAL and COM test jacks. Adjust +300 VOLTAGE ADJUST for 0 volt on the meter. Connect the VTVM (dc) between the +300 and COM test jacks and check for +300 volts. The values of +300 and -300 volts should be equal. If necessary, recheck the balance.
2	Low Voltage Power Supply (fig. 15).	LAMP SUP ADJ VOLTS.	Adjusts neon indicator lamp supply voltage.	Set TARG COMP AMP OPR-ADJ switch on the encoder at ADJ (fig. 14). Set the H, X, and Y parallax switches on the transmitter unit (fig. 9) at alternate ONE's (up) and ZERO's (down) for a code of 1010101010, etc. Set the PC switch on the transmitter unit panel at test (down). Advance the program generator manually by pressing the PULSE button once for each step. Observe the shift register indicator lamps. Adjust LAMP SUP ADJ VOLTS on the power supply so the lamps light and extinguish as the shift register advances.
3	Modulator (fig. 10) (part of transmitter unit).	1,500~LEV-----	Adjusts the 1,500-cycle oscillator feedback voltage (fig. 159(10)).	Set OPR-ADJ switch on the encoder at OPR. Set PC switch on the transmitter unit panel at normal (up). On the transmitter unit panel set the TENS switch at 0 and the UNITS switch at 4. Set the PC switch on the transmitter unit panel at test (down). Press the RECYC switch until the ring counters stop. Synchronize the oscilloscope at SYNC on the transmitter unit panel.

Table IV. Adjustments for Operation—Continued

Step	Unit	Control	Function	Method of setting
3				Connect the input of the oscilloscope to TP1 of the modulator and ground. Observe 1,500-cycle signal. Adjust 1,500~LEV for maximum signal at the point where distortion becomes apparent (about 25%) (fig. 159(10)). Lock the control. Caution: Never use 1,500~LEV to adjust the level of the line output. If the adjustment is set too low, the oscillations will die out.
4	Modulator (fig. 10) (part of transmitter unit).	MOD-----	Adjusts the modulation percentage.	Connect the oscilloscope input to input terminal 1 of T1 and ground of the test panel (fig. 157). Set the PC switch at normal (up). Set the H parallax switches for 5 ZERO's and 5 ONE's for a line code of 0000011111. Adjust the oscilloscope to observe the line code. Adjust the MOD control until the 1,500-cycle signal for the last 3 ZERO's is 5% of the level of the last 3 ONE's.
5	Modulator (fig. 10) (part of transmitter unit).	600~LEV-----	Adjusts the 600-cycle oscillator level.	Note the level of the last 3 ONE's With the oscilloscope connected as in step 4, set the PC switch at test (down) and set the TENS switch at 5 and the UNITS switch at 6. Adjust 600~LEV potentiometer until the amplitude of the 600-cycle signal is the same as the level of the 1,500-cycle signal measured in step 4.
6	Amplifier Synchronizer (fig. 11).	OSC ADJ (R25)-----	Adjusts the 1,500-cycle oscillator feedback voltage.	Set XMTR AT (db) on the test panel to the setting for normal operation (par. 26d). Connect the oscilloscope to E1 and ground on the amplifier synchronizer and observe the waveform. Turn OSC ADJ clockwise to increase the feedback. Set the control to the point where the positive peaks are flattened and the negative peaks begin to show distortion. Lock the control.

Table IV. Adjustments for Operation—Continued

Step	Unit	Control	Function	Method of setting
7	Amplifier Synchro- nizer (fig. 11).	DATAADJ (R17) (CDG/ TAC operation).	Determines the data slic- ing level.	Set the transmitter group TENS switch at 0 and the UNITS switch at 6. Set the EXT-LOCAL switch on the test panel at LOCAL. Connect the oscilloscope input to test point E3 on the amplifier synchronizer, and synchronize the oscilloscope at SYNC test jack on the transmitter unit panel. Operate the even H parallax switches up and the odd switches down. Set CDG/TAC-OC switch at CDG/TAC. Adjust DATA ADJ control to obtain equal widths of the ONE's and ZERO's.
8	Amplifier Synchro- nizer (fig. 11).	OC LEVEL (R41) (OC operation).	-----	Set all switches as in step 7. Set CDG/TAC-OC switch at OC. Adjust OC LEVEL control to obtain equal widths of ONE's and ZERO's.
9	Amplifier Synchro- nizer (fig. 11).	READY ADJ (R13)-----	Determines the ready slicing level.	Connect the oscilloscope input to test point E4 and synchronize the oscilloscope at SYNC test jack on the transmitter unit panel. Set the TENS switch on the transmitter unit panel at 5 and the UNITS switch at 6. Adjust READY ADJ control to produce a sliced ready signal having a width of about 4 milliseconds.
10	Encoder (fig. 14)-----	ZERO SET (R7) (sweep generator).	Adjusts the sweep gen- erator for zero out- put when the input is shorted.	On the encoder, set the OPR-ADJ switch S1 at ADJ. Connect the input of the oscilloscope to pin 2 of chopper K1 of the automatic zero set panel (fig. 143(1)). Synchronize the oscilloscope at SYNC test jack on the transmitter unit panel using any time slot, and adjust the sweep length to about 70 milliseconds. Make a note of the level of the signal. Rotate the sweep generator ZERO SET control sharply about one turn in either direction. Note that the amplitude of the observed signal changes to a new level and then returns to approximately the original level as the AZS amplifier corrects for the error introduced. Adjust the ZERO SET control for minimum amplitude of this signal. Set S1 to OPR.

Table IV. Adjustments for Operation—Continued

Step	Unit	Control	Function	Method of setting
11	Encoder (fig. 14)----	ZERO SET (R30) (target amplifier).	Adjusts the target amplifier for zero output when the input is shorted.	On the encoder, set the OPR-ADJ switch S2 at ADJ. Connect the oscilloscope input to pin 2 of chopper K2 of the automatic ZERO SET (fig. 143(1)). Synchronize and adjust the oscilloscope as in step 10. Adjust the target amplifier ZERO SET control for minimum amplitude as in step 10. Set S2 at OPR.
12	Encoder (fig. 14)----	ZERO SET (R58) (reference amplifier).	Adjusts the reference amplifier for zero output when the input is shorted.	On the encoder set the OPR-ADJ switch S3 at ADJ. Connect the oscilloscope input to pin 2 of chopper 3 of the automatic ZERO SET (fig. 143(1)). Synchronize and adjust the oscilloscope as in step 10. Adjust the reference amplifier ZERO SET control for minimum amplitude as in step 10. Set S3 at OPR.
13	Encoder (fig. 14)----	RESET LEVEL (R114)	Adjusts the level of the reset voltage so that the sweep voltage is between +53 and +55 volts during reset time and passes through -55 volts before sweep reset. The entire waveform is moved up and down when this control is operated.	Using the dc input to the oscilloscope, synchronize at the SYNC jack on the transmitter unit panel at any time slot. Short the oscilloscope input terminals and adjust the vertical positioning of the trace to coincide with a reference mark. Remove the short. Connect the oscilloscope input to TP1 on the encoder. Adjust RESET LEVEL control so that the sweep voltage passes through -50 volts, and the reset level during reset time is between +53 and +55 volts (fig. 25). Lock the control.
14	Encoder (fig. 14)----	Target and reference delay controls (C46 and C47).	<i>Note.</i> Before making these adjustments, allow the equipment to warm up for 1 hour. The target and reference delay controls are used to compensate for any difference in delay between the target and reference comparison channels.	Set TARGET THRESHOLD ADJUST and REFERENCE THRESHOLD ADJUST at their maximum CCW positions. Set the target and reference delay controls, C46 and C47, at minimum capacitance (with the silver portion of the rotor parallel with the terminals and on the side away from the terminals). Set OPR-ALIGN switch at ALIGN.

Table IV. Adjustments for Operation—Continued

Step	Unit	Control	Function	Method of setting
14			Delay differences result from small manufacturing tolerances. These controls are adjusted for coincidence of the gate-open and gate-close pulses with target and reference inputs shorted to REF COM, but with sweep voltage applied.	Adjust C46 or C47, or both, until the binary counter indicator lamps on the transmitter unit panel go off. Continue to adjust C46 and C47, using the least amount of capacitance possible, until BC1 lamp flickers occasionally, but the other 9 lamps remain off. Repeat the test after 5 minutes and readjust if necessary.
15	Encoder (fig. 14) ----	TARGET THRESHOLD ADJUST (R124) and REFERENCE THRESHOLD ADJUST (R134).	These controls perform the same function as C46 and C47 described in step 14. These controls should be left at their maximum CCW position, corresponding to minimum delay, unless the range of C46 and C47 is not great enough for proper delay adjustments.	In the event that C46 and C47 cannot be adjusted to yield coincidence of the gate-open and gate-close pulses, set them at positions giving the lowest binary number. Adjust R124 and R134 separately, leaving the one that affects coincidence unfavorably at its maximum CCW position to avoid unnecessary circuit delay. Lock the controls.
16	Encoder (fig. 14) ----	SLOPE TRIMMER (R23).	This control varies the slope of sweep voltage over a small range. It is adjusted to yield the correct number of 100-kc output pulses after the amplifier delay controls have been set. Zero dc input is used to provide half-scale (512) output.	Set OPR-ALIGN switch at ALIGN. Set the PC switch on the transmitter unit panel to the normal (up) position. Set up the oscilloscope to observe the line signal (step 3), and synchronize the oscilloscope at TS 17. Set all parallax and auxiliary switches at 0 (down). Adjust R23 while observing the line code. Set R23 at the point which yields the half-scale binary pattern: 111111110 or 000000001. Lock the control.
17	Encoder (fig. 14) ----	EARTH CURVATURE CORRECTION (R121).	This control has a calibrated dial so that a predetermined correction may be set in at the time of installation. The amount of this correction is dependent upon the distance to the remote receiver.	When this table is used for preliminary settings, set the EARTH CURVATURE CORRECTION control at 0.00. During normal operation the setting of this control will be determined by the commanding officer. The dial setting should be logged on a tag affixed to a convenient part of the data set so that if the control is disturbed, it can be reset to the correct setting.

Table IV. Adjustments for Operation—Continued

Step	Unit	Control	Function	Method of setting
18	Decoder (fig. 13) ----	ZERO SET (R6) -----	Adjusts the dc amplifier for zero output when the input is shorted.	Connect the oscilloscope to terminal 2 of chopper K4 in the automatic ZERO SET (fig. 143(1)). Synchronize the oscilloscope as in step 10. Rotate the ZERO SET control sharply about 1 turn in either direction. Note that the amplitude of the observed signal changes to a new level and then returns to approximately the original level as the AZS amplifier corrects for the error introduced. Adjust the ZERO SET control for minimum amplitude of this signal.

26. System Line Level Adjustments

After installation has been completed, it is necessary to make adjustments to the system line levels. These line levels should also be checked at regular intervals and when parts of the equipment affecting transmission are changed. The test facilities required for making these lineups are built into the data set; however, it is recommended that an ac vacuum tube voltmeter be used for the preliminary lineup.

a. Basis for System Lineup. System lineup is required to assure the proper performance of the system. The lineup consists of two phases: first, adjustment of the transmitter to be sure that it is transmitting signals of the proper amplitude or power level to the line; and second, adjustment of the receiver to be sure that signals of the proper amplitude and power level are being fed to the receiving circuits.

b. Frequency of Lineup. It is not possible to set forth one rule for determining the lineup schedules for all systems. These schedules must be determined by the performance of the specific system being maintained. Monthly and daily system lineups will indicate the need for adjusting lineup schedules.

c. Control of Lineup. All lineups are supervised by the higher echelon terminal. It is designated terminal A. The second, or lower echelon terminal, is designated terminal B. The data set at terminal B may be identical with the equipment at terminal A.

Caution: Permission to make any line level

adjustments must be obtained from the control data set (terminal A). The control data set will not allow any adjustments to be made to the equipment when it is in use. Adjustments will be allowed during scheduled maintenance periods.

d. Measurement and Adjustment of Terminal A Transmitter Power Output Level. The terminal A transmitter is measured to check its power output to the line. During normal operating conditions, the output level to the transmission line should be $0 \pm .5$ dbm. Be sure that the equipment is operating properly as indicated in table V. Then make the test as follows:

- (1) Connect a VTVM (ac) to terminals 1 and 2 of transformer T1, located on the test panel (fig. 157).
- (2) Turn the equipment on (par. 40).
- (3) Set the XMTR AT (db) control, located on the test panel, at 0.
- (4) On the transmitter unit set the PC switch at test (down), set the TENS switch at 0, and the UNITS switch at 4. Press the RECYC button. This will transmit a steady 1,500-cycle test tone to the distant receiver, located at terminal B.
- (5) Adjust the XMTR AT (db) control for a reading as close to 0 dbm as is possible.

Caution: Do not adjust the 1,500~LEV control on the modulator. This is the oscillator feedback control, not an output level control.

- (6) Set the PC switch in its normal (up) position.

e. Alternate Method of Measuring and Adjusting Terminal A Transmitter Power Output Level.

- (1) Turn the equipment on (par. 40).
- (2) On the transmitter unit set the PC switch at test (down), set the TENS switch at 0, and the UNITS switch at 4. Press the RECYC button.
- (3) Set the meter switch on the test panel at the XMTR SIG LVL position. Note the reading on the test panel meter.
- (4) Set the XMTR AT (db) control to the setting giving a meter reading on the heavy red line.
- (5) Set the PC switch at normal (up).

f. Measurement and Adjustment of Terminal B Receiver Input Level.

The input level for the receiver must be set to a value which is determined by the position of the CDG/TAC-OC switch on the amplifier synchronizer. With the switch at the CDG/TAC position, the signal level measured at REC LINE (TP4) on the test panel must be $-20 \text{ dbm} \pm 5 \text{ db}$. For the OC position the level must be $-4 \text{ dbm} \pm 1 \text{ db}$. When in CDG/TAC position, the AGC circuit of the amplifier will compensate for line level variations of $\pm 5 \text{ db}$. In the OC position, line level variations are corrected by AGC circuits in the associated equipment. Also, in the OC position, the setting of OC LEVEL R41 will have been set when adjustments for operation were made (par. 25). Measurement and adjustment of the receiver line level for CDG/TAC operation are made as follows:

- (1) Connect a VTVM (ac) from test point REC LINE (TP4) and ground of the test panel (fig. 8).
- (2) Turn the equipment on (par. 40). Have

the operator at the distant terminal transmit a 1,500-cycle test tone (*e* above).

- (3) Set the CDG/TAC-OC switch on the amplifier synchronizer (fig. 12) at CDG/TAC.
- (4) Set the REC AT (db) control on the test panel for a meter reading of $-20 \text{ dbm} \pm 5 \text{ db}$.

Measurement and adjustment of the receiver line level for OC operation are made as follows:

- (5) Perform steps (1) and (2) above.
- (6) Set CDG/TAC-OC switch on the amplifier synchronizer at OC.
- (7) Set REC AT (db) control on the test panel for a meter reading of $-4 \text{ dbm} \pm 1 \text{ db}$.

g. Measurement and Adjustment of Terminal B Transmitter Power Output Level. Use the procedures described in *d* or *e* above to measure and adjust the transmitter power output level.

h. Measurement and Adjustment of Terminal A Receiver Input Level. Use the procedure described in *f* above to measure and adjust the terminal A receiver.

27. Recording Control Settings

a. The earth curvature correction and the parallax corrections are all determined at the time of installation. As soon as these corrections are determined, set the earth curvature correction dial to the correct value, and operate the H, X, and Y parallax switches in accordance with the correction required. Set each switch representing a ONE in the up position, and each switch representing a ZERO in the down position.

b. Record this data and attach it to the data set in a conspicuous place for future reference in the event the controls are later changed inadvertently or during testing.

CHAPTER 3

PREOPERATIONAL AND STARTING PROCEDURES

Note. This chapter covers general and typical procedures incident to the operation of Coordinate Data Set AN/TSQ-36. For operation in a particular system, refer to the applicable system manual.

Section I. CONTROLS AND INSTRUMENTS

Note. This section locates, illustrates, and describes the use of the various controls and indicators that are provided for the proper operation of the equipment.

28. General

It is important to know the function of every control of the data set. The following paragraphs list the functions of all controls by major units. Refer to the appropriate panel illustrations (fig. 8-16) for control locations and panel markings. A log sheet showing the normal positions of all switches and the normal settings of all controls

should be kept so that if the switches are disturbed, they can be reset to normal.

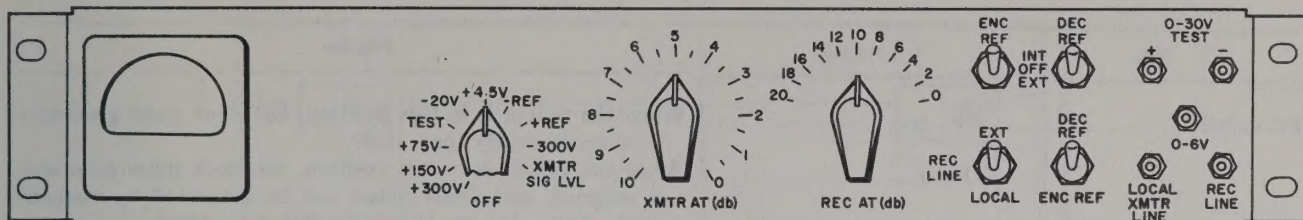
29. Test Panel

(fig. 8)

The following chart lists the controls and indicators of the test panel and describes their functions:

Item	Position	Function
Meter switch.....	+300V.....	Connects the test panel meter to measure the +300-volt output of the high voltage power supply.
	+150V.....	Connects the test panel meter to measure the +150-volt output of the low voltage power supply.
	+75V.....	Connects the test panel meter to measure the +75-volt output of the high voltage power supply.
	TEST.....	Connects the test panel meter to the test jacks TP1 and TP2 through the 0-6V TEST switch. The meter then can be used with external test leads as a general purpose voltmeter measuring up to ± 30 volts.
	-20V.....	Connects the test panel meter to measure the -20-volt output of the low voltage power supply.
	+4.5V.....	Connects the test panel meter to measure the +4.5-volt output of the low voltage power supply.
	-REF.....	Connects the test panel meter to measure the negative reference voltage (furnished by associated equipment) and the internal negative reference voltage (ENC REF below).
	+REF.....	Connects the test panel meter to measure the positive reference voltage (furnished by associated equipment) and the internal positive reference voltage (ENC REF below).
	-300V.....	Connects the test panel meter to measure the -300-volt output of the high voltage power supply.
	XMTR SIG LVL.....	Connects the test panel meter to measure the output signal level of the modulator.
	OFF.....	In this position, the switch disconnects the meter from all circuits.

Item	Position	Function
REC LINE switch	EXT	Used with the meter switch in the XMTR SIG LVL position. In the EXT position, REC LINE switch connects the meter to the output of XMTR AT (db) to measure the output level of the transmitted signal.
	LOCAL	In this position, the output of the modulator through AT 1 is applied to the receiver input through a 20-db fixed pad.
0-6V switch	Depressed	Used with the meter switch in TEST position and with external test leads. When the 0-6V switch is depressed, it gives the test panel meter a full-scale reading of 6 volts.
	Normal	Used with the meter switch in the TEST position and with external leads. In the normal position, the 0-6V switch gives the test meter a full-scale reading of 30 volts.
XMTR AT (db) attenuator		This control inserts attenuation between the modulator output and the transmitter line. The amount of attenuation is adjustable in 20 steps of .5 db each.
ENC REF switch	INT (up)	In this position the switch connects the internal high voltage power supply plus and minus 300 volts to the encoder reference terminals in place of the external reference voltages. The internal voltages are used only for testing purposes when external reference voltages are not available. The equipment normally is not operated from this supply, and encoded data is not necessarily accurate when this voltage supply is used.
	OFF (midposition)	In this position the switch removes all reference voltages from the encoder.
	EXT (down)	In this position the switch connects the external plus and minus reference voltages to the encoder reference terminals. This is the switch position for normal operation.
DEC REF switch	INT (up)	In this position the switch connects the internal high voltage power supply plus and minus 300 volts to the decoder reference terminals in place of the external reference voltages. The internal voltages are used only for testing purposes when external reference voltages are not available. The equipment normally is not operated from this supply and decoded data is not necessarily accurate when this voltage supply is used.
	OFF (midposition)	In this position the switch removes all reference voltages from the decoder.
	EXT (down)	In this position the switch connects the external plus and minus reference voltages to the decoder reference terminals. This is the switch position for normal operation.
DEC REF-ENC REF	DEC REF	Used with the meter switch in the - REF and + REF positions. In the DEC REF position, this switch connects the meter to indicate the decoder reference voltages.
	ENC REF	Used with the meter switch in the - REF and + REF positions. In the ENC REF position, this switch connects the meter to indicate the encoder reference voltages.
0-30V TEST +test point (TP1).		Used with external test leads. These jacks connect through the 0-6V switch and through the meter switch in the TEST position to the meter.
0-30V TEST -test point (TP2).		
REC AT (db) attenuator		This is a 20-db attenuator adjustable in 2-db steps. It is connected in the receiver line to provide an adjustable signal loss between the receiver line and the amplifier synchronizer input.
LOCAL XMTR LINE test point (TP3).		Used with an external meter to indicate the modulator output level when the REC LINE switch is at LOCAL.
REC LINE test point (TP4).		Used with an external meter to indicate the receiver input level.



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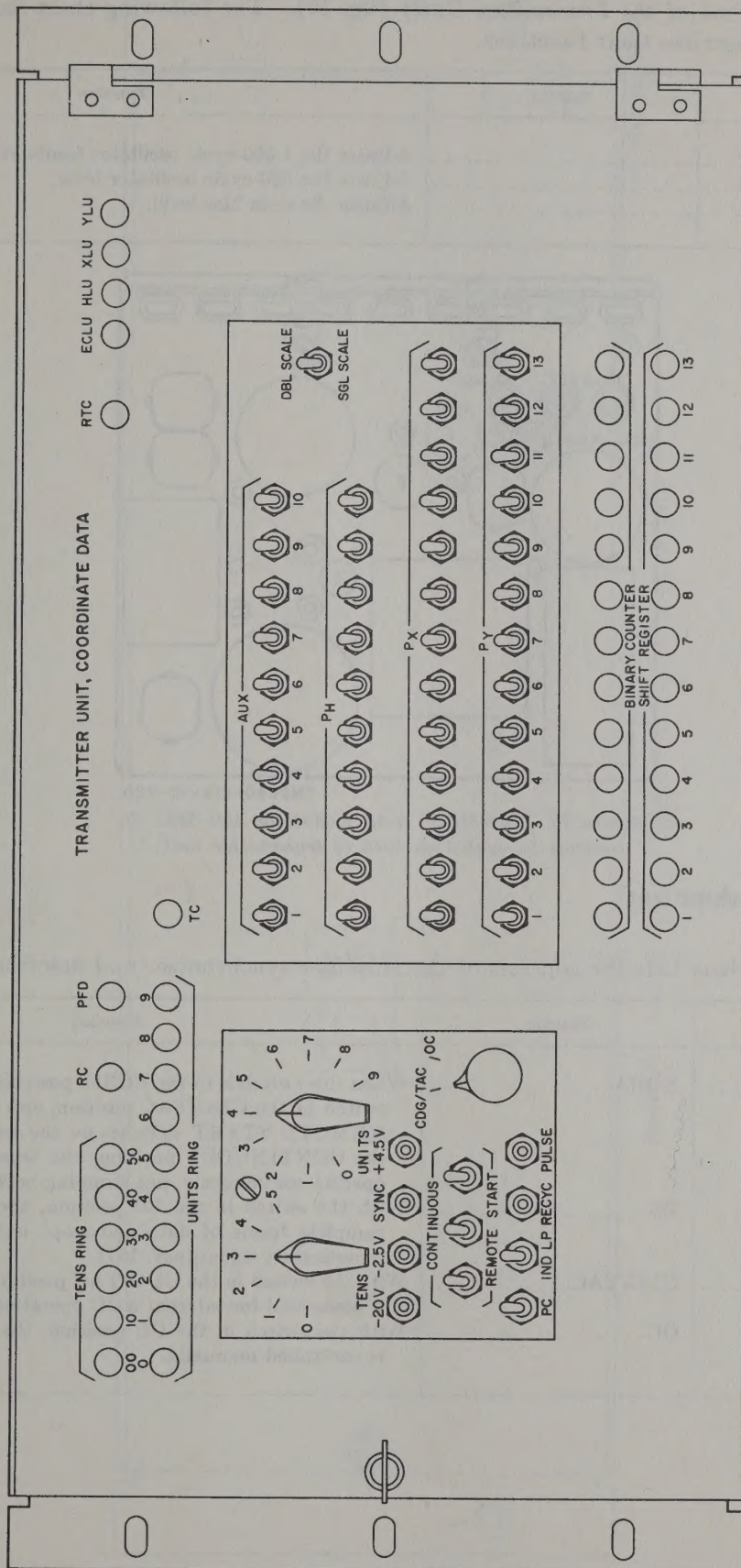
Figure 8. Electrical test panel SB-976/TSQ-36, controls.

30. Transmitter Unit

a. *Transmitter Unit* (fig. 9). The following chart lists the controls and indicators of the transmitter group and describes their functions:

Item	Position	Function
TENS RING lamps 00, 10, 20, 30, 40, 50.		When lit, these lamps indicate that the tens ring F/F associated with each lamp is ON (par. 106).
UNITS RING lamps 0 through 9.		When lit, these lamps indicate that the units ring F/F associated with each lamp is ON (par. 106).
RC lamp		When lit, this lamp indicates that the RC (reset) F/F is ON (par. 107).
PFD lamp		When lit, this lamp indicates that the PFD (pulse frequency divider) F/F is ON (par. 105c).
RTC lamp		When lit, this lamp indicates that the RTC (ready tone control) F/F is ON (par. 108).
ECLU lamp		When lit, this lamp indicates that the ECRLU (earth curvature correction relay lockup) F/F is ON (par. 111).
HLU lamp		When lit, this lamp indicates that the HRLU (H coordinate relay lockup) F/F is ON (par. 111).
XLU lamp		When lit, this lamp indicates that the XRLU (X coordinate relay lockup) F/F is ON (par. 111).
YLU lamp		When lit, this lamp indicates that the YRLU (Y coordinate relay lockup) F/F is ON (par. 111).
TC lamp		When lit, this lamp indicates that the TC (recycle) F/F is ON (par. 105e).
TENS switch	0 through 5	This switch is used in conjunction with the UNITS switch, the PC switch, and the RECYC switch. The position of the TENS and UNITS switches determines the time slot at which the ring counters stop when the PC switch is down and the RECYC switch is depressed. It also determines the time slot during which voltage will appear at the SYNC test jack (par. 105e).
UNITS switch	0 through 9	Used with the TENS switch as described above.
SYNC (test jack TP1)		This is a test jack connected to the time slot voltage at the time slot indicated by the TENS and UNITS switches. It is used to synchronize an external oscilloscope (not part of the data set) for test purposes.
+4.5V (test jack TP2)		Provides a convenient point for measuring the +4.5-volt bias.
-2.5V (test jack TP3)		Provides a convenient point for measuring the -2.5-volt bias derived from the -20-volt voltage divider.
-20V (test jack TP4)		Provides a convenient point for measuring the -20-volt supply.
CONTINUOUS-REMOTE START switches.	CONTINUOUS REMOTE START	When in the CONTINUOUS position, the transmitter transmits continuously, not stopping between frames (par. 107). In the REMOTE START position, the transmitter sends one complete frame of data and then stops until it is started by a remote start signal.
CDG/TAC-OC switch	CDG/TAC OC	Connects the transmitter for CDG/TAC operation (par. 107). Connects the transmitter for OC operation (par. 107).

Item	Position	Function
PC switch	Up	When the switch is in this position, the clock pulse generator runs continuously (par. 105f).
	Down	When the switch is in this position, the clock pulse generator is stopped, and single pulses can be generated by momentarily depressing the PULSE switch (par. 105f).
IND LP switch	Up	With the switch in the up position, the -70-volt lamp supply is connected to all indicator lamps of the transmitter unit, energizing them when their associated circuits are ON.
	Down	When the switch is in this position, the -70-volt lamp supply is disconnected from all indicator lamps in the transmitter unit.
RECYC switch	Depressed	This switch is used in connection with the TENS and UNITS switches. When the ring counters are stopped by the PC switch, depressing the RECYC switch causes the ring counters to advance to one time slot later than the one indicated by the TENS and UNITS switches (par. 105e).
PULSE switch	Depressed	After the PC switch has been set to the down position, momentarily depressing the PULSE switch advances the ring counters 1 time slot (par. 105f).
AUX switches 1 through 10	Up	There is 1 auxiliary switch for each digit of the auxiliary word. The switch number is the same as the corresponding digit number. In the up position, the digit is a ONE.
	Down	When the switch is in this position, the digit of the corresponding auxiliary word is a ZERO.
P _H switches 1 through 10	Up	These switches add the parallax correction to the H coordinate. When a switch is in the up position, the correction is a ONE for the digit corresponding to the switch number.
	Down	In this position each switch adds a ZERO to the H coordinate parallax for the digit corresponding to the switch position number.
P _X switches 1 through 13	Up	In this position each switch adds a ONE X coordinate parallax digit corresponding to the switch position number.
	Down	In this position each switch adds a ZERO X coordinate parallax digit corresponding to the switch position number.
P _Y switches 1 through 13	Up	In this position each switch adds a ONE Y coordinate parallax digit corresponding to the switch position number.
	Down	In this position each switch adds a ZERO Y coordinate parallax digit corresponding to the switch position number.
BINARY COUNTER indicator lamps 1 through 13.		When lit, these lamps indicate that the binary counter F/F associated with each lamp is ON. These lamps flicker, depending on the value of the coordinate voltage being encoded. Usually the higher numbered lamps flicker the most.
SHIFT REGISTER indicator lamps 1 through 13.		When lit, these lamps indicate that the shift register F/F associated with each lamp is ON. These lamps flicker according to the digits of the auxiliary and coordinate words.
DBL SCALE-SGL SCALE switch.	DBL SCALE	When the switch is in this position, the binary counters start counting at BC 2 instead of BC 1 (par. 124) for operation on a double-scale grid.
	SGL SCALE	When the switch is in this position, the binary counters start counting at BC 1, and the data set operates normally for use with a single-scale grid.



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Figure 9. Coordinate data transmitter unit T-271/TSQ-36, controls.

b. Modulator (Part of the Transmitter Unit) (fig. 10). The following chart lists the controls of the modulator and describes their functions.

Item	Position	Function
1500~ LEV-----	-----	Adjusts the 1,500-cycle oscillator feedback voltage.
600~ LEV-----	-----	Adjusts the 600-cycle oscillator level.
MOD-----	-----	Adjusts the data bias level.

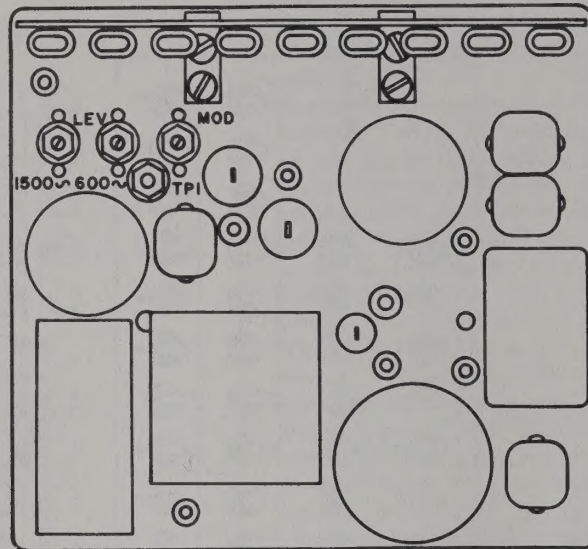
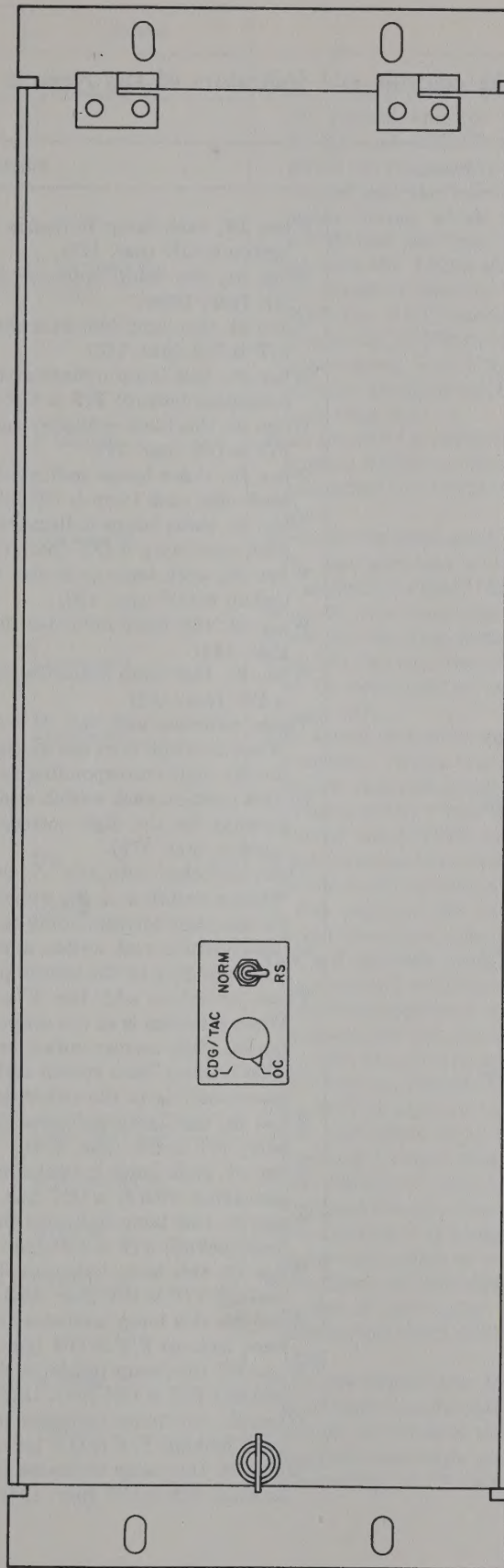


Figure 10. Coordinate data modulator MD-323A/G controls (mounted on back of transmitter unit).

31. Amplifier Synchronizer (fig. 11)

The following chart lists the controls of the amplifier synchronizer and describes their functions.

Item	Position	Function
NORM-RS switch-----	NORM-----	When this switch is in the NORM position, the CDG/TAC-OC switch in the CDG/TAC position, and the CONTINUOUS-REMOTE START switches on the transmitter unit are in the CONTINUOUS position, the transmitter and receiver operate continuously, not stopping between frames.
	RS-----	With the switch in the RS position, the transmitter sends 1 complete frame of data and stops until it is started by a remote start signal (par. 157).
CDG/TAC-OC switch-----	CDG/TAC-----	With the switch in the CDG/TAC position, the input amplifier is connected for internal AGC operation.
	OC-----	With the switch in the OC position, the input amplifier gain is controlled manually.



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Figure 11. Amplifier-synchronizer unit AM-2126/TSQ-36, controls.

32. Receiver Unit

(fig. 12)

The following chart lists the controls and indicators of the receiver unit and describes their functions:

Item	Position	Function
AUX LOCK-UPS lamps		When lit, each lamp indicates that the associated auxiliary lockup is ON (par. 176).
CS lamp		When lit, this lamp indicates that CS (clear storage) F/F is ON (par. 169e).
SPD lamp		When lit, this lamp indicates that the SPD (shift pulse disable) F/F is ON (par. 173).
ECC lamp		When lit, this lamp indicates that the ECC (earth curvature correction lockup) F/F is ON (par. 191).
OSD lamp		When lit, this lamp indicates that the OSD (off scale detection) F/F is ON (par. 177).
UNITS RING lamps 0 through 9.		When lit, these lamps indicate that the units ring F/F associated with each lamp is ON (par. 164).
TENS RING lamps 00, 10, 20, 30, 40, and 50.		When lit, these lamps indicate that the tens ring F/F associated with each lamp is ON (par. 164).
DATA LOCK-UPS lamps 1 through 10.		When lit, each lamp indicates that the associated data relay lockup is ON (par. 180).
TC lamp		When lit, this lamp indicates that the TC (recycle) F/F is ON (par. 161).
MS lamp		When lit, this lamp indicates that the MS (manual start) F/F is ON (par. 163).
P _H switches 1 through 10.	Up	These switches add the H coordinate parallax correction. When a switch is in the up position, the correction is a ONE for the digit corresponding to the switch number (par. 175).
	Down	In this position each switch adds a ZERO to the H coordinate parallax for the digit corresponding to the switch position number (par. 175).
P _X switches 1 through 13.	Up	These switches add the X coordinate parallax correction. When a switch is in the up position, the correction is a ONE for the digit corresponding to the switch number (par. 175).
	Down	In this position each switch adds a ZERO to the X coordinate corresponding to the switch position number (par. 175).
P _Y switches 1 through 13.	Up	These switches add the Y coordinate parallax correction. When a switch is in the up position, the correction is a ONE for the digit corresponding to the switch number (par. 175).
	Down	In this position each switch adds a ZERO to the Y coordinate corresponding to the switch position number (par. 175).
PSR lamp		When lit, this lamp indicates that PSR (parallax storage register) F/F is ON (par. 174).
SHIFT REGISTER lamps 1 through 13.		When lit, each lamp indicates that the SR (shift register) F/F associated with it is ON (par. 174).
STORAGE LOCK-UP HF lamp.		When lit, this lamp indicates that the HF (H coordinate feedback lockup) F/F is ON (par. 190).
STORAGE LOCK-UP HG lamp		When lit, this lamp indicates that the HG (H coordinate grid lockup) F/F is ON (par. 189).
STORAGE LOCK-UP XF lamp		When lit, this lamp indicates that the XF (X coordinate feedback lockup) F/F is ON (par. 191).
STORAGE LOCK-UP XG lamp		When lit, this lamp indicates that the XG (X coordinate grid lockup) F/F is ON (par. 191).
STORAGE LOCK-UP YF lamp		When lit, this lamp indicates that the YF (Y coordinate feedback lockup) F/F is ON (par. 191).
STORAGE LOCK-UP YG lamp		When lit, this lamp indicates that the YG (Y coordinate grid lockup) F/F is ON (par. 191).

Item	Position	Function
TENS switch.....	0 through 5.....	This switch is used in conjunction with the UNITS switch, the PC switch, and the RECY switch. The position of the TENS and UNITS switches determines the time slot at which the ring counters stop when the PC switch is at TEST (down) and the RECY switch is depressed. It also determines during which time slot voltage will appear at the SYNC test jack (par. 161).
UNITS switch.....	0 through 9.....	Used with the TENS switch as described above.
TDC switch.....	1 (up).....	This switch is used in conjunction with the DATA switch. With the DATA switch at TEST, this switch in the 1 position sends a ONE to the serial adder each time a single pulse is generated (par. 172). With the data set in normal operation, a string of ONE's is sent to the serial adder, one for each time slot.
	0 (down).....	With the DATA switch at TEST, this switch in the 0 position sends a ZERO to the serial adder each time a single pulse is generated (par. 172) or a string of ZERO's in normal operation.
MS switch.....	Depressed.....	Momentarily depressing this switch restarts the ring counters for test purposes when no signals are being received from a transmitter (par. 163).
RC 1 lamp.....		When lit, this lamp indicates that RC 1 F/F is ON.
RC 2 lamp.....		When lit, this lamp indicates that RC 2 F/F is ON.
SP switch.....	Depressed.....	With the ring counters stopped this switch causes a single pulse to be generated to advance the ring counters 1 time slot (par. 161).
RECY switch.....	Depressed.....	This switch is used in connection with the UNITS and TENS switches. When the ring counters are stopped by the PC switch, depressing the RECY switch causes the ring counters to advance to 1 time slot later than the one indicated by the TENS and UNITS switches (par. 161).
IND LP switch.....	Up.....	In this position the switch connects the -70-volt lamp supply to the indicator lamps in the receiver unit.
	Down.....	In this position the switch disconnects the -70-volt lamp supply from the indicator lamps in the receiver unit.
SYNC test jack.....		This is a test jack connected to a voltage occurring during the time slot indicated by the TENS and UNITS switches. It is used to synchronize an external oscilloscope (not part of the data set) for test purposes.
+4.5V (TP 2).....		Used with an external meter to measure the +4.5 volts dc.
-20V (TP 3).....		Used with an external meter to measure the -20 volts dc.
-2.5V (TP 4).....		Used with an external meter to measure the -2.5 volts dc.
DBL SCALE-SGL SCALE switch.	DBL SCALE.....	When the switch is in this position, the receiver circuits are arranged for operating with a double-scale grid (par. 178).
	SGL SCALE.....	When the switch is in this position, the receiver circuits are arranged for operation with a single-scale grid (par. 178).
DATA switch.....	NORM.....	When the switch is in this position, data from the receiver input section is applied to the serial adder (par. 172).
	TEST.....	When the switch is in this position, data from the receiver input section is interrupted to allow individual data digits to be sent to the serial adder by means of the TDC switch (par. 172).
PC switch.....	NORM.....	When the switch is in this position, the clock pulse generator runs continuously (par. 161).
	TEST.....	When the switch is in this position, the clock pulse generator is stopped, and single pulses can be generated by momentarily depressing the SP switch (par. 161).

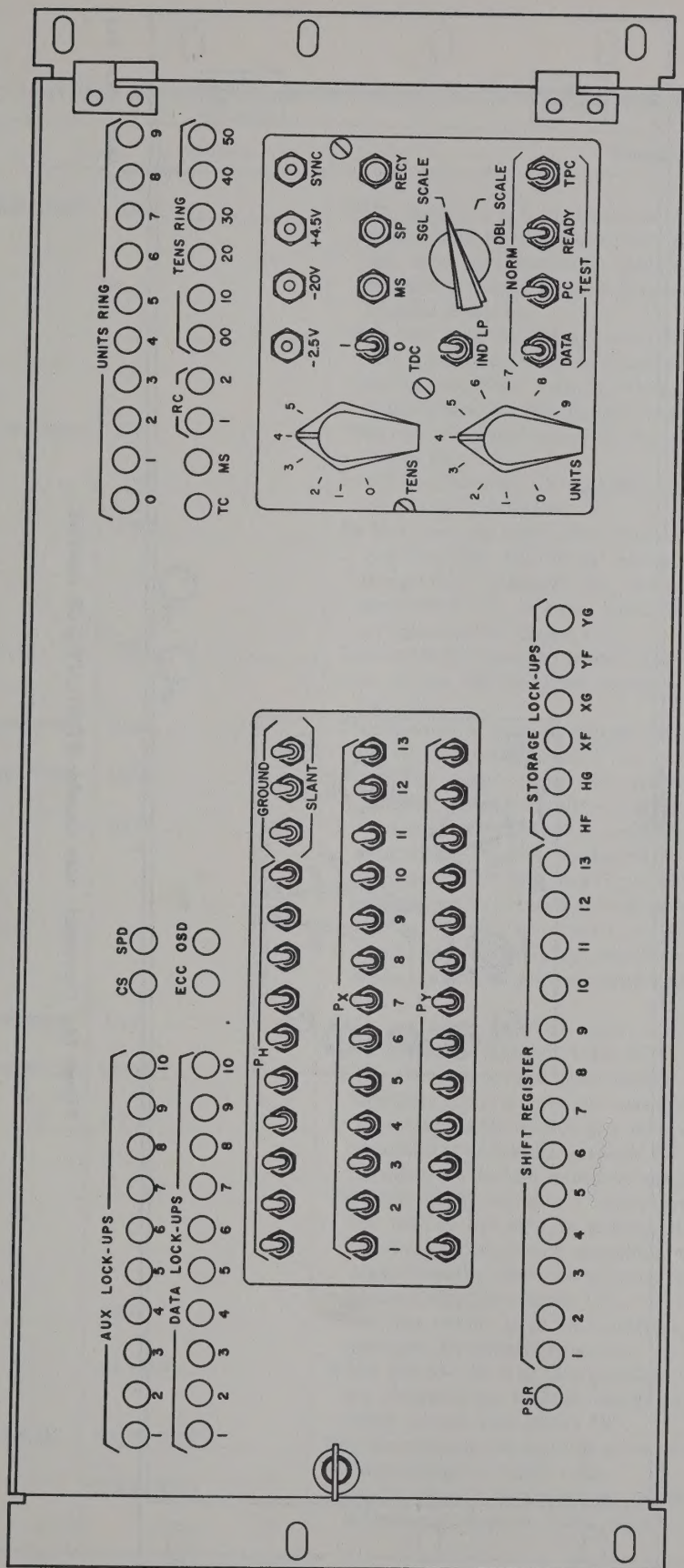
Item	Position	Function
READY switch-----	NORM-----	When the switch is in this position, the reset circuits are controlled by the ready signal from the amplifier synchronizer (par. 142).
	TEST-----	When the switch is in this position, a simulated ready signal is provided by TSG 51 (par. 142).
TPC switch-----	NORM-----	When the switch is in this position, the clock pulses are controlled by the incoming data signals (par. 146).
	TEST-----	When the switch is in this position, the clock pulse generator runs continuously (par. 146).
GROUND-SLANT switches----	GROUND-----	In this position, serial data from the serial adder is applied directly to the shift register.
	SLANT-----	In this position, serial data is applied to auxiliary equipment where it is converted to represent slant range before being applied to the shift register.

33. Decoder

(fig. 13)

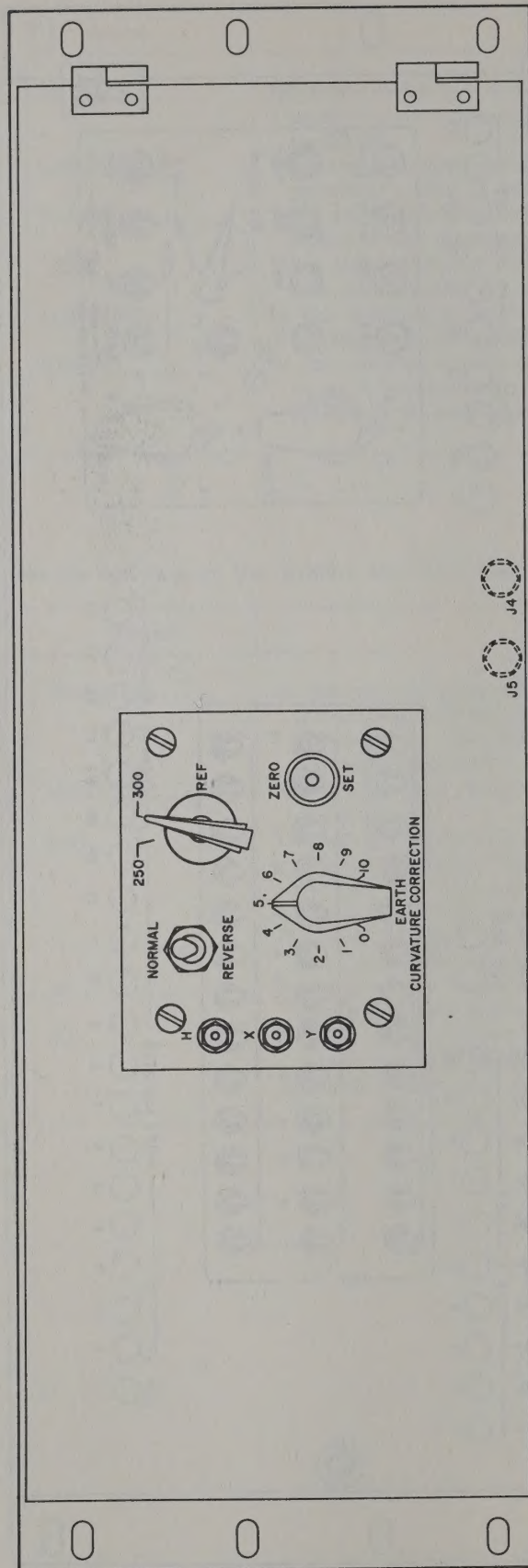
The following chart lists the controls of the decoder and indicates their functions.

Item	Position	Function
NORMAL-REVERSE switch---	NORMAL-----	In this position the switch connects the reference voltage to the decoder to yield normal output (maximum positive for an all ONE data code) when proper reference terminal connections are made.
	REVERSE-----	Reverses the polarity of the reference voltage applied to the decoder.
EARTH CURVATURE CORRECTION knob.	0-10-----	This control adds a small amount of resistance to the feedback network to correct for decoding error due to the earth's curvature. It is normally left at a predetermined setting unless the data set is relocated.
ZERO SET knob-----		This control adjusts the balance of the decoder amplifier for a zero output when the input voltage is zero.
REF switch-----	250-----	Provides proper connections to the decoder network for a system reference voltage of ± 250 volts.
	300-----	Provides proper connections to the decoder network for a system reference voltage of ± 300 volts.
H, X, and Y test points-----		Analog coordinate data output voltage test points.



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Figure 12. Coordinate data receiver unit R-980/TSQ-36, controls.



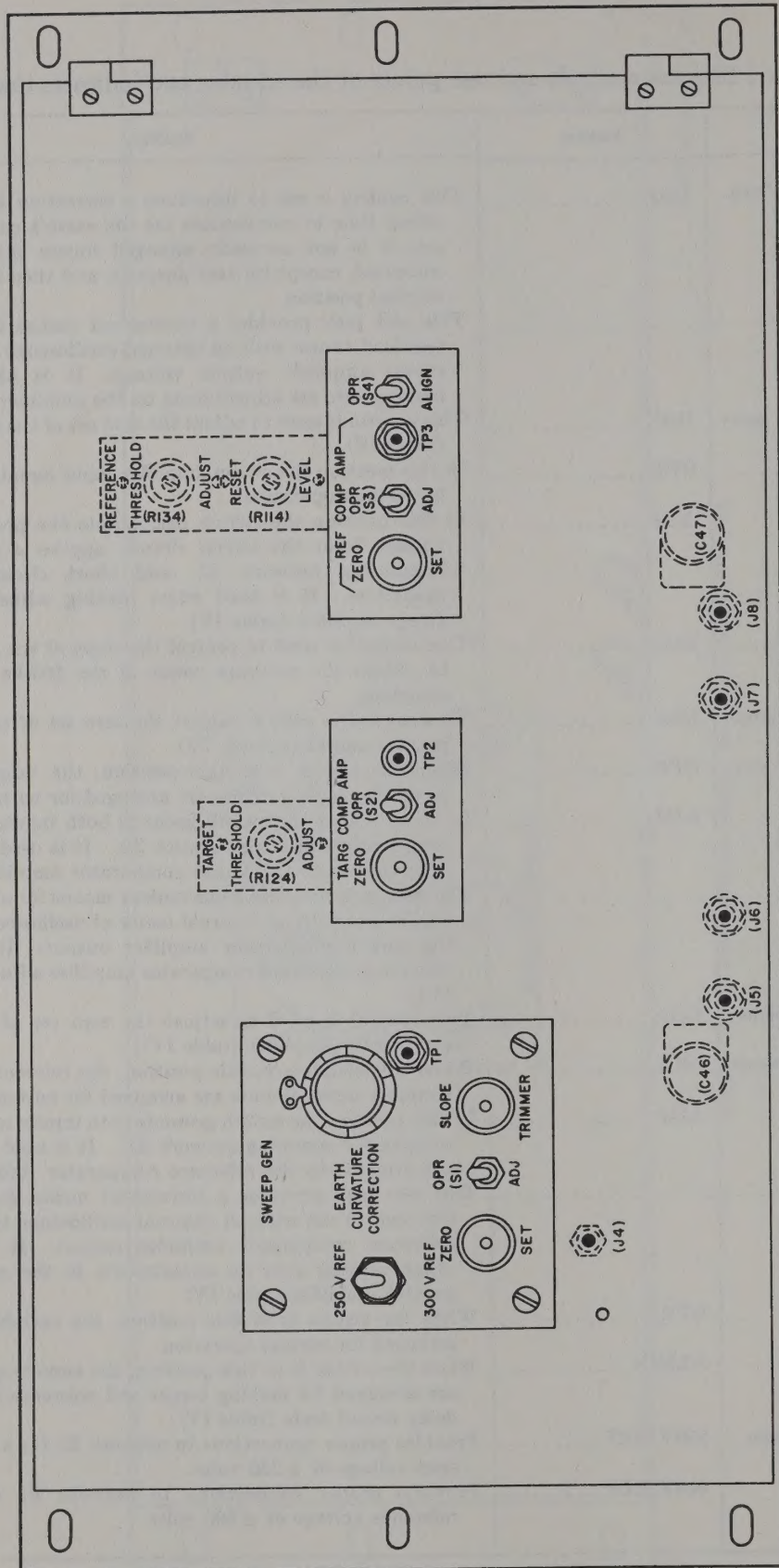
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Figure 13. Coordinate data decoder KY-277/TSQ-36, controls.

34. Encoder (fig. 14)

The following chart lists the controls and test points of the encoder and indicates their functions:

Item	Position	Function
EARTH CURVATURE CORRECTION knob.	Dial	This control is set to introduce a correction in the encoding sweep time to compensate for the earth's curvature. Once set, it is not normally changed unless the equipment is relocated, except for test purposes and then it is reset to its original position.
TP1 test jack		This test jack provides a convenient means for attaching a test lead to use with an external oscilloscope to measure the sweep amplifier output voltage. It is also used when making zero set adjustments on the amplifier (table IV).
ZERO SET knob (sweep generator).	Dial	This control is used to adjust the zero set of the sweep amplifier (table IV).
OPR-ADJ switch (S1)	OPR	In this position the sweep amplifier input circuits are arranged for normal operation.
	ADJ	In this position the switch disconnects the positive reference voltage from the sweep circuit, applies a ground to the integrating network Z1, and short circuits the sweep capacitors. It is used when making adjustments to the sweep amplifier (table IV).
SLOPE TRIMMER knob	Dial	This control is used to control the slope of the sweep in order to obtain the accurate count of the 100-kc pulses during encoding.
ZERO SET knob (target comparator amplifier).	Dial	This control is used to adjust the zero set of the target comparator amplifier (table IV).
OPR-ADJ switch (target comparator amplifier).	OPR	When the switch is in this position, the target comparator amplifier input circuits are arranged for normal operation.
	ADJ	In this position the switch grounds both inputs to the target comparator summing network Z2. It is used when making adjustments to the target comparator amplifier (table IV).
TP2 test jack		This test jack provides a convenient means for attaching a test lead to use with an external meter or oscilloscope to measure the target comparator amplifier output. It is also used when making target comparator amplifier adjustments (table IV).
ZERO SET knob (reference comparator amplifier).	Dial	This control is used to adjust the zero set of the reference comparator amplifier (table IV).
OPR-ADJ switch (reference comparator amplifier).	OPR	When the switch is in this position, the reference comparator amplifier input circuits are arranged for normal operation.
	ADJ	In this position the switch grounds both inputs to the reference comparator summing network Z3. It is used when making adjustments to the reference comparator (table IV).
TP3 test jack		This test jack provides a convenient means for attaching a test lead to use with an external oscilloscope to measure the reference comparator amplifier output. It is also used when making zero set adjustments to the reference comparator amplifier (table IV).
OPR-ALIGN switch	OPR	When the switch is in this position, the encoder circuits are arranged for normal operation.
	ALIGN	When the switch is in this position, the circuits of the encoder are arranged for making target and reference threshold and delay circuit tests (table IV).
250V REF-300V REF switch	250V REF	Provides proper connections to network Z1 for a system reference voltage of ± 250 volts.
	500V REF	Provides proper connections to network Z1 for a system reference voltage of ± 300 volts.



NOTE:

DESIGNATIONS APPEARING IN PARENTHESES () DO NOT
APPEAR AS EQUIPMENT PANEL MARKINGS.

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Figure 14. Coordinate data encoder KY-278/TSQ-36, controls.

35. Low Voltage Power Supply

(fig. 15)

The following chart lists the controls, indicators, and test jacks of the low voltage power supply and describes their functions:

Item	Position	Function
+4.5V & -20V PWR ON lamp		When lit, this lamp indicates the presence of both the +4.5- and -20-volt outputs.
2A FN AC INPUT +4.5 & -20V fuse.		This fuse protects the primary circuit of the +4.5- and -20-volt rectifiers against overload. The fuse is rated at 2 amperes.
1.5A FN AC INPUT LAMP & FIL fuse.		This fuse protects the primary circuits of the lamp supply and unregulated filament supply against overloads. The fuse is rated at 1.5 amperes.
-20V 4A DC OUTPUT fuse		This fuse protects the -20-volt dc output circuits against overloads. The fuse is rated at 4 amperes.
+4.5V 3A DC OUTPUT fuse		This fuse protects the +4.5-volt dc output circuits against overloads. The fuse is rated at 3 amperes.
+20V and -20V DC OUTPUT test jacks.		These jacks provide a convenient means for connecting an external meter to the output of the -20-volt supply.
+4.5V DC OUTPUT and GRD test jacks.		These jacks provide a convenient means for connecting an external meter to the output of the +4.5-volt supply.
+4.5V & -20V SUP ON-OFF switch.	ON	In this position the switch applies primary ac power to the voltage regulator circuit VR1.
	OFF	In this position the switch removes primary ac power from the voltage regulator circuit VR1.
LAMP SUP ADJ VOLTS knob		This control adjusts the output of the -70-volt lamp supply.
LAMP SUP TEST test jack		This jack provides a convenient means for connecting external measuring equipment to the output of the -70-volt supply.

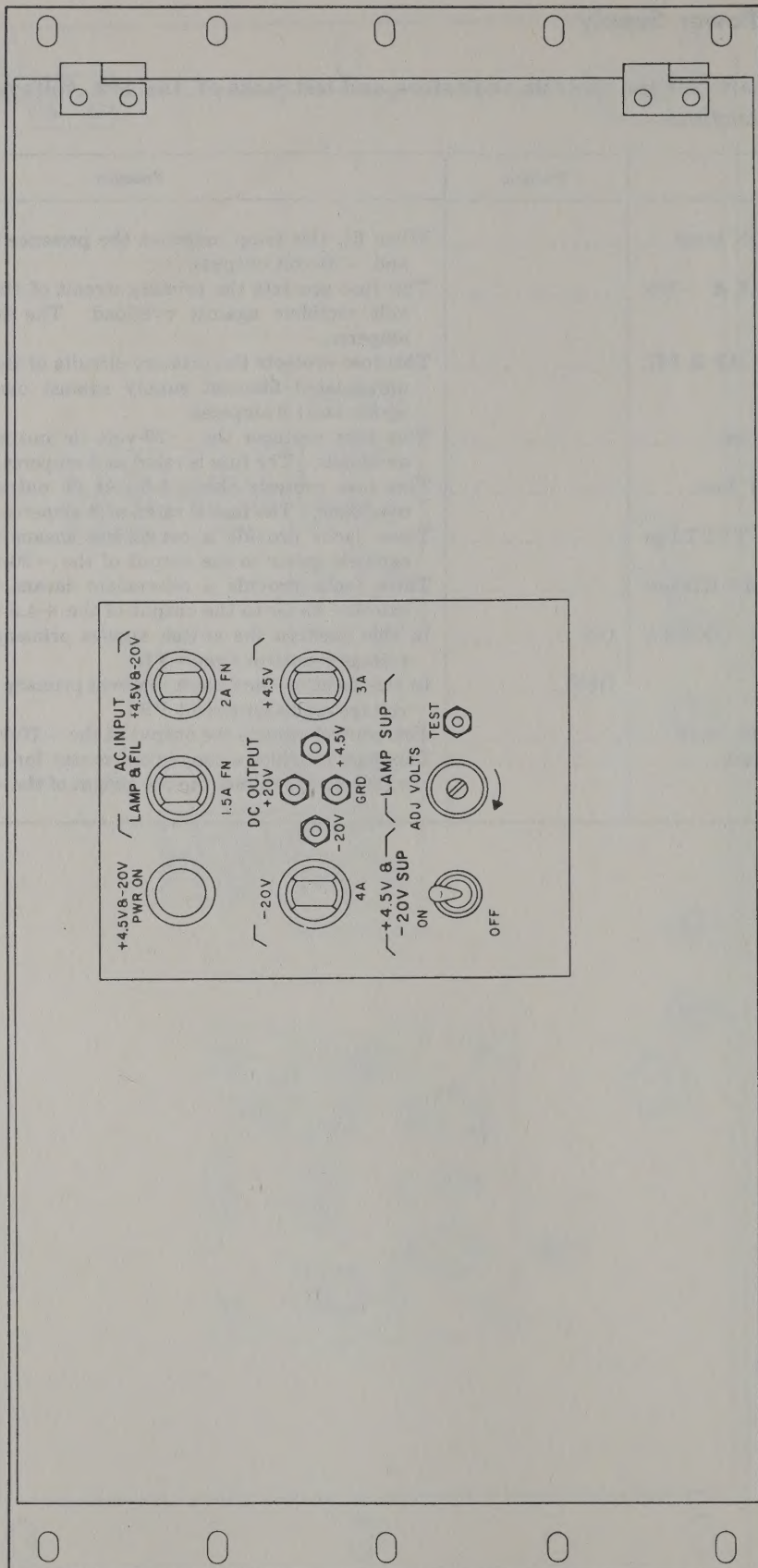


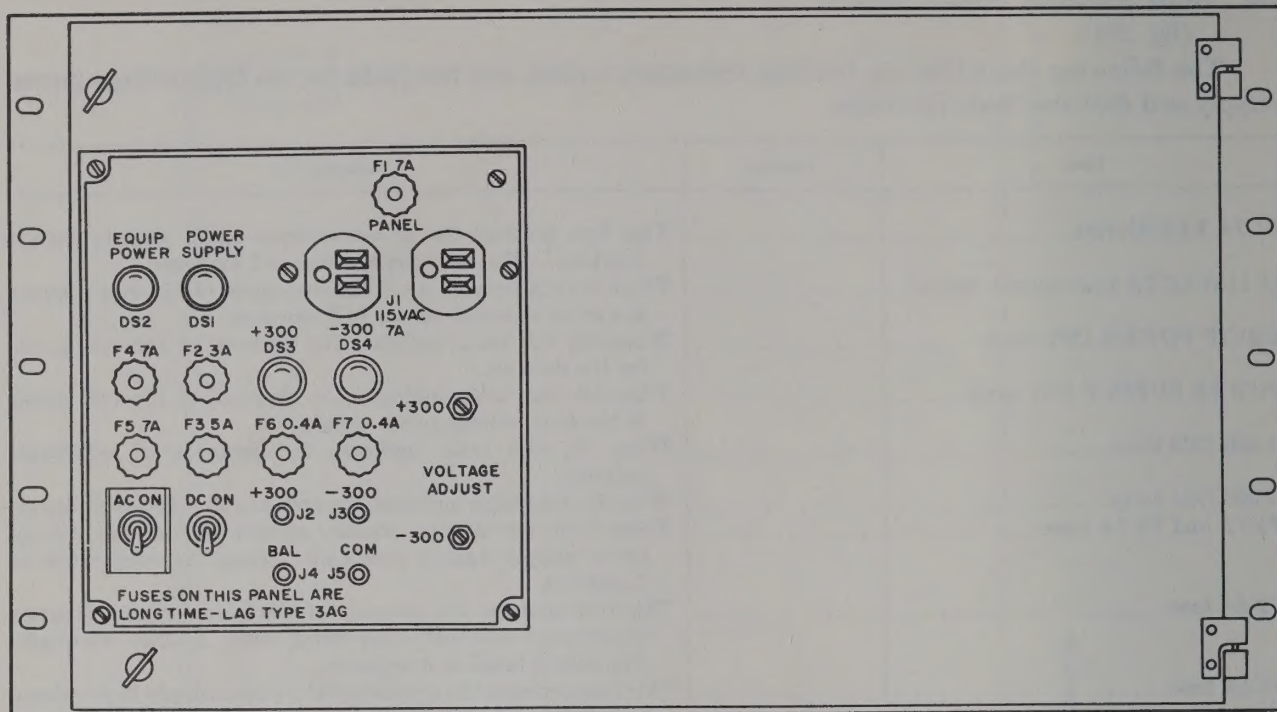
Figure 15. Power supply PP-2235/G, controls.

36. High Voltage Power Supply

(fig. 16)

The following chart lists the controls, indicators, outlets, and test jacks for the high voltage power supply and describes their functions:

Item	Position	Function
F1 7A PANEL fuse.....		This fuse protects the ac convenience outlet circuits against overload. The rating of the fuse is 7 amperes.
J1 115VAC 7A convenience outlets.....		These outlets provide a convenient source of 115-volt primary power for external use up to 7 amperes.
EQUIP POWER DS2 lamp.....		When lit, this lamp indicates the presence of 115-volt power for the data set.
POWER SUPPLY DS1 lamp.....		When lit, this lamp indicates the presence of 115-volt power to the high voltage power supply.
+300 DS3 lamp.....		When lit, this lamp indicates the presence of +300-volt output.
-300 DS4 lamp.....		When lit, this lamp indicates the presence of -300-volt output.
F4 7A and F5 7A fuses.....		These fuses protect the primary circuits of the high voltage power supply against overloads. They are each rated at 7 amperes.
F2 3A fuse.....		This fuse protects the primary of the power supply filament transformer and the time delay relay against overloads. The fuse is rated at 3 amperes.
F3 5A fuse.....		This fuse protects the primary of the power supply high voltage transformer against overload. The fuse is rated at 5 amperes.
F6 0.4A fuse.....		This fuse protects the output of the +300-volt rectifier against overloads. The fuse is rated at .4 ampere.
F7 0.4A fuse.....		This fuse protects the output of the -300-volt rectifier against overloads. The fuse is rated at .4 ampere.
AC ON switch.....	On (up).....	In this position the switch connects 115-volt primary power to the data set.
	Off (down).....	In this position the switch removes 115-volt primary power from the data set except for the convenience outlets.
DC ON switch.....	On (up).....	This switch connects the 115-volt primary power to the high voltage rectifier transformer through a 45-second delay relay.
	Off (down).....	In this position the switch removes 115-volt primary power from the high voltage rectifier transformer.
+300 VOLTAGE ADJUST control.....		This control is used for adjusting the +300-volt output.
-300 VOLTAGE ADJUST control.....		This control is used for adjusting the -300-volt output.
+300 J2 and COM J5 test jacks.....		These jacks provide a convenient means for measuring the +300-volt output.
-300 J3 and COM J5 test jacks.....		These jacks provide a convenient means for measuring the -300-volt output.
BAL J4 and COM J5 test jacks.....		These jacks provide a convenient means for connecting external measuring equipment so that the voltages of the +300- and -300-volt outputs can be balanced with respect to each other.



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Figure 16. Power supply PP-2236/G, controls.

Section II. OPERATION UNDER USUAL CONDITIONS

37. Modes of Operation

(fig. 17)

a. General. The data set is generally used in two locations in the defense area: the CDG/TAC group location and the OC group location. A typical arrangement of an AN/TSQ-36 transmitter and receiver is shown with connecting circuits to associated equipment. The remote start mode of operation is normally used (*b* below) although the continuous mode (*c* below) also may be used. Separate receiving and transmitting lines are used.

b. Remote Start Operation. Upon receipt of a remote start signal, the transmitter sends one complete frame of coordinate and auxiliary data to the remote station. Upon completion of the frame the transmitter remains idle until the next remote start signal is received. The receiver may receive data continuously except when the transmitter is transmitting.

c. Continuous Operation. In continuous operation the transmitter sends continuous frames of data to a remotely located receiver, repeating the

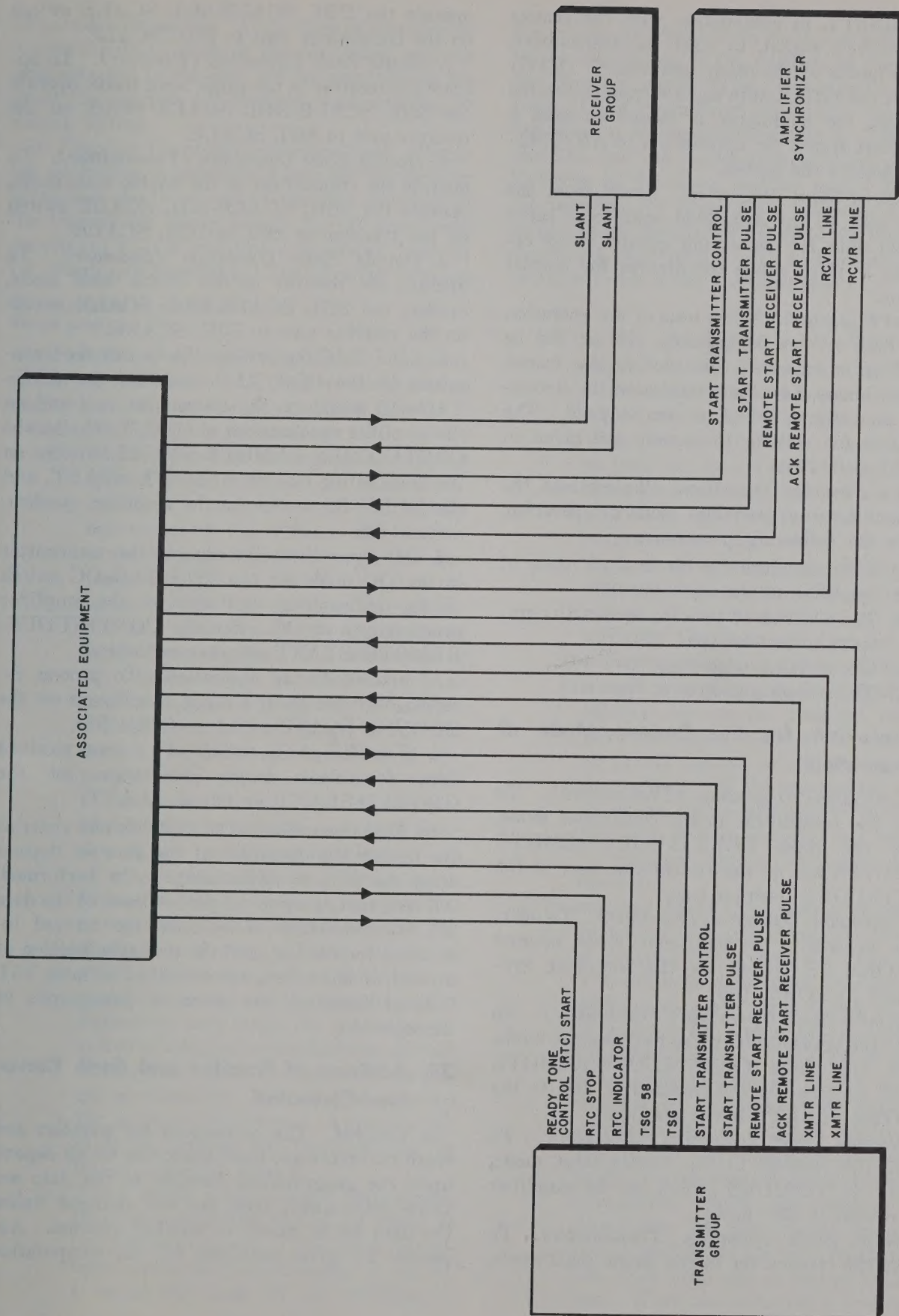
complete frame continuously. The receiver, to which the transmitter is sending, is located at a distance from the transmitter and receives continuously.

d. Single Scale Operation (app. V). In single scale operation the transmitted data is referenced to a single scale coordinate grid. The receiver is set into single scale operation if it is working in a single scale grid area.

e. Double Scale Operation (app. V). In double scale operation the transmitted data is referenced to a double scale grid. The receiver is set into double scale operation if it is working in a double scale grid area.

f. CDG/TAC Operation. The CDG/TAC mode of operation uses the start transmitter control signal (STC) and the start transmitter pulse (STP) and a remote start signal of 600 cycles sent to the amplifier synchronizer. The transmitter is started upon receipt of the remote start signal as described in paragraph 158.

g. OC Operation. The OC mode of operation uses the remote start receiver pulse (RSRP) and the acknowledge remote start receiver pulse



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Figure 17. External control circuits, simplified block diagram.

(ACK RSRP), in conjunction with the remote start 600-cycle signal, to start the transmitter. Also, by means of the ready tone control (RTC) start and the (RTC) stop signals from associated equipment, the modulator is caused to send a remote start signal for application to AN/TSQ-36 data sets in the system.

h. Ground-Slant Operation. Leads from the receiver unit to the associated equipment carry the serial data for converting ground range coordinates to slant range coordinates for normal operation.

i. Test Operation. When tests of the operation of the data set are being made, the set can be stopped at any desired time slot in the frame. Indicator lamps show the condition of the circuits at the time slot at which it was stopped. The procedures for making these tests are given in tables IV and VII.

j. Procedure for Operation. To operate the equipment for any particular mode of operation, perform the following procedures:

- (1) The procedure for the desired mode of operation (*b* through *i* above).
- (2) The addition of parallax and earth curvature correction (par. 39).
- (3) The starting procedure (par. 40).
- (4) The stopping procedure (par. 41).

38. Procedure for the Desired Mode of Operation

a. Continuous Operation (Transmitter). To operate the transmitter in the continuous mode, operate the three CONTINUOUS-REMOTE START switches on the transmitter unit to the CONTINUOUS position (up).

b. Continuous Operation (Receiver). To operate the receiver in the continuous mode, operate the NORM-RS switch on the amplifier synchronizer to NORM (up).

c. Remote Start Operation (Transmitter). To operate the transmitter in the remote start mode, operate the three CONTINUOUS-REMOTE START switches on the transmitter unit to the REMOTE START (down) position.

d. Remote Start Operation (Receiver). To operate the receiver in the remote start mode, operate the NORM-RS switch on the amplifier synchronizer to RS (down).

e. Single Scale Operation (Transmitter). To operate the transmitter in the single scale mode,

operate the DBL SCALE-SGL SCALE switch on the transmitter unit to SGL SCALE.

f. Single Scale Operation (Receiver). To operate the receiver in the single scale mode, operate the SGL SCALE-DBL SCALE switch on the receiver unit to SGL SCALE.

g. Double Scale Operation (Transmitter). To operate the transmitter in the double scale mode, operate the DBL SCALE-SGL SCALE switch on the transmitter unit to DBL SCALE.

h. Double Scale Operation (Receiver). To operate the receiver in the double scale mode, operate the SGL SCALE-DBL SCALE switch on the receiver unit to DBL SCALE.

i. CDG/TAC Operation. To operate the transmitter in the CDG/TAC mode set the CDG-TAC-OC switch on the transmitter unit and on the amplifier synchronizer at CDG/TAC. Set the CONTINUOUS-REMOTE START switches on the transmitter unit at REMOTE START, and the NORM-RS switch on the amplifier synchronizer at RS.

j. OC Operation. To operate the transmitter in the OC mode set the CDG/TAC-OC switch on the transmitter unit and on the amplifier synchronizer at OC. Set the CONTINUOUS-REMOTE START switches as desired.

k. Ground Range Operation. To process received data for ground range coordinates set the GROUND-SLANT switch at GROUND.

l. Slant Range Operation. To process received data for slant range coordinates set the GROUND-SLANT switch at SLANT.

m. Test Operation. The switches and controls for testing the operation of the data set depend upon the tests or adjustments to be performed. All tests to determine the performance of the data set, the procedure to be used, the normal indication for the test, and the probable location of a fault, if one exists, are described in table VII. Control functions are given in paragraphs 28 through 36.

39. Addition of Parallax and Earth Curvature Correction

a. General. The corrections for parallax and earth curvature are fixed quantities which depend upon the geographical location of the data set. Once determined, they are not changed unless the data set is moved to another location. Appendix IV gives examples for the computation

of parallax quantities. At the time of installation a note should be made of the correction, and the note attached to the data set for reference in the event the controls are changed inadvertently, or during testing.

b. Parallax Correction (Transmitter). Parallax correction is introduced into the transmitter by setting the three sets of parallax switches on the transmitter group panel: P_H (H coordinate parallax); P_X (X coordinate parallax); and P_Y (Y coordinate parallax). The parallax switches

Binary number H coordinate-----	0	1	1	0	1	1	0	1	0	1
Switch position-----	down	up	up	down	up	up	down	up	down	up

c. Parallax Correction (Receiver). Parallax correction is added to the receiver in the same manner as in the transmitter (*a* and *b* above).

d. Earth Curvature Correction.

- (1) The nature of the stereographic mapping system (used in data set data transmission) is such that the relationship between earth arc distance and its corresponding stereographic projection distance is not linear. In addition, because of the fact that the stereographic projection is a distortion of the magnitude of earth distances, there is a distortion in the transformation of coordinates from one stereographic projection to another stereographic projection. It is for this reason that data transformed from one projection to another must be corrected to compensate for distortion. The amount of correction required is a complex function of the transformation distance and of the target coordinate. If the transformation distance is small, no correction is required. If the transformation distance is moderate, a linear correction, which is a function only of this distance, may be employed. If the transformation distance is very large, the correction required is a higher order function of both the transformation distance and the target coordination. The data set provides for a linear correction. Appendix IV gives the formula (9) for obtaining the linear correction term A .
- (2) For a single point-to-point transformation, the correction should be made at the transmitter only. The earth curvature correction potentiometer is set at a value 400 times A . In addition, a

are numbered from left to right, the switch number corresponding to the position of the digit of the parallax word. The *least* significant digit (app. I) is represented by switch position 1. Switches in the up position add a ONE to the parallax for the corresponding digit positions. Switches in the down position add a ZERO to the parallax for those digit positions. For example, an H parallax word of 0110110101 (least significant digit to the left) will require the P_H switches to be in the positions shown.

digital earth curvature correction of value (-510 times A) quanta must be added to the digital parallax correction.

- (3) The question of double transformation, at both the transmitter and the receiver, is complex and is not covered here. There is a case, however, for which a simple correction can be made at the receiver. Suppose that data is transmitted to a rather distant central point, using a correction at the transmitter as just described. The data will then be correct with respect to that distant point. Suppose it is now sent back, digitally, to a location not too far removed from the point of origin. Here, a correction term of $(1-A)$ instead of $(1+A)$ is used in the receiver. If the transmitter and receiver are within 200 miles of each other, the data will be in error by less than $\frac{1}{2}$ quantum, and no correction will be necessary.

e. Transmitter Earth Curvature Correction.

- (1) Provision for earth curvature correction is included in the data set. The X and Y coordinate data to be transmitted is modified by a correction factor, A , which is inserted by means of the EARTH CURVATURE CORRECTION dial on the encoder and the P_X and P_Y parallax switches on the transmitter unit. The correction factor, A , is a second order function of the separation distance between the transmitter and receiver, plus a constant. Since the value of A is determined by the overall system, of which the data set is a part, this information must originate at higher headquarters. When the value of A is obtained,

the EARTH CURVATURE CORRECTION control on the encoder is set at a dial reading of 400 times A. As an example, for a value of A equal to .007 (approximate maximum value), the corresponding dial setting is—

$$400 \times .007 = 2.8$$

The corresponding digital correction to be added to the parallax-correction word is equal to -510 times A (in quanta). As an example, for a value of A equal to .007, the corresponding digital correction to be added is—

$$-510 \times .007 = -3.57 \text{ quanta.}$$

f. Receiver Earth Curvature Correction. Provision also is furnished for modifying the received coordinate data (in the receiver) by a correction factor, B. The correction factor, B, is a function of the separation distance between the original transmitter and final receiver, and of any intermediate transformation correction which may have been made. It is also determined by the overall system, of which the data set is a part, and similarly must originate at higher headquarters. When the value of B is obtained, the EARTH CURVATURE CORRECTION control on the decoder panel is set at one of the following dial readings, depending upon the wiring option being used for the particular equipment.

Wiring option A, dial reading = $500 \times B$

Wiring option B, dial reading = $1000 \times B$

Wiring option C, dial reading = $1200 \times B$

As an example, for a value of B equal to .006 and wiring option A in use, the dial setting is—

$$500 \times .006 = 3.00$$

A mathematical treatment of earth curvature correction is included in appendix V.

g. Auxiliary Data.

- (1) The data set has provision for the transmission of auxiliary data along with the H, X, and Y coordinate data. The auxiliary data may be any information which can be expressed by 10 binary bits. (The word bit is derived from the two words binary digit.) The 10-bit binary word may be set in either by means of the 10 auxiliary switches on the transmitter unit, or by associated equipment at a remote location. If the auxiliary switches on the transmitter unit are to be used, P3 (part of the transmitter) should be connected to J2 on the

transmitter panel, and P2 should be connected to J3. If associated equipment is to be used to set in auxiliary data, P3 should be connected to J3, and P2 to J2. The auxiliary data from the associated equipment is connected to terminals 1 through 10 of P18A-1-10 (see connections, par. 19).

- (2) Outgoing auxiliary data is supplied in the form of 10 open or closed relay circuits. These circuits are accessible at terminals 11 through 20 of P18A-11-20. Since the circuits are completed to the auxiliary common lead through reed relay contacts, there is a limitation on the current and voltage that may safely be employed on these contacts. Inductive loads (such as relay windings) must not exceed .5 ampere and the contacts must be protected against arcing. A protective network consisting of a .1-microfarad capacitor in series with a 500-ohm resistor connected across each contact will reduce contact arcing to a minimum. (Such a network is not furnished as part of the data set; see fig. 18 for a suggested network.) The voltage rating of the capacitor should not be less than 600 vdw. Noninductive or carbon lamp loads need no protective networks. If

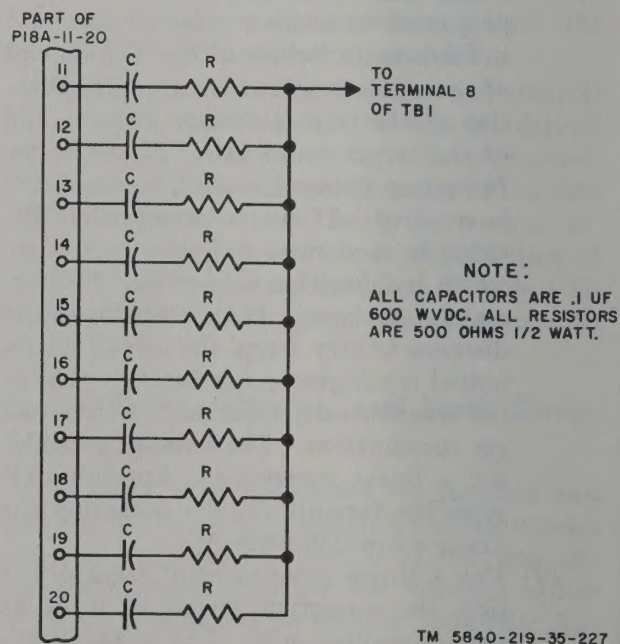


Figure 18. Auxiliary data relay contact, arc suppressor circuit, schematic.

the contacts are to operate tungsten lamps, whose cold resistance may be very low, it is recommended that 24-volt lamps be used in a 50-volt circuit with an appropriate value of dropping resistance in series.

40. Starting Procedure

To start the data set, perform the following operations:

a. Set the controls as indicated in table III.

b. *Partial Shutdown (± 300 Volts).* The ± 300 -volt power supply to the on position (up). With these switches on, all power will be applied to the equipment as soon as the thermal delay switch in the high voltage power supply operates (about 45 seconds).

41. Stopping Procedure

a. *Complete Shutdown.* To turn off all power to the data set except convenience outlets, set

the AC ON switch on the high voltage power supply to the off position (down). To remove power from the convenience outlets shut off the power at the source.

b. *Partial Shutdown (± 300 Volts).* The ± 300 -volt outputs of the high voltage power supply can be shut off, if desired, by operating the DC ON switch in the high voltage power supply to the off position (down). This does not affect the thermal delay switch in the high voltage power supply and the ± 300 volts can be turned back on without delay.

c. *Partial Shutdown ± 4.5 Volts and -20 Volts).* The $+4.5$ -volt and -20 -volt output of the low voltage power supply can be shut off, if desired, by operating the $+4.5V$ & $-20V$ SUP switch on the panel of the low voltage power supply to OFF. This supply can be turned back on without delay from the thermal delay switch in the high voltage power supply.

CHAPTER 4

PREVENTIVE MAINTENANCE

Section I. TOOLS AND EQUIPMENT

42. Tools and Materials Supplied With Equipment

No standard issue tools, materials, or tool equipment kits are supplied with the data set. Sufficient tools for organizational maintenance are supplied with associated equipment and should be used when needed.

43. Special Tools Issued for Equipment

No special tools are furnished with the data set. Tools required for making interconnections (par. 15) are furnished with the associated equipment. Instructions for their use are listed in paragraph 19c.

44. Special Materials Issued for Equipment

The following special materials are supplied with the data set:

- 1 SM-D-130326 Cable Assembly, Special Purpose, Electrical (fig. 160)
- 1 SM-C-130330 Adapter, Test, Electrical (fig. 161)
- 1 SM-C-130333 Adapter, Test, Electrical (fig. 161)

The cable assembly is used for testing the modulator components during equipment operation with the modulator removed from the data transmitter. The two test adapters are used for testing and troubleshooting on the printed circuit packages during equipment operation. Refer to paragraph 198c for details on their use.

Section II. PREVENTIVE MAINTENANCE SERVICES

45. Definition of Preventive Maintenance

Preventive maintenance is work performed on equipment (usually when the equipment is not in use) to keep it in good working order so that breakdowns and needless interruptions in service will be kept to a minimum. Preventive maintenance differs from troubleshooting and repair since its object is to prevent troubles from occurring.

46. Use of DA Form 11-238

Warning: Prior approval must be obtained to shut down equipment which is working on a 24-hour basis. Disconnect all power from the data set before performing the operations listed on DA Form 11-238. When maintenance is completed, reconnect the power and check the data set for satisfactory operation by performing the test listed in paragraph 48.

DA Form 11-238 (fig. 19(1) and 19(2)) is a preventive maintenance checklist to be used by the unit repairman. Items not applicable to the equipment are lined out in the figures. References in the Item block in the figures are to paragraphs which contain additional information pertinent to the particular item. Instructions for the use of the form appear on the front of the form.

47. Visual Inspection

Inspect the equipment periodically for the following:

- a. Connections to terminal boards for loose or otherwise poor contact.
- b. Loose connectors, loose terminal board connections, and damaged cables.
- c. Plug-in packages, components, and electron tubes for poor seating.
- d. Ceramic and plastic parts for breakage.
- e. Electron tubes for heater glow.

ADDITIONAL ITEMS FOR 2D AND 3D ECHELON INSPECTIONS		CONDITION
26. INSPECT ANTENNA FOR CORRUPTIONS, CORROSION, LOOSE FIT, DAMAGED INSULATORS AND RE-SELECTORS.		
27. CHECK FOR NORMAL OPERATION.		✓
28. SECURE SHIPBOARD OR SHOREMOUNT REMOVE BATTERIES		

MAINTENANCE CHECK LIST FOR SIGNAL EQUIPMENT SOUND EQUIPMENT, RADIO, DIRECTION FINDING RADAR, CARRIER, RADIOSONDE AND TELEVISION (AR 750-623)																														
EQUIPMENT NOMENCLATURE Coordinate Data Set AN/TSQ-8																														
EQUIPMENT SERIAL NUMBER 0001																														
INSTRUCTIONS This form may be used for a period of one month by using the correct dates and weeks of the month. It is to be used as a Preventive Maintenance check list for Signal equipment in actual use, or for a check on equipment prior to issue. - For detailed Preventive Maintenance instructions see: - The Technical Manual (in TM 11 series) for the equipment. (See DA Pamphlet Number 310-4) - The Supply Bulletin (SB 11-100 series) for the equipment. (See DA Pamphlet Number 310-4) - The Department of the Army Lubrication Order. (See DA Pamphlet Number 310-4) - The following action will be taken by either the Communications Officer/Chief for 1st echelon, or the Inspector for higher echelon: - Enter Equipment Nomenclature and Serial Number. - Strike out items that do not apply to the equipment. - Operator/Inspector will enter in the columns entitled CONDITION, on the proper line, a notation regarding the condition, using symbols specified under LEGEND. - After operator completes each daily inspection he will initial over the appropriate dates under "Daily Condition for Month", then return form to his supervisor.																														
TYPE OF INSPECTION <table border="1"> <thead> <tr> <th>OPER- ATOR</th> <th>2/3 ECH- ELON</th> <th>DATE</th> <th>SIGNATURE</th> </tr> </thead> <tbody> <tr> <td>✓</td> <td></td> <td>7 Dec.</td> <td>Jack Ludwig</td> </tr> <tr><td></td><td></td><td></td><td></td></tr> <tr><td></td><td></td><td></td><td></td></tr> <tr><td></td><td></td><td></td><td></td></tr> <tr><td></td><td></td><td></td><td></td></tr> <tr><td></td><td></td><td></td><td></td></tr> </tbody> </table>			OPER- ATOR	2/3 ECH- ELON	DATE	SIGNATURE	✓		7 Dec.	Jack Ludwig																				
OPER- ATOR	2/3 ECH- ELON	DATE	SIGNATURE																											
✓		7 Dec.	Jack Ludwig																											

REPLACES DA FORMS 11-238, 1 NOV 55; 11-238, 11-244, 11-245, 11-248, 11-249, 11-250, AND 11-251; WHICH ARE OBSOLETE.

DA FORM 11-238
1 MAY 57

4

Figure 19. DA Form 11-238.

TM 5840-219-35-230 ①

LEGEND for marking conditions: Satisfactory, ✓. Adjustment, Repair or Replacement required, X. Defect corrected, (X).		DAILY CONDITION FOR MONTH OF December 1957																											
NO.	DAILY ITEM	CONDITION EACH WEEK							2D ECH	CONDITION																			
		1ST	2D	3D	4TH	5TH	6TH	7TH																					
1.	COMPLETENESS AND GENERAL CONDITION OF EQUIPMENT. (Transmitter, receiver, carrying case, wire, cables, microphones, tubes, spare parts, technical manuals).																												
2.	GROUNDING AND MOISTURE PROTECTION. MICROPHONE HEADSETS, TEST JACKS, AUDIO COMMUNICATION PANELS.																												
3.	INSPECT EQUIPMENT FOR NORMAL OPERATION. INSPECT FOR EVIDENCE OF CUT-OUT FROM LOOSE CONTACTS.																												
4.	CHECK FOR NORMAL OPERATION OF EQUIPMENT. BE ALERT FOR UNUSUAL OPERATION OR CONDITION.																												
WEEKLY										ADDITIONAL ITEMS FOR 2D AND 3D ECHELON INSPECTIONS																		CONDITION	
5.	CLEAN AND TIGHTEN EXTERIORS OF CASES, RACKS, MOUNTS. TRANSMITTERS. PAR. 14	✓								15. INSPECT EXTERIORS OF RECEIVERS. TRANSMITTERS. MICROPHONE HEADSETS. TEST JACKS. AUDIO COMMUNICATION PANELS.																			
6.	INSPECT CASES, MOUNTS, ANTENNA HOUSINGS AND EXPOSED METAL SURFACES FOR RUST, CORROSION.	✓								16. INSPECT RELAYS AND SWITCHES. OPERATORS FOR LOOSE TERMINALS. INSPECT CONTACTS. INSPECT TERMINALS. INSPECT CASES AND SPRINGS. PROPER SPRING TENSION.																			
7.	INSPECT CORDS, CABLE, WIRE. SHOCK MOUNTS FOR CUTS, KINKS, BREAKS, FRAYING, UNDUE STRAIN. PAR. 14	✓								17. INSPECT VARIABLE CAPACITORS FOR DIRT, MIS-ALIGNMENTS OF PLATES. LOOSE MOUNTINGS. MOISTURE.																			
8.	CHECK ANTENNA SWITCHES FOR PROPER TENSION OR DAMAGE.									18. INSPECT RESISTORS, BUSHINGS AND INSULATORS FOR CRACKS, CHIPPING, BLISTERING, MOISTURE, DISCOLORATION.	✓																		
9.	INSPECT CABLES AND LEATHER TIES FOR MOISTURE, TEARS, FRAYING.									19. CLEAN AND TIGHTEN SWITCHES, TERMINAL BLOCKS, BLOWERS, RELAY CASES AND INTERIORS OF CHASSIS AND CABINETS NOT READILY ACCESSIBLE.	✓																		
10.	INSPECT ACCESSIBLE ITEMS FOR LOOSE NUTS, SWITCHES, KNOBS, JACKS, CONNECTORS, RELAYS, TRANSFORMERS, MOTOR-DRIVEN BLOWERS, ETC.	✓								20. INSPECT TERMINAL BLOCKS FOR LOOSE CONNECTIONS, CRACKS AND BREAKS. PAR. 9	✓																		
11.	CLEAN AND/OR INSPECT AIR FILTERS, BRASS NAME PLATES, AND METER WINDOWS.	✓								21. INSPECT TERMINALS OF LARGE FIXED CAPACITORS AND RESISTORS FOR DIRT, CORROSION, LOOSE CONTACTS.	✓																		
12.	INSPECT STORAGE BATTERIES FOR DIRT, LOOSE TERMINALS, SPECIFIC GRAVITY, DAMAGED CASES. INSPECT DRY BATTERIES FOR LEAKAGE.									22. INSPECT TRANSFORMERS, CHOKES, POTENTIOMETERS AND RESISTORS FOR OVERHEATING AND OIL LEAKAGE.	✓																		
ADDITIONAL ITEMS FOR 2D AND 3D ECHELON INSPECTIONS										CONDITION																			
13.	INSPECT SHELVES AND COVERS FOR ADEQUACY OF WEATHER-PROOFING. TEARS, FRAYING.									23. INSPECT GENERATORS. MICROPHONES. BATTERIES FOR BURNING. SPRING TENSION. WEAR AND FITTING OF COMMUTATOR.																			
14.	CHECK EQUIPMENT BOX COVERS FOR CRACKS, BURN, WEAR, DAMAGED SHELVES, CASES.									24. INSPECT CATHODE RAY TUBES FOR BURNING. SCREENS. ETC.																			
										25. INSPECT WATERPROOF CASES FOR CRACKS. WEAR AND FITTING OF COMMUTATOR.																			

CONTINUED ON PAGE 4

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GPO 1957 O-47034

Figure 19—Continued.

TM5840-219-35-230 (2)

f. Resistors and power transformers for overheating; look for charred resistors, feel transformers cases for excessive temperature rise, smell for burning odor.

g. Signs of arcing.

h. Fuses for burnout or corrosion.

i. Foreign material shorting terminals or wiring.

48. Equipment Performance Checklist

The equipment performance checklist provides a rapid means of checking for normal operation

of the data set during preventive maintenance operations. Operate the equipment as directed in the checklist. Check for the normal indication listed in the operation column, and, if an abnormal indication is obtained check the remarks column. For troubleshooting, refer to the equipment maintenance procedures outlined in chapter 9.

Note. Prior approval must be obtained to shut down equipment working on a 24-hour basis.

Caution: Before attempting to replace any tubes, lamps, or fuses, refer to paragraph 195.

Table V. Equipment Performance Checklist

Equipment	Operation	Remarks
1. High voltage and low voltage power supplies.	a. Set all switches on the high voltage and low voltage power supplies to the off position (down). b. On the high voltage power supply (fig. 16) set the AC ON switch to on (up). The EQUIP POWER DS2 and POWER SUPPLY DS1 lamps should light. All electron tube heaters in the power supply should light. c. On the low voltage power supply (fig. 15) set the +4.5V & -20V SUP ON-OFF switch to ON. The +4.5V & -20V PWR ON lamp should light. d. On the high voltage power supply set the DC ON switch to on (up). The +300 DS3 and -300 DS4 lamps should light if 45 seconds have elapsed since the AC ON switch was turned on.	If indicator lamps and tube heaters do not light, check fuses F2, F4, and F5. If lamps light but all heaters do not light, check the individual tubes. If the tubes light but lamps do not light, replace the lamps. Check for open fuses as indicated by associated neon lamps.
2. Supply voltages-----	e. On the high voltage power supply check for the presence of 115 volts ac at the convenience outlets, using the VTVM(ac). a. On the test panel check the dc supply voltages by setting the meter switch at +300V, +150V, +75V, -20V, +4.5B, and -300V in turn. The meter should indicate the voltages. b. On the test panel set the ENC REF and DEC REF switches to INT. Check the dc reference voltages by setting the meter switch at +REF and -REF, in turn. The meter should indicate the voltages. c. Set the ENC REF and DEC REF switches at EXT and set the meter switch at +REF and -REF, in turn. The meter should indicate the voltages.	Check fuses F3, F6, and F7 if lamps do not light. If fuses are good and lamps do not light, replace the lamps. If the lamps are good, check tubes V9, V10, V11, and V12 (fig. 134(4)). If the tubes are good, replace time delay relay K1. If no voltage is present, check fuse F1.

Table V. *Equipment Performance Checklist—Continued*

Equipment	Operation	Remarks
3. Overall operation of transmitter and receiver (single scale).	a. Connect the transmitter and receiver back-to-back by operating REC LINE switch on the test panel to LOCAL. b. Set the CONTINUOUS-REMOTE START switches on the transmitter unit at CONTINUOUS. Set the NORM-RS switch on the amplifier synchronizer at NORM. c. Set CDG/TAC-OC switch at CDG/TAC. d. Set the DBL SCALE-SGL SCALE switch on the transmitter unit at SGL SCALE. Set the SGL SCALE-DBL SCALE switch on the receiver unit at SGL SCALE. e. Set the XMTR AT (db) control on the transmitter unit at 10. f. Set the EARTH CURVATURE CORRECTION controls on the encoder and decoder at zero. g. Set all test switches (par. 28 through 36) at their normal positions, and set IND LP switch on the transmitter unit and receiver unit to on (up). h. Using the VTVM (dc), measure the H, X, and Y coordinate target voltage from terminals J2-1, 2, and 3 (fig. 140(1)) of the transmitter unit to ground. If voltage is present, disconnect the target voltages by removing the pins from terminals 15, 16, and 17 of P18C on the cabinet (fig. 7). Ground terminal 3 of Z2 of the encoder with a clip lead. i. Set all parallax switches on the transmitter unit and receiver unit at 0 (down). Start the data set by setting the AC ON switch on the high voltage power supply to on (up). j. Using the VTVM (dc) or an oscilloscope, measure the H, X, and Y coordinate output voltages at the decoder at TP1, TP2, and TP3 in turn. The voltage at each point should be 0 ± 2. k. Set the H, X, and Y parallax code of 1010101010 into the transmitter by operating the odd-numbered switches on the transmitter unit up and the even-numbered switches down. l. Determine the complement of the code 1010101010 (app. I). Set in the H, X, and Y parallax complement code into the receiver using the H, X, and Y parallax switches (1010101010). Check that the H, X, and Y coordinate output voltages are still 0 ± 2. This tests for single scale operation.	Neon indicator lamps will light for those circuits that are operating. If no lamps light, check LAMP SUP ADJ VOLTS on the low voltage power supply (table IV, step 2). This is half-scale, or zero output voltage.

Table V. Equipment Performance Checklist—Continued

Equipment	Operation	Remarks
4. Overall operation of transmitter and receiver (double scale).	a. Set up the transmitter and receiver back-to-back as described in step 3. b. Set all switches as in step 3 except: set the DBL SCALE-SGL SCALE switch on the transmitter unit at DBL SCALE, and set the 3 SGL SCALE-DBL SCALE switches on the receiver group panel unit at DBL SCALE. c. Ground the encoder input (step 3h above). Set all parallax switches down. d. Using the VTVM (dc) or an oscilloscope, measure the H, X, and Y output voltages at the decoder (step 3j above). The voltages should be 0 ± 2. e. Set the H, X, and Y parallax code of 1010101010 into the transmitter. f. Determine the complement of the code 1010101010 (app. I). Set in the H, X, and Y complement code into the receiver, using the H, X, and Y parallax switches moved 1 digit to the right (1101010101). The output voltage at each coordinate output should be 0 ± 2.	
5. Overall operation using separate transmitter and receiver.	a. The tests described in steps 3 and 4 can be made with a transmitter and receiver which are separated geographically but are connected together by a wire line. b. Make line level adjustments at both the transmitter and receiver (par. 26). c. Perform steps 3b, c, d, g, h, i, j, and k or 4b, c, d, e, and f.	
6. Remote start-----	a. Set up the transmitter and receiver back-to-back as in step 3. Set the AC ON switch on (up). b. Connect the oscilloscope to TP4 and ground of the test panel. c. Synchronize the oscilloscope at the SYNC on the transmitter unit to observe a complete frame. d. Set the CONTINUOUS-REMOTE START switches on the transmitter unit at REMOTE START and set the NORM-RS switch on the amplifier synchronizer at RS. e. Arrange to have the associated equipment send RTC start and RTC stop signals. Observe that the transmitter sends 1 complete frame and then stops.	

CHAPTER 5

THEORY—BASIC SYSTEM

Section I. GENERAL

49. General

a. Coordinate Data Set AN/TSQ-36 is used to send and receive positional information between remote points connected by standard telephone circuits. The positional information handled by the data set is received from associated equipment over three leads in the form of dc analog voltages which correspond to the values of the coordinates to be transmitted. These analog voltages are converted to binary numbers transmitted as sequential pulses of 1,500-cycle tone to the distant point over a standard telephone circuit. At the receiver, the pulses of each coordinate binary number are decoded and distributed sequentially as coordinate analog voltages to three separate output leads representing the three coordinates originally presented to the transmitter. To establish a uniform reference for the utilization of the data received from the transmitters at different locations, parallax corrections may be manually set in and automatically applied at both the transmitter and the receiver at all stations. Corrections for an error due to the curvature of the earth may be similarly applied. Data at the receiver is normally converted from ground coordinates to slant coordinates by associated equipment.

b. The basic block diagram (fig. 20) is used in this chapter as the basis for the discussion of the theory of operation of the data set. The power supplies, being common to both the transmitter and receiver, are described first. Following this description, the functions of the transmitter are described in the following order: program generator, coordinate multiplex section, encoding section, data processing section, output section and the automatic zero set control. The functions of the receiver are described in the following order: input section, programmer section, data process-

ing section, decoder network and amplifier section, and coordinate multiplex and storage section. This general procedure is also followed in chapters 7 and 8.

Figure 20. Coordinate data set AN/TSQ-36, basic block diagram.
(Contained in separate envelope)

50. Abbreviations and Terms

Many of the abbreviations and terms used in the discussion of the theory of operation of the data set are peculiar to this type of equipment and are not usually found in discussions of the more familiar radio circuits. For this reason, a glossary, containing a list of abbreviations and definitions of unusual terms, is included in this manual and is located immediately following the appendixes. Reference should be made to the glossary each time an unfamiliar abbreviation or term is found in the text.

51. Binary Numbers

The digital data in the data set is expressed by the binary system of numbers. The processing of binary numbers is performed by the binary counters, shift registers, and other circuits. A knowledge of binary numbers, to the extent of their application here, is required for a full understanding of the processing functions. Appendix I, Binary Numbers—Theory and Application, contains enough information on the nature and use of binary numbers to explain how they are used in the transmission of information by the data set. Familiarity with appendix I will aid in understanding the material in chapters 7 and 8.

52. Circuit Configurations

Certain circuit configurations are used repeatedly throughout the data set, and in chapters 7

and 8 each configuration is referred to by its type of circuit. Examples are flip-flop, flip-zero, AND gates, OR gates, and their variations. These, and other repetitive circuit configurations, are described in appendix II, Basic Control Circuit Elements. Unless circuit configurations referred to in chapters 7 and 8 differ from those described in appendix II, they will not be described in detail in those chapters.

53. Packaged Circuits

Flip-flop, and flip-zero circuits are packaged circuits. There are nine different types of these packages, each type being identified by a letter prefix, such as A package. The other packages are identified as B, C, D, E, J, K, L, and M. Each of these packages is described in detail in paragraphs 92 through 102. It will be helpful to recognize the function of each of these packages, whether flip-flop (F/F) or flip-zero (F/O), and to recognize their input and output circuits

before proceeding with chapters 7 and 8. On main schematic drawings of the data set, packages are represented as blocks with numbered terminals, and the type of package (A, B, etc.), function (F/F, F/O), and other identifying information is printed within the enclosures of the blocks. A schematic diagram of each package used on the main drawing is shown on the right hand side of the first sheet of the drawing. Reference to the package schematics will assist in associating the terminal numbers used in the blocks with the internal wiring of the packages.

54. Transistors

Appendix III, Transistors, defines the transistor and describes both the junction type and the point contact type used in the data set. Two typical circuits, the F/F and the F/O, are analyzed, and the features of the point contact transistor which make such circuits possible are discussed.

Section II. POWER SUPPLIES

55. General

All power for the data set is furnished by one low voltage power supply and one high voltage power supply. Both power supplies require a primary power source of 115 volts, 60 cycles.

56. Low Voltage Power Supply

(fig. 21)

The low voltage power supply furnishes +4.5 volts dc transistor emitter bias, -20 volts dc for transistor collector circuits, -70 volts dc for the indicating neon lamps in the transmitter and receiver units, nominal 6.3 volts ac heater power to the tubes in both the transmitter and receiver, and a voltage divider in the transmitter unit and one in the receiver unit to furnish intermediate negative voltages to the various circuits.

a. Both the +4.5-volt dc and the -20-volt dc rectifiers operate from a power transformer which is voltage and frequency regulated. The +4.5-volt rectifier uses a bridge-type selenium rectifier, with the rectified output voltage filtered by an L-type inductance-capacitance network. The output is loaded by a resistor. A relay, whose contacts are in series with the output of the -20-volt rectifier, ensures that -20 volts cannot be delivered to the data set by the power supply in the absence of +4.5 volts.

b. The -20-volt rectifier consists of two selenium diodes in a full wave circuit. The rectifier output is filtered by an L-type inductance-capacitance network.

c. The low voltage power supply has four 6.4-volt ac outputs, all of which are unregulated.

d. The -70-volt output derives its power from the -300-volt output of the high voltage power supply. It has half-cycle voltage of power line frequency superimposed on its output, which varies its output from -62 to -80 volts at the line frequency.

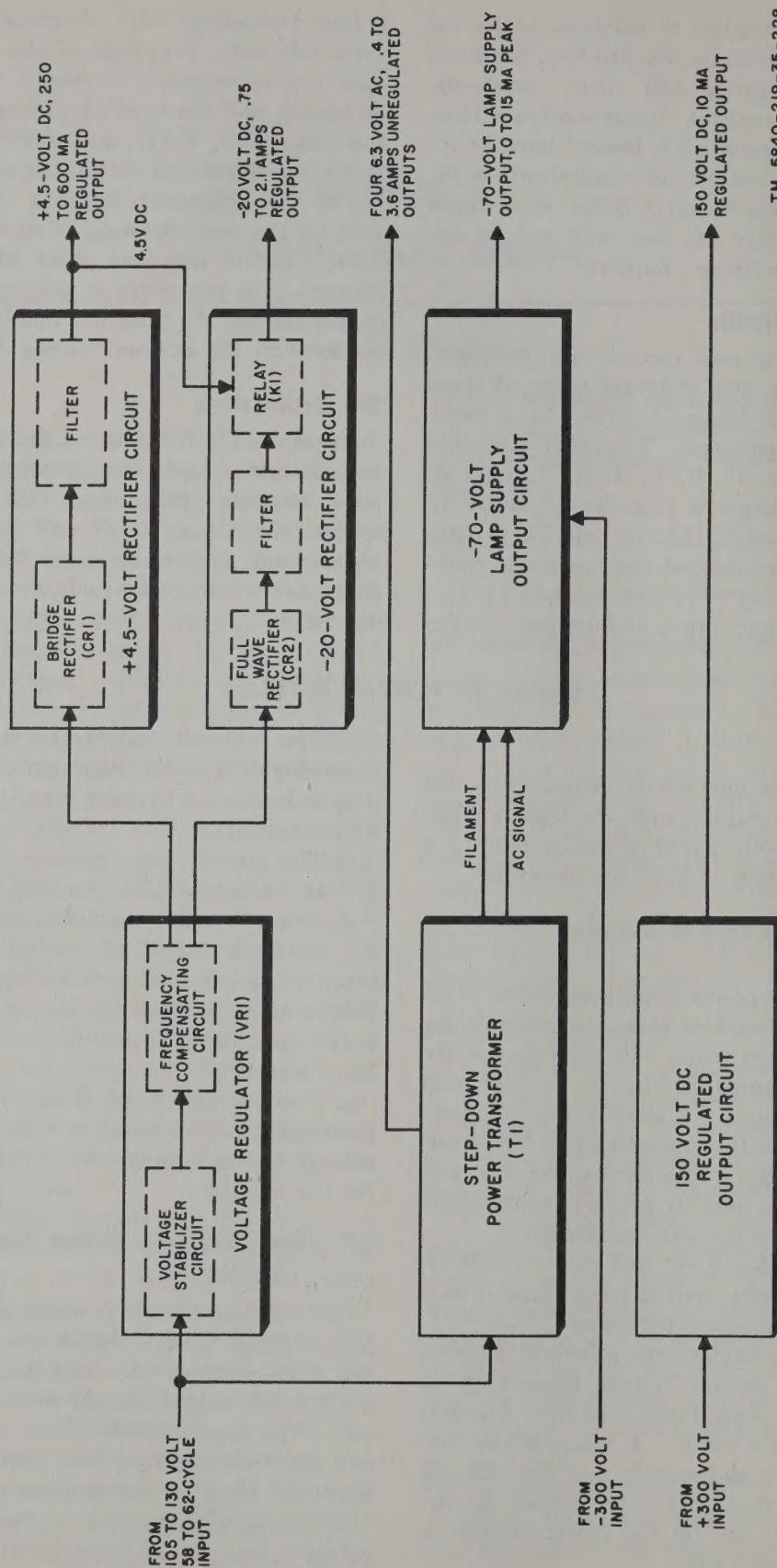
e. Positive 300 volts from the high voltage power supply is applied to a gas tube in the low voltage power supply and furnishes +150 volts for the encoder.

57. High Voltage Power Supply

(fig. 22)

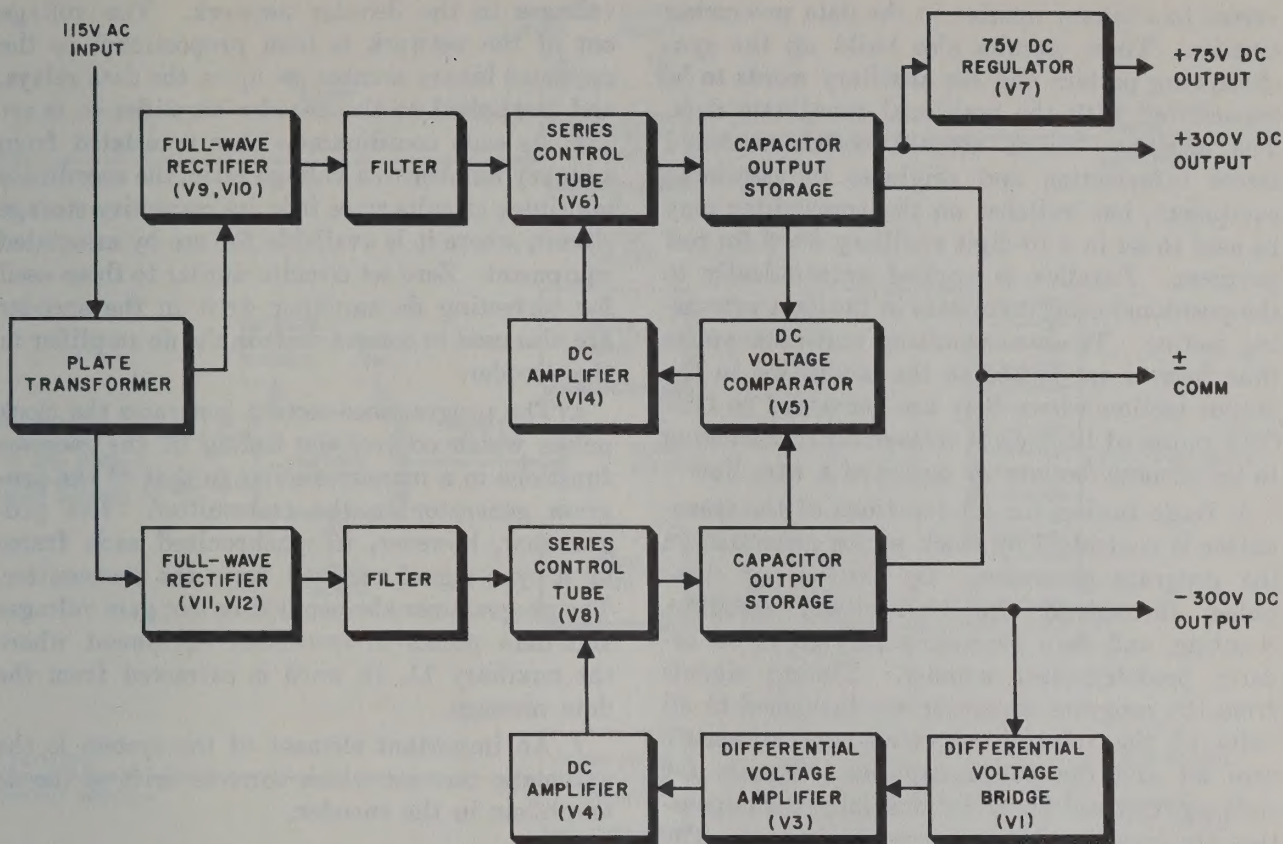
a. The high voltage power supply uses a single high voltage power transformer operating two full wave electron tube rectifiers, one to furnish a +300-volt output and the other a -300-volt output. The negative side of the +300-volt output and the positive side of the -300-volt output are connected together at a common point.

b. The output of each of the rectifiers is filtered by an inductance-capacitance filter network and



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Figure 21. Low voltage power supply, block diagram.



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Figure 22. High voltage power supply, block diagram.

is regulated by series control tubes. Additional storage capacitance is connected across the output of the regulator tubes for further filtering. To maintain the 300 volts within limits and to ensure that the negative and positive voltages vary together with respect to their common output lead, the -300-volt output is load- and reference-potential regulated, and is made the reference voltage for the +300-volt output. A differential voltage bridge and reference voltage gas tube monitor the -300-volt output. The output of the bridge is amplified and applied to the control grids of the -300-volt series regulator tubes. A

voltage comparator operating on a potentiometer connected between the positive and negative 300-volt outputs applies its amplified voltage to the control grids of the +300-volt series regulator tubes. Precise regulation and interlocking of the positive and negative 300-volt supplies is a requirement imposed by the dc amplifiers in the encoder and decoder for which these voltages are primarily required. The +300-volt output also furnishes a gas tube regulated +75-volt output for use as screen grid supply voltage. A voltage of ± 300 volts is furnished to the low voltage power supply.

Section III. TRANSMITTER AND RECEIVER

58. General

(fig. 20)

a. Target position data is received from associated equipment in the form of three slowly varying dc voltages, one for each of the three positional coordinates, H, X, and Y. Each of these voltages represents a coordinate of position

of an aerial target in space. The coordinate voltages appear continuously at the inputs to the coordinate multiplex circuits, which present each coordinate voltage in turn to the encoder. The output of the encoder is a series of 100-kc pulses, varying in number according to the value of the voltage being encoded. These pulses are con-

verted to a binary number in the data processing circuits. These circuits also build up the synchronizing pattern and the auxiliary words to be transmitted with the positional coordinate data. The auxiliary words contain coded command status information and originate in associated equipment, but switches on the transmitter may be used to set in a 10-digit auxiliary word for test purposes. Parallax is applied automatically to the positional coordinate data in the data processing section. The synchronizing and data pulses thus formed are passed to the modulator in the output section where they are converted to ON-OFF pulses of 1,500-cycle voltage for transmission to the distant receiver by means of a wire line.

b. Basic timing for all functions of the transmitter is controlled by clock pulses generated in the program generator. By the use of these pulses throughout the transmitter, encoding, counting, and data processing proceed in an orderly predetermined manner. Timing signals from the program generator are furnished to all units of the transmitter except the automatic zero set and the power supplies. Signals for starting the transmitter for normal system operation are furnished by associated equipment. The transmitter furnishes its own stop control. Some of the circuits which aid in controlling the starting of the transmitter are in the input section of the receiver. Under certain conditions, these circuits also determine what associated equipment the receiver will listen to.

c. Signals for controlling the normal system operation of the receiver are furnished by associated equipment and are applied to the input section. The input section also demodulates the incoming signals, selects the sense of each incoming pulse (whether a ONE or a ZERO), and passes on to the data processing section the dc pulses which are reshaped and retimed duplicates of the data signals received on the line from the transmitter. The data processing section separates the 10-digit auxiliary word from the coordinate data words, and automatically applies parallax correction to the coordinate data. The parallax corrected coordinate data is sent to associated equipment for conversion from ground coordinate data to slant coordinate data, and then is returned to the data processing section. The corrected coordinate data is further processed to set up the binary number on the decoder data relays. These relays apply positive and negative

voltages to the decoder network. The voltage out of the network is then proportional to the corrected binary number set up on the data relays, and is applied to the decoder amplifier.

d. As each coordinate is thus translated from a binary number to a voltage ratio, the coordinate multiplex circuits store it in its respective storage circuit, where it is available for use by associated equipment. Zero set circuits similar to those used for correcting dc amplifier drift in the encoder are also used to correct drift in the dc amplifier in the decoder.

e. The programmer section generates the clock pulses which control the timing of the receiver functions in a manner similar to that of the program generator in the transmitter. The programmer, however, is synchronized each frame by a sync signal received from the transmitter. The programmer also sends time slot gate voltages and data pulses to associated equipment where the auxiliary 11, 12 word is extracted from the data message.

f. An important element of the system is the automatic zero set which corrects drift of the dc amplifiers in the encoder.

59. Transmitter Program Generator (fig. 23)

a. The program generator is normally started by control signals received from associated equipment and is stopped by a reset gate circuit within the program generator. It also may be started by control signals from the receiver input section which, in turn, are developed upon receipt of a remote start signal from associated equipment.

b. The program generator produces the time slot signals and clock pulses which activate the transmitter circuits to time the various functions. The basic timing for the program generator is the 1,500-cycle signal input to the clock pulse generator. The 1,500-cycle signal drives the clock pulse generator circuits at a rate of 750 pps, the basic line signaling speed. These clock pulses are spikes of voltage which are applied continuously to the units and tens ring stages (ring counters), to logic circuits within the program generator, and to other circuits throughout the transmitter. The clock pulse generator also generates set zero pulses which are used in the data processing section. The ring counter circuits control the program generator coincidence gates (time control gates). These gates activate vari-

start and reset pulses to the encoder. In addition the program generator generates a signal to the modulator which sends a ready tone out on the line to the receiver. This is done in the ready tone control circuits which are activated by clock pulses and appropriate time slot gate voltages as well as by start and stop signals from associated equipment.

60. Transmitter Coordinate Multiplex Circuits (fig. 24)

The coordinate multiplex circuits consist of the H, X, and Y coordinate data relays and their lockup circuits, the lockup release gates, and the lockup release F/O. Included in this section are the earth curvature correction relay lockup and the earth curvature correction relay. Dc voltages, one for each of the target coordinate positions, are applied to their respective data relay contacts and, upon the operation of the relays, are applied in time sequence to the single output circuit going to the encoder. Each relay is operated by its lockup, which, in turn, is turned ON by clock pulses during appropriate time slot gates. The lockups are released by clock pulses applied at appropriate times to the lockup release gates and lockup release F/O. The earth curvature correction relay is actuated by its own lockup and is released by the same circuits which release the data relays.

61. Encoder (fig. 25)

The encoder converts an analog voltage to a number of 100-kc pulses which are processed into a binary number by the data processing section. To do this the encoder first converts the analog voltage to a time interval during which pulses, at the rate of 100,000 per second, are allowed to pass through the encoder circuits. The magnitude of the analog voltage being encoded determines the number of pulses passed.

a. Analog data arriving from the coordinate multiplexer and dc reference voltages from associated equipment are applied to two comparator amplifiers simultaneously with sweep voltages from the sweep circuits. The sweep circuits are started and reset by the reset multivibrator, which is controlled by the program generator. Coincidence of target, reference, and sweep voltages generates gate-open and gate-close pulses representing the start and end of encoding time which

is proportional to the analog voltage being encoded. These pulses are applied to the gate control circuits.

b. The gate control circuits contain a multivibrator which is controlled by the gate-open and gate-close pulses. The output is a square wave gate control voltage having a duration equal to the time between the gate-open and gate-close pulses. This gate-control voltage is applied to the 100-kc pulse gate.

c. The 100-kc pulse gate is a diode enabled by the gate control voltage. The gate is open for the duration of the control voltage. During the time the gate is open, pulses from the 100-kc pulse generator pass through it to the data processing circuits.

d. The 100-kc pulse generator uses a crystal controlled 100-kc oscillator and a pulse generator. These circuits furnish pulses continuously to the pulse gate circuits.

62. Transmitter Data Processing Section (fig. 26)

a. During remote-start operation, each frame of the message is started at time slot 57. At the end of TS 58 a clock pulse is permitted to pass through the ready and sync read-in gate, setting up the ready and sync word in the shift register where it is shifted out. Following this operation at time slot 7, a clock pulse enables the auxiliary read-in gates, setting up the auxiliary 1-10 word in the shift register where it is also shifted out to the output section.

b. A parallax word is read into all binary counter stages in parallel, leaving each stage turned ON or OFF, depending on the digit of the word applied to that stage. Immediately following this, sequential decimal data in the form of 100-kc pulses representing the coordinate H, X, and Y data is applied to the 13-stage binary counter from the 100-kc pulse gate and pulse generator. Each of the binary counter stages divides the count of the number of pulses by 2, and having counted, remains in the state of ON or OFF, depending on the count. Upon completion of the count, the digital word with the parallax added is in the binary counters. The word in the counters is then shifted, all stages simultaneously, by a clock pulse applied through the 13 data read-in gates which are opened by a time slot gate voltage. The binary counters are then reset by a clock pulse passing through

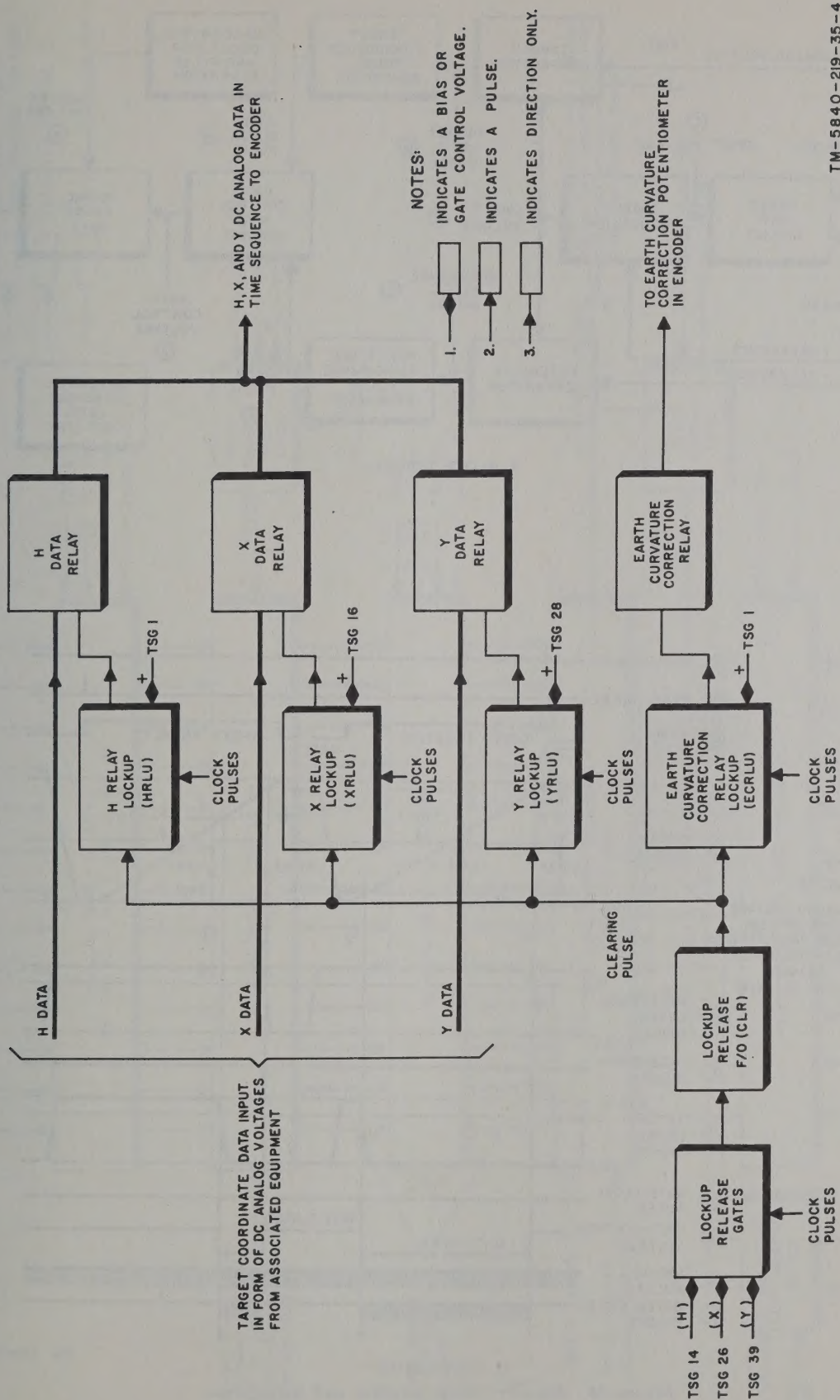
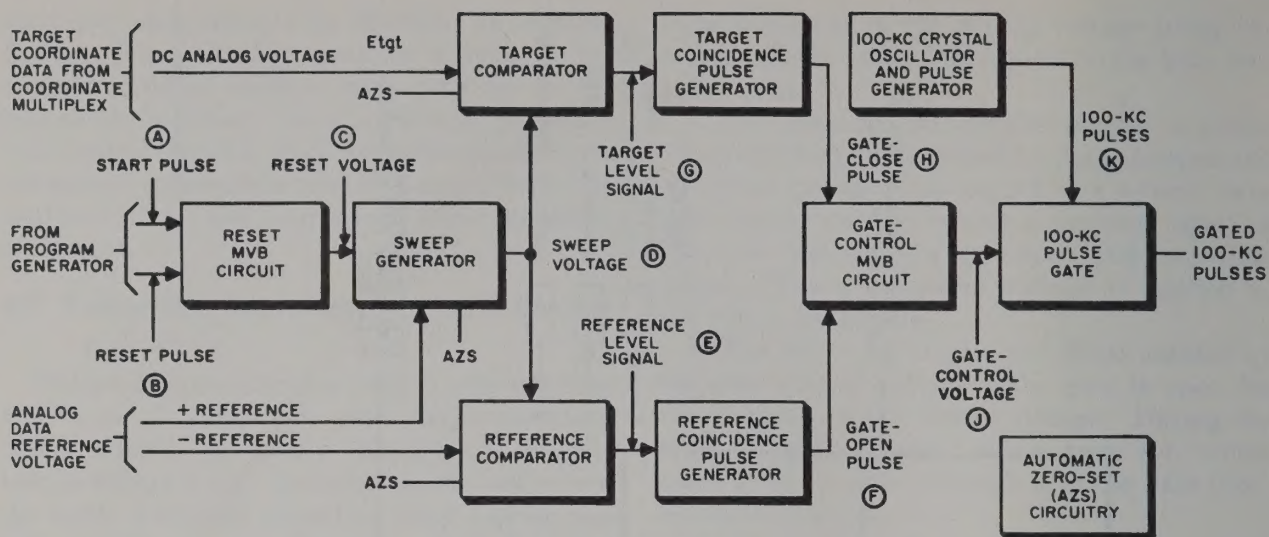


Figure 24. Coordinate multiplexer, block diagram.



NOTE:
 E_{tgt} = DC ANALOG VOLTAGE
 $-E_{tgt}$ = NEGATIVE OF E_{tgt}
 K_{ref} = VOLTAGE PROPORTIONAL TO NEGATIVE REFERENCE VOLTAGE
 $-K_{ref}$ = NEGATIVE OF K_{ref}

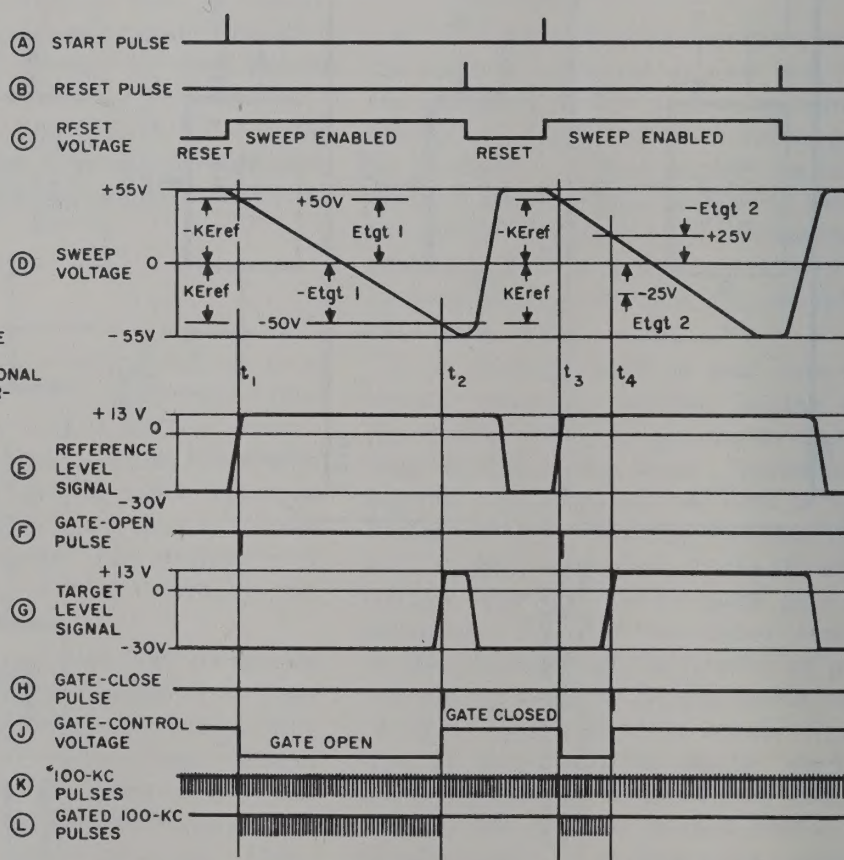


Figure 25. Encoder, block diagram and waveforms.

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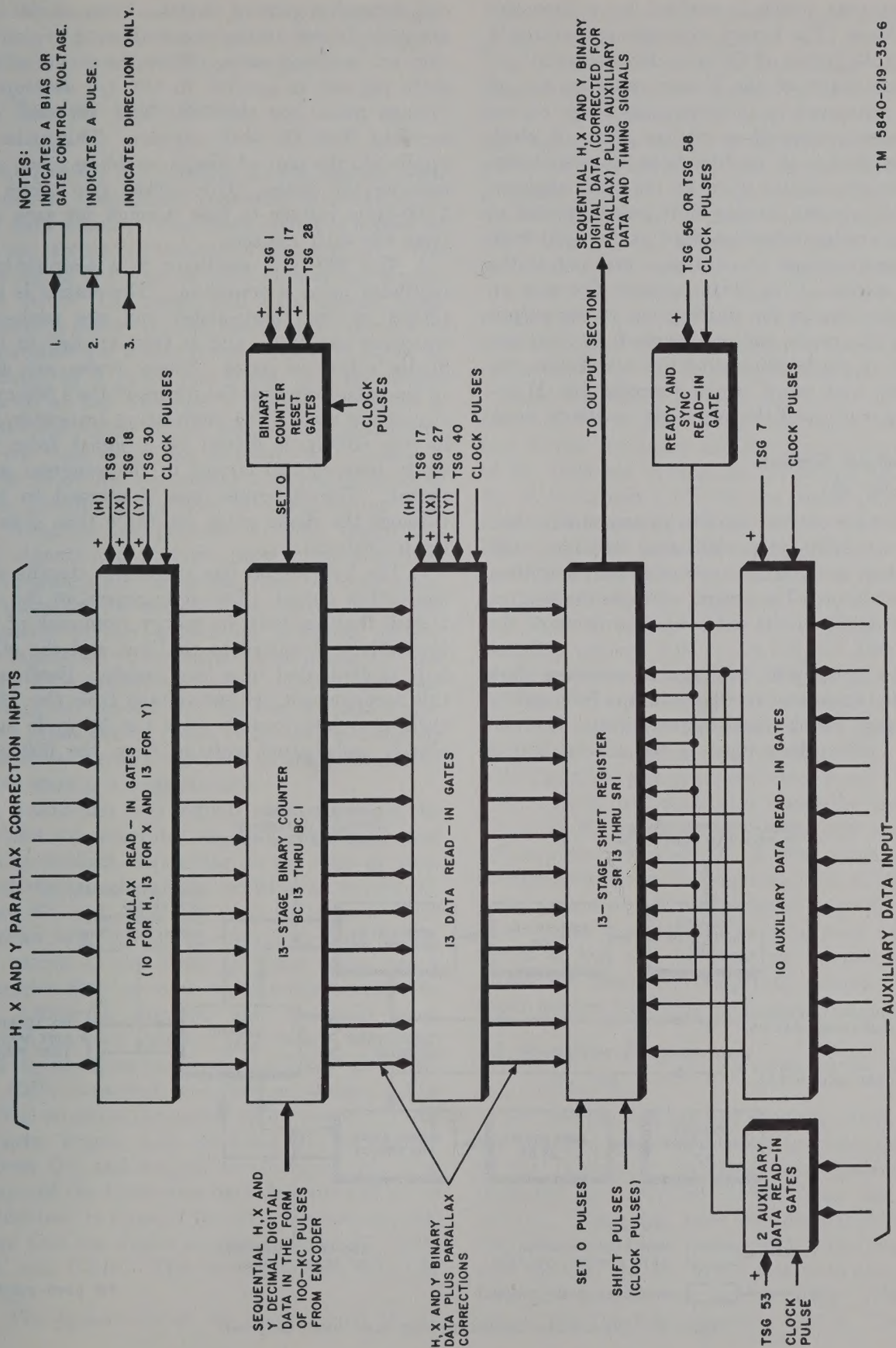


Figure 26. Transmitter, data processing section, basic block diagram.

the reset gate which is enabled by a time slot gate voltage. The binary counters are then ready to count the pulses of the next decimal word.

c. Each stage of the binary counters has its output connected to its associated stage of the shift register through a read-in gate. A clock pulse, applied to all read-in gates simultaneously, transfers the digital word to the shift register. The shift register, having shift pulses applied to it continuously, shifts each digit of the word from shift register stage 13 to stage 1 and out to the output section. The shift register also sets up three other words for shifting out to the output section; the ready and sync signals to start the receiver at the beginning of the new frame, the auxiliary 1-10 word which precedes the H coordinate word, and the two-digit auxiliary word.

63. Output Section

(fig. 27)

The output section consists of two similar circuits: the 1,500-cycle oscillator, amplifier, and modulator; and the 600-cycle oscillator, amplifier, and modulator. The output of these modulators is transmitted to the outgoing line through the hybrid coil.

a. The 1,500-cycle oscillator is a tuning fork controlled transistor oscillator and is followed by a two-stage tuned transistor amplifier. The amplified 1,500-cycle voltage is fed to the hybrid

coil through a pair of diodes. These diodes are normally biased to the nonconducting region so they act as closed gates. When the output of the shift register is applied to Q6, Q6 develops a voltage pulse, one time slot long, for each one arriving from the shift register. This pulse is applied to the pair of diodes, enabling them, and opening the gates. This allows two cycles of 1,500-cycle voltage to pass through for each one from the shift register.

b. The 600-cycle oscillator is a Colpitts-type oscillator using a transistor. The output is amplified by one single-ended and one push-pull transistor amplifier, and is then applied to two diodes acting as gates. These diodes are used in the same way that the diodes in the 1,500-cycle circuit are used. The modulating transistor, Q5 in this circuit, is driven by a signal from the ready tone control circuit in the program generator. The 600-cycle tone is allowed to pass through the diode gates for three time slots to the hybrid coil.

c. The hybrid coil has two input circuits and one output circuit. The arrangement of the coil is such that one-half the energy from each of the inputs is transmitted to the line, and the other half is dissipated in a load resistor. Because of this arrangement, output voltage from the 1,500-cycle modulator cannot enter the 600-cycle modulator, and output voltage from the 600-cycle

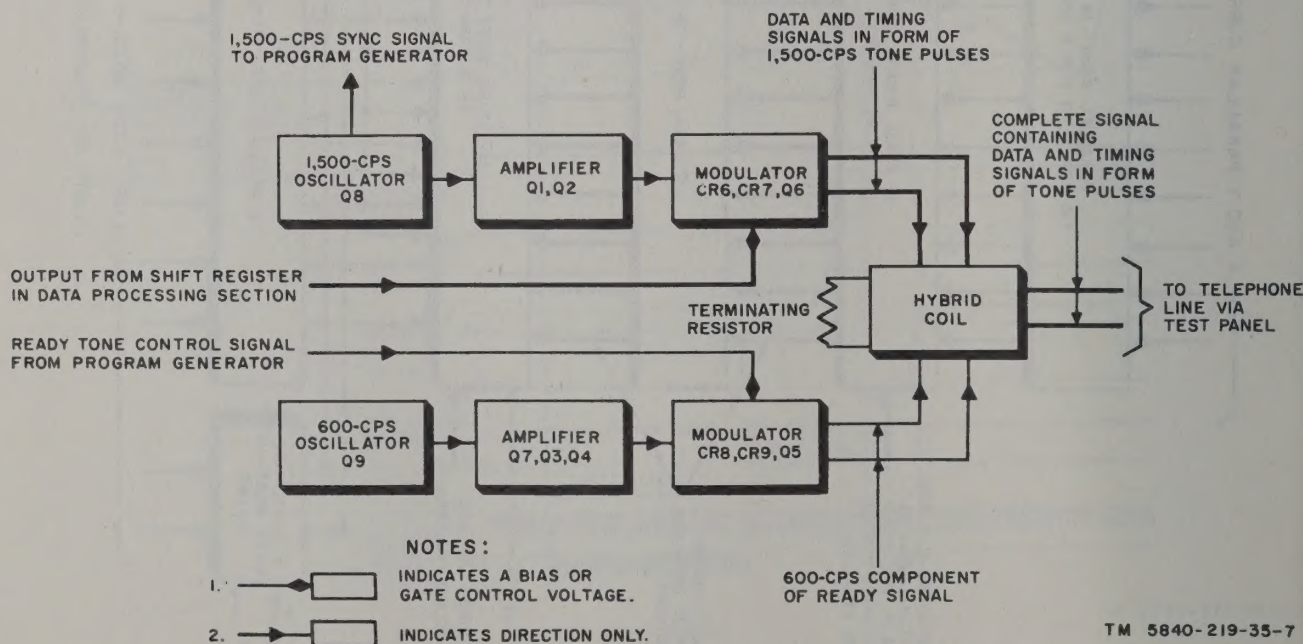


Figure 27. Transmitter output section, basic block diagram.

modulator cannot enter the 1,500-cycle modulator. Both the 1,500-cycle and the 600-cycle signals are transmitted to the common output line.

64. Receiver Input Section

(fig. 28)

The receiver input section accepts signals from the distant transmitter, consisting of ready, sync, and data signals. The ready signal is a tone of 600 cps lasting for three time slots (fig. 2). The data signal is a tone of 1,500 cps lasting for six time slots. The ready and data signals must overlap in order to reset the receiver circuits in preparation for a new frame. The sync signal is preceded by a guard slot which is a no-voltage interval of one time slot. The sync signal is a 1,500-cycle signal which follows the guard slot for one time slot. The auxiliary H, X, and Y words follow the sync signal as shown in figure 2. Logic circuits in the receiver input section (fig. 28) recognize the presence of both ready and data signals and perform these functions: reset the frequency divider stages, reset the ring counter stages in the programmer section, start the frequency divider generating sampling pulses, and regenerate the received data pulses for use in the data processing section. Circuits for performing the remote start function are also a part of the input section (Pars. S157-159) and signals from these circuits are used to start the transmitter start and reset circuits.

a. Ready and data signals are received on the line and are amplified by V2A, or by V1 and V2A in tandem, depending on the type of associated equipment and the position of switch S1. When V1 and V2A are used in tandem, V2B provides AGC voltage to control the gain of V1. The output of the input amplifier feeds into a separation filter network which separates the 600- and 1,500-cycle signals, and transmits each through its own detector and slicer. The 600-cycle signal is detected by diodes CR3, CR4, CR5, and CR6, connected in a bridge rectifier. The rectified envelope is squared up by means of three transistor stages: a dc amplifier Q1; an emitter follower Q2; and a signal level trigger Q3. The circuits of the 1,500-cycle data detector and slicer are identical to those of the 600-cycle counterpart, except that the diodes are designated CR7, CR8, CR9, and CR10. The transistors are Q4, Q5, and Q6.

b. The appearance of the ready signal at the

input to the delay F/F circuit turns it ON, which in turn turns ON the divider reset F/F No. 6. The divider reset and F/F No. 3 apply enabling bias to the frequency divider BC 1, BC 2, and BC 3. The frequency divider divides the 6,000-pps signal by a factor of 8, creating sampling pulses at the rate of 750 pps for use in the programmer section. In order to be synchronized by the transmitter, it must first be reset by the OFF bias of sync control F/F No. 3 and then restarted by the received sync signal (*d* below).

c. ON and OFF bias from the divider reset turns F/F No. 2 ON and OFF, allowing it to send signals to the programmer to reset the ring counters so they will be ready for the data signals.

d. At the end of the data signal, the sync control F/F No. 3 goes OFF, applying a matching bias to the frequency dividers and allowing one of the 6,000 pps to reset the divider stages. F/F No. 6 is turned OFF by the same pulse that resets the frequency divider. Sync control F/F No. 3 is turned back ON for the duration of the frame, causing sampling pulses to be generated continuously by the frequency divider.

e. Data from the data slicer triggers data sampling control F/F No. 5 ON for each ONE of the received message, and OFF for each ZERO of the received message. The output of F/F No. 5 is retimed and reformed data pulses for use in the data processing section.

f. The 6,000-pps generator consists of a 1,500-cycle tuning fork controlled transistor oscillator Q1, a buffer amplifier Q2, a shaping amplifier Q3, a pulse generator Q5, a reset stage Q6, an electron tube harmonic generator V3A, a 6,000-pps pulse generator Q4, and a pulse amplifier V3B. The output is a continuous supply of negative pulses at the rate of 6,000 per second. These pulses are used for triggering circuits of the input section (fig. 28).

65. Receiver Programmer

(fig. 29)

The receiver programmer generates clock pulses and time slot gates for the data processing section of the receiver. The clock pulse generator is triggered by sampling pulses from the input section. Time slot gates are generated by the ring counter. Clock pulses and three time slot gate voltages are sent to the associated equipment from the programmer section along with data pulses from the data processing section. The time

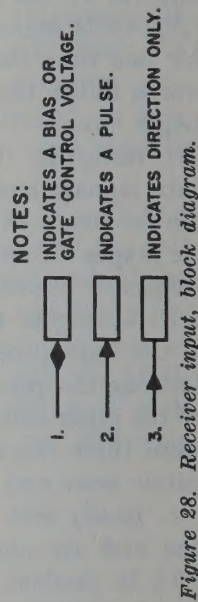
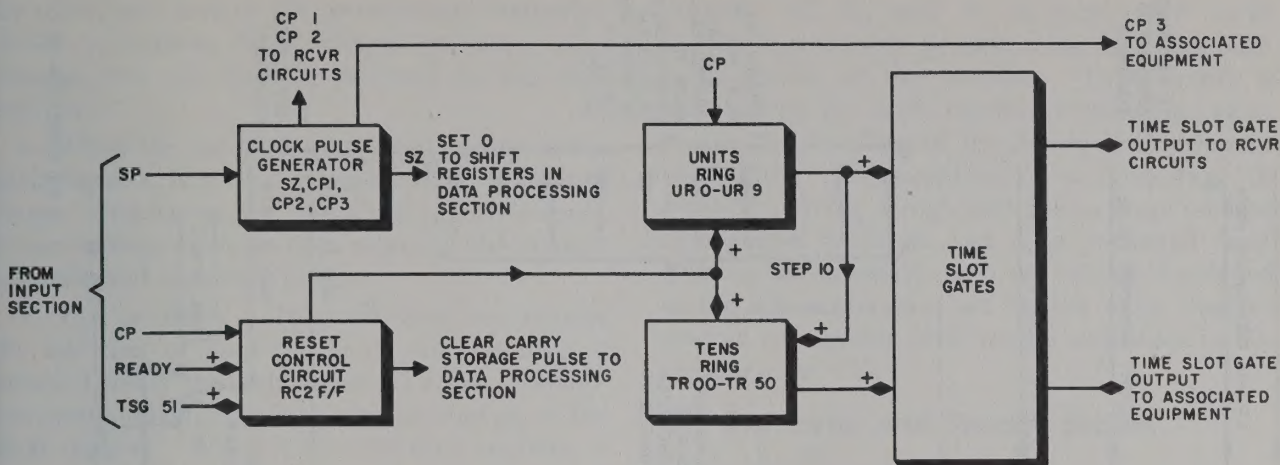


Figure 28. Receiver input, block diagram.



NOTES:

1. INDICATES A BIAS OR GATE CONTROL VOLTAGE.
2. INDICATES A PULSE.
3. INDICATES DIRECTION ONLY.

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Figure 29. Receiver programmer, block diagram.

slot gate voltages which coincide with the auxiliary 11-12 word are used by associated equipment to extract this auxiliary word from the serial data.

a. Sampling pulses (SP) generated in the receiver input section (par. 64b) are applied to four transistor packages, SZ, CP 1, CP 2, and CP 3. These packages are in effect pulse power amplifiers, each repeating the sampling pulse in a modified form. The output of the SZ package is a set zero pulse, and the outputs of CP 1, CP 2, and CP 3 are clock pulses. Two identical clock pulse packages are needed for a distribution of clock pulse load within the receiver and the third for use by associated equipment. Both the SZ and CP outputs are used in the data processing section.

b. The ready signal from the input section (par. 64a) resets the ring counters (units ring (UR) and tens ring (TR)) at the start of the frame through RC 2 F/F, which also enables a gate to pass a clear carry storage pulse. TSG 51 is used to time the reset of the ring counters for continuous operation.

c. The ring counters and time slot gates function in the same way as do those in the transmitter (par. 59). The time slot gates are used for programming the functions of the data processing section (fig. 29).

66. Receiver Data Processing Section (fig. 30)

In the data processing section, serial data from the input section and parallax data are added together and presented sequentially to the decoder network and amplifier section (par. 67). Auxiliary 1-10 data is separated from the coordinate data at the shift registers and appears on relays for distribution to associated equipment. Time slot gate voltages from the programmer are sent to associated equipment for the extraction of auxiliary 11 and 12 digits. An off-scale detector is a part of the data processing section.

a. The serial adder, the parallax read-in gates, the ground-slant converter, and the shift register all work together. The parallax word for each coordinate is set up on the parallax switches and is read in to the shift register through the ground-slant converter at the appropriate times. The shift register is controlled by the shift pulse disable circuit (fig. 131). The parallax word is shifted out of the shift register, digit by digit, into the serial adder. The selection of time slot gates causes the first digit of parallax to arrive at the serial adder coincident with the arrival of the first digit of the coordinate word. The serial adder is a combination of logic circuits which adds the parallax digits and the data digits. The sum word is brought out of the serial adder, digit

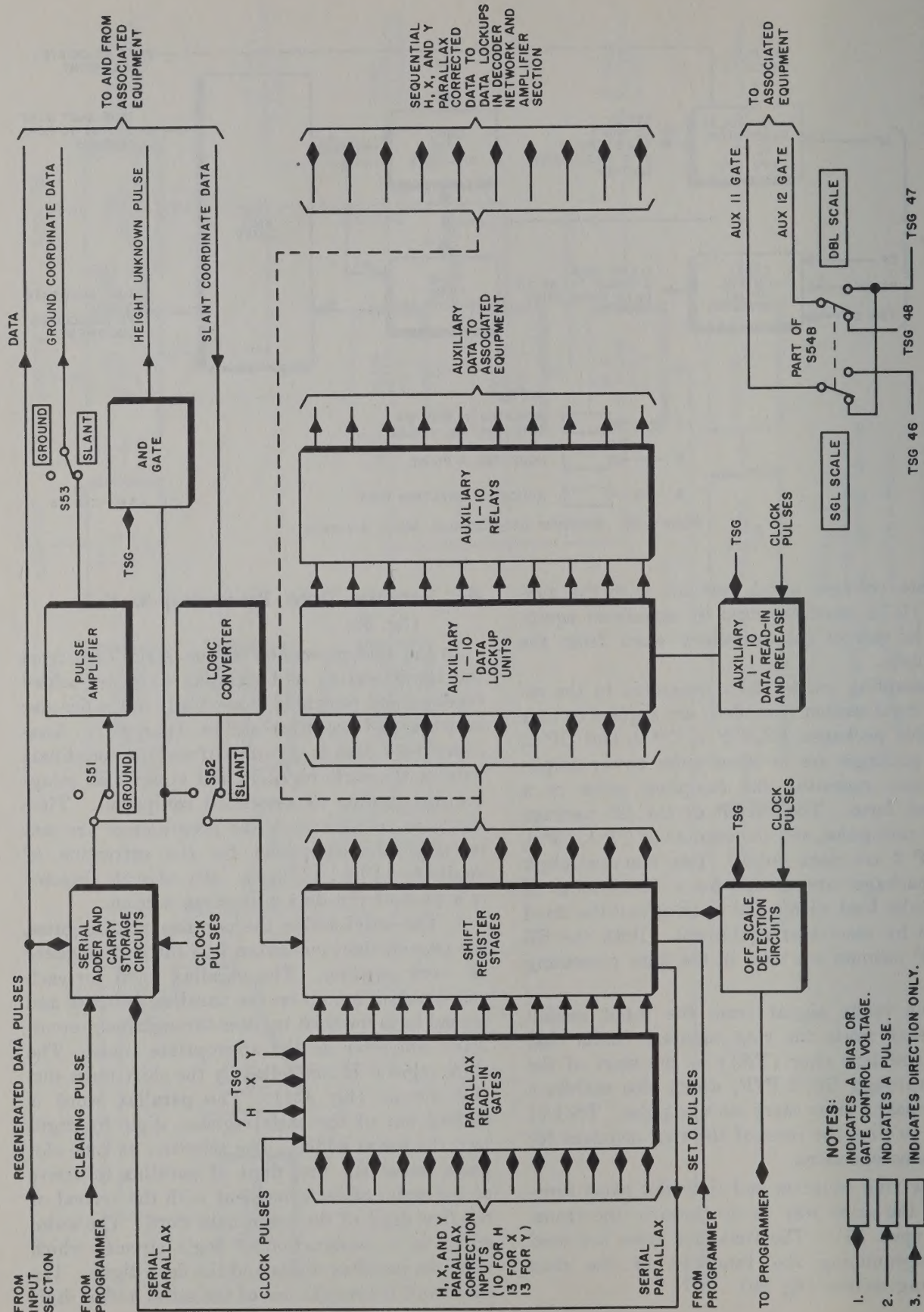


Figure 30. Receiver data processing section, simplified block diagram.

by digit, and sent to the ground-slant converter. After conversion from ground to slant coordinates, the sum data is returned to the shift register.

b. When the complete sum word has filled the shift register, it is read out from all shift register stages simultaneously into the data lockups. These lockups energize data relays in the decoder network and amplifier section.

c. The auxiliary 1-10 word does not require the addition of parallax to it; consequently, it passes directly through the serial adder, through the ground-slant converter without change, to the shift register. When it fills the shift register, it is transferred to the auxiliary data lockups and data relays for use by associated equipment.

d. An AND gate is associated with the data output from the serial adder which generates a height unknown pulse when coincidence of H10 data and TS 19 (for double scale operation) or TS 20 (for single scale operation) occurs.

e. In the event a digital word that is too large to be accommodated by the data relays appears in the shift register, the off-scale detection circuits send a signal to associated equipment.

67. Decoder Network and Amplifier Section (fig. 31)

Each of the data relays in this section is operated by its own data relay lockup. The data relays and decoder network act as a relay-operated voltage divider, dividing the positive and negative reference voltages so that the voltage out of the network is proportional to the binary number shifted out of the shift register in the data processing section. This voltage is then applied to the input of the decoder amplifier where it is sent to the distributor and storage section. This process is performed for each co-

ordinate, H, X, and Y, in turn. The earth curvature correction potentiometer is in the feedback circuit of the decoder. This circuit is switched by the earth curvature correction relay during the decoding of the X and Y coordinates (par. 39f). The amplifier is a three-stage dc amplifier having a high gain and a large amount of negative feedback, and it is prevented from drifting by automatic zero set voltage developed in the automatic zero set in the same manner used to correct for drift in the amplifiers in the encoder (par 61).

68. Distributor and Storage Section (fig. 32)

H, X, and Y coordinate analog voltages from the decoder amplifier are applied to grids of each of three storage cathode follower amplifiers, one for each coordinate. During the time the H coordinate is being decoded, the decoder amplifier output is fed to the grid of the H storage amplifier through its distributor relay contacts. A capacitance-resistance network from grid to ground of the storage amplifier charges to the decoder voltage to store that voltage while decoding circuits are engaged in decoding the X and Y coordinates. The output of the H storage amplifier appears across its cathode resistor and is available at the H coordinate output terminal for use by associated equipment. The same output voltage is fed back to the decoder network through the H feedback relay so that the decoder amplifier feedback voltage is correct for that coordinate. This process is repeated for each of the other coordinates, X and Y, through their respective storage amplifier and relays. The grid and feedback relays are operated by their associated grid and feedback storage lockups. The lockup for the earth curvature correction relay is located in the distributor and storage section.

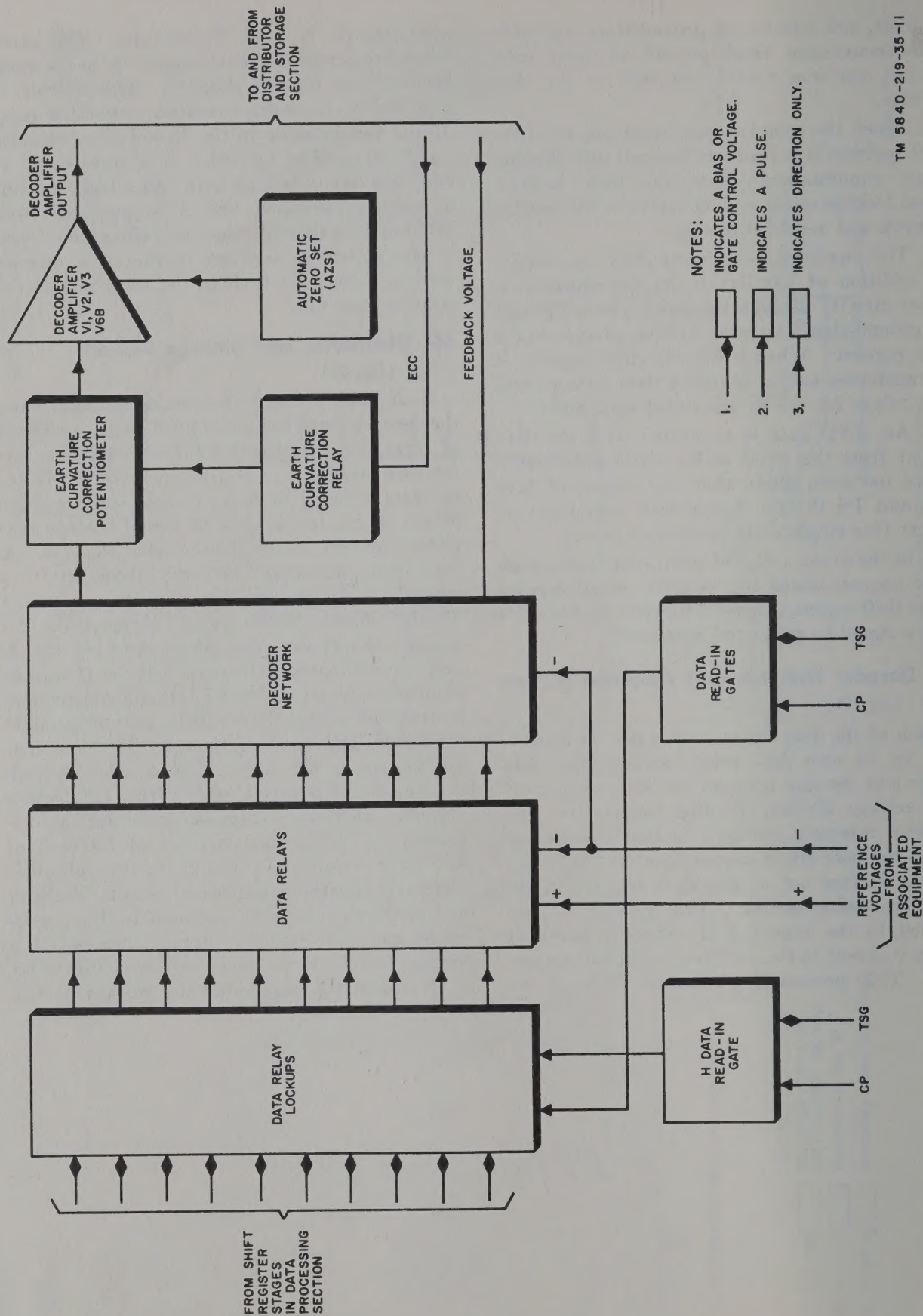
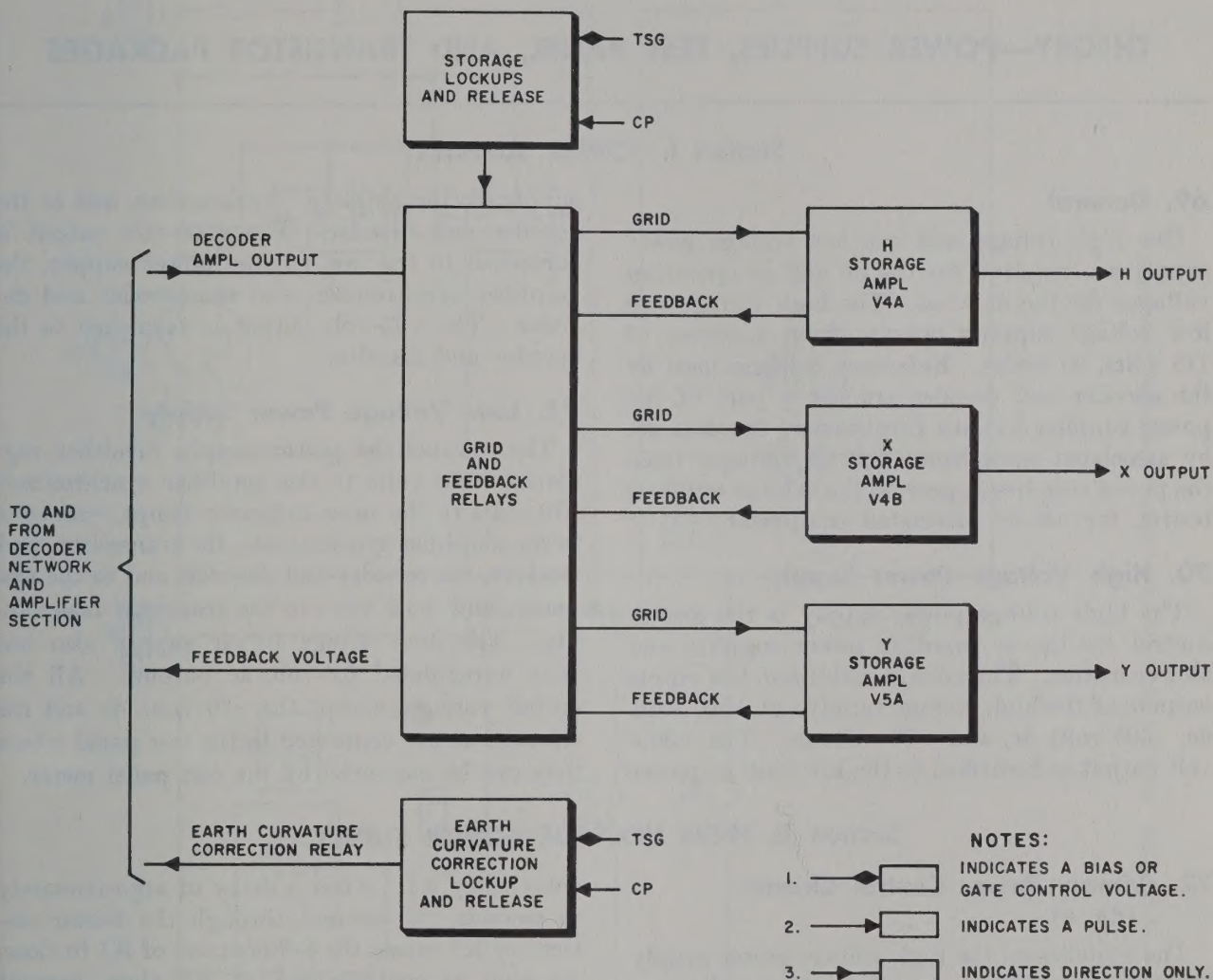


Figure 31. Decoder network and amplifier section, simplified block diagram.



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Figure 32. Distributor and storage section, block diagram.

CHAPTER 6

THEORY—POWER SUPPLIES, TEST PANEL, AND TRANSISTOR PACKAGES

Section I. POWER SUPPLIES

69. General

One high voltage and one low voltage power supply are required for the dc and ac operating voltages for the data set. The high voltage and low voltage supplies operate from a source of 115 volts, 60 cycles. Reference voltages used by the encoder and decoder are not a part of the power supplies but are furnished to the data set by associated equipment. All dc voltages from the power supplies appear on the cabinet terminal boards for use by associated equipment.

70. High Voltage Power Supply

The high voltage power supply is the master control for the ac input to power supplies and blower motors. The voltage stabilized, low ripple outputs of the high voltage supply are +300 volts dc, -300 volts dc, and +75 volts dc. The +300-volt output is furnished to the low voltage power

supply, to the amplifier synchronizer, and to the encoder and decoder. The -300-volt output is furnished to the low voltage power supply, the amplifier synchronizer, and the encoder and decoder. The +75-volt output is furnished to the encoder and decoder.

71. Low Voltage Power Supply

The low voltage power supply furnishes regulated +150 volts to the amplifier synchronizer, -70 volts to the neon indicator lamps, -20 volts to the amplifier synchronizer, the transmitter and receiver, the encoder and decoder, and to the test panel; and +4.5 volts to the transistor bias supply. The low voltage power supply also has four unregulated 6.4-volt ac outputs. All the output voltages except the -70 volts dc and the 6.4 volts ac are connected to the test panel where they can be measured by the test panel meter.

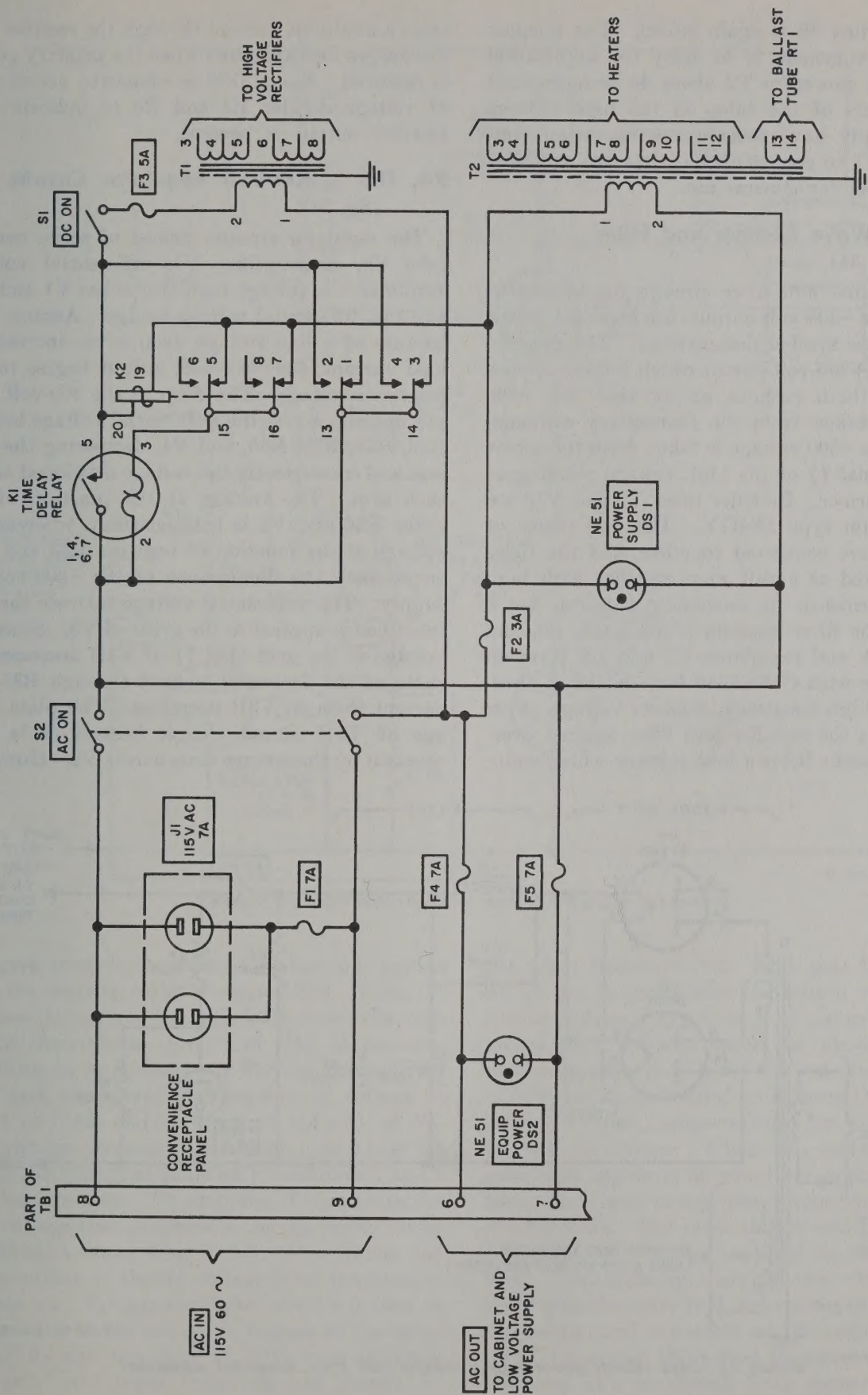
Section II. HIGH VOLTAGE POWER SUPPLY

72. Primary Power Control Circuits

(fig. 33)

The switches on the high voltage power supply function as a master control for the application of all power to the data set. Primary power is connected to terminals 9 and 10 of TB1 on the high voltage power supply. Terminals 6 and 7 go to the low voltage power supply and to the blower motors in the cabinet. During normal operation the +4.5V & -20V SUP ON-OFF switch on the low voltage power supply is left at the ON position, although it may be operated independently if desired. When AC ON switch S2 is closed, power is supplied to AC OUT terminals 6 and 7, and to the primary of transformer T2 through fuse F2. Power is also applied to the heater element (contacts 2 and 3) of time

delay relay K1. After a delay of approximately 45 seconds, the current through the heater element of K1 causes the 5-7 contacts of K1 to close. As soon as contacts 5-7 of K1 close, current flows through the winding of K2, opening contacts 5-15 and 7-16 of K2, and closing contacts 2-13 and 4-14 of K2. This action interrupts the current through heater 2-3 of K1, allowing it to cool and open contacts 5-7 of K1. Current now flows from AC IN terminal 8 through S2, contacts 2-13 and 4-14 of K2, through S1, F3, and primary 1-2 of T1, back through S2 to AC IN terminal 9. Relay K2 is held operated by current from AC IN terminal 8, through S2, K2 contacts 2-13 and 4-14, through K2 winding and back through F2 and S2 to AC IN terminal 8. When S2 is opened, K2 releases. This process is



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Figure 33. Primary power control circuits, simplified schematic.

repeated when S2 is again closed. The purpose of this arrangement is to delay the application of primary power to T2 about 45 seconds until the filaments of the tubes in the high voltage power supply have come up to operating temperature. Two convenience outlets are available on the panel for general use.

73. Full Wave Rectifier and Filter (fig. 34)

The rectifier and filter circuits for the +300-volt and the -300-volt outputs are identical except for reference symbol designations. The description of the +300-volt circuit which follows applies equally to both circuits, except that the +300 voltage is taken from the filamentary cathodes, whereas the -300 voltage is taken from the center tap (terminal 7) of the high voltage winding of the transformer. Rectifier tubes V9 and V10 are high vacuum type 5R4GY. The two plates of each tube are connected together, and the tubes are connected as a full wave rectifier with high voltage furnished by secondary winding 3-4-5 of T1. The filter consists of C13, C1, C2, and L1A. L1A and capacitors C1 and C2 form an L-type filter with C13 added for additional filtering of the high frequency transient voltage. Fuse F6 protects the rectifier and filter against overloads. Resistor R2 is a load resistor which main-

tains a minimum current through the rectifier and discharges the capacitors when the primary power is removed. Lamp DS3 is connected across part of voltage divider R4 and R6 to indicate that rectifier output is present.

74. The -300-Volt Regulator Circuits (fig. 35)

The regulator circuits consist of series control tube V8, dc amplifier V4, differential voltage amplifier V3, voltage regulator tubes V1 and V2, and the differential voltage bridge. Assume that because of a line voltage drop or an increase in load current, the -300-volt output begins to decrease in voltage. The drop in the 300-volt output appears across the differential voltage bridge, R33, R34, R39, R36, and V1, decreasing the current and consequently the voltage developed across each arm. The voltage at the junction of resistor R36 and V1 is held constant, whereas the voltage at the junction of resistors R33 and R34 varies with the fluctuations of the -300-volt dc supply. The differential voltage between the two junctions is applied to the grids of V3. Since the voltage at the grid (pin 7) of V3B decreases because of the decreased current through R33, the current through V3B decreases. The plate voltage of V3B cannot change because it is held constant by the voltage drop across V2. However,

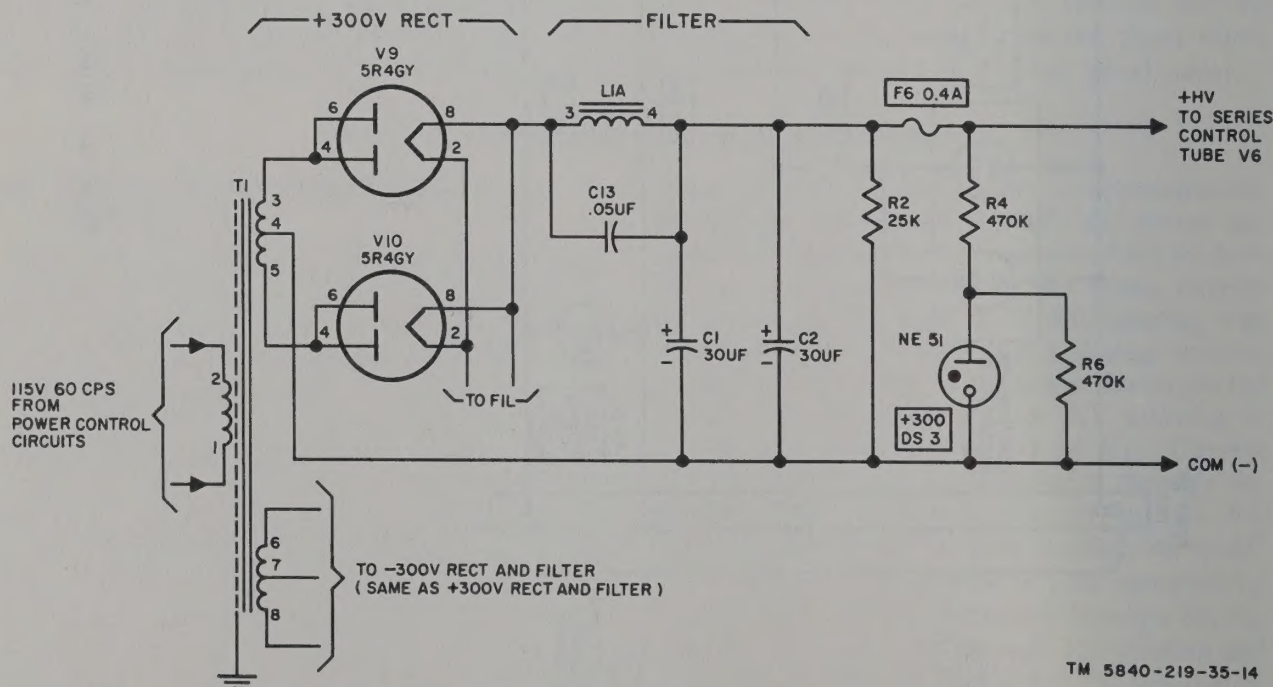


Figure 34. High voltage power supply rectifier and filter, simplified schematic.

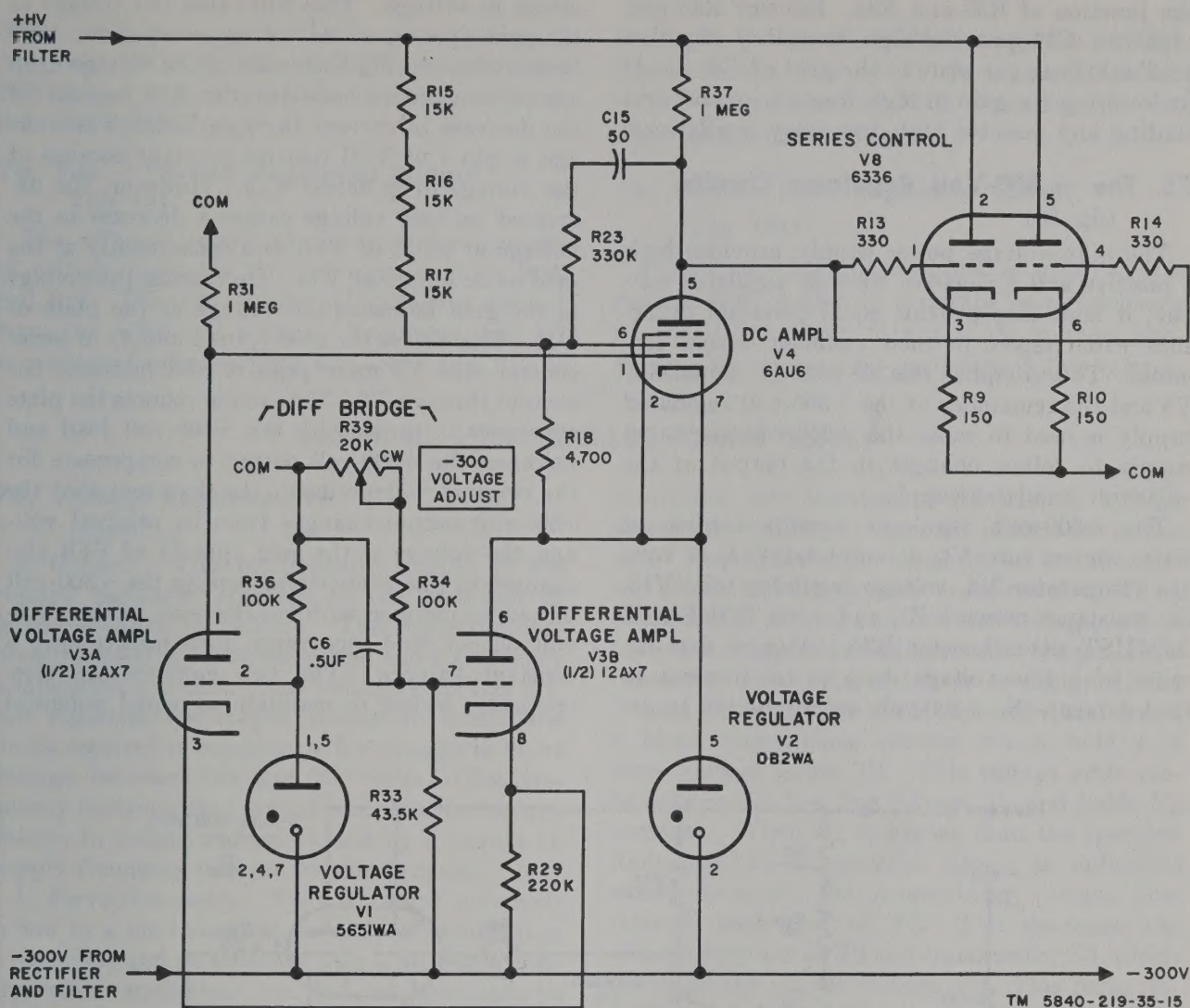


Figure 35. -300-volt regulator circuit, simplified schematic.

the grid receives the voltage change and applies it to the common cathode resistor R29. Thus, the decrease in current through V3B causes the voltage at the cathode (pin 3) of V3A to decrease, resulting in an increase of current through the tube and consequently a decrease in voltage at pin 1 of V3A and at the grid (pin 1) of V4. The voltage decrease at the grid (pin 1) of V4 causes the voltage at pin 5 of V4 and pins 1 and 4 of V8 to increase. Dc amplifier V4 provides the bias voltage that produces a change in the plate-to-cathode voltage drop in V8. It amplifies the dc variations to the dc voltage level required to operate V8. Voltage regulator tube V2 is used to prevent any variations of dc voltage at the cathode of V4 and the plate of V3B, thus ensuring that only grid input variations are present in

the plate circuit of V4. Note that both halves of V8 are in series with the output voltage and that a positive-going voltage at the grids will increase plate current, lower the plate-to-cathode resistance, effectively lower the resistance in series with the load, and therefore increase the negative voltage output, compensating for the original decrease in voltage. When the -300-volt output goes more negative, an equal but opposite action takes place and brings the output voltage back to -300 volts. The ratio of R39 and R34 to R33 determines the voltage applied to the grid of V3B. Consequently, varying the -300 voltage adjust potentiometer R39, determines the final output voltage and is used to set the output at -300 volts. Capacitor C6 is used to prevent any high frequency or noise signals from appearing across

the junction of R33 and R34. Resistor R23 and capacitor C15 provide high frequency negative feedback from the plate to the grid of V4, thereby lowering the gain to high frequencies and preventing any possible high frequency oscillations.

75. The +300-Volt Regulator Circuits (fig. 36)

The high voltage power supply provides both a positive and a negative 300-volt regulated output; it must also provide equal potential difference with respect to their common output terminal. To accomplish this, dc voltage comparator V5 and the remainder of the +300-volt regulated supply is used to cause the +300-volt regulated supply to follow changes in the output of the -300-volt regulated supply.

The +300-volt regulator circuits consist of series control tube V6, dc amplifier V14, dc voltage comparator V5, voltage regulator tube V13, the resistance network Z1, and +300 VOLTAGE ADJUST potentiometer R35. Assume that because of a line voltage drop or an increase in load current, the +300-volt output begins to de-

crease in voltage. This will cause the voltage at the grid (pin 2) of dc voltage comparator V5B to decrease, causing a decrease in the voltage drop across common cathode resistor R30 because of the decrease in current through V5B. The voltage at pin 1 of V5B remains constant because of the voltage drop across V13. However, the decreased cathode voltage causes a decrease in the voltage at pin 6 of V5A and consequently at the grid of dc amplifier V14. Decreasing the voltage at the grid increases the voltage at the plate of V14. This drives the grid (pins 1 and 4) of series control tube V6 more positive and increases the current through V6. This action reduces the plate resistance in series with the +300-volt load and increases the +300-volt output to compensate for the original voltage drop. In the event that the -300-volt output changes from its original voltage, the voltage at the grid (pin 2) of V5B also changes in like proportion, causing the +300-volt output to increase with the decrease in the -300-volt output, and vice versa, thus maintaining a constant balance. The two voltages are electronically locked to maintain an equal potential

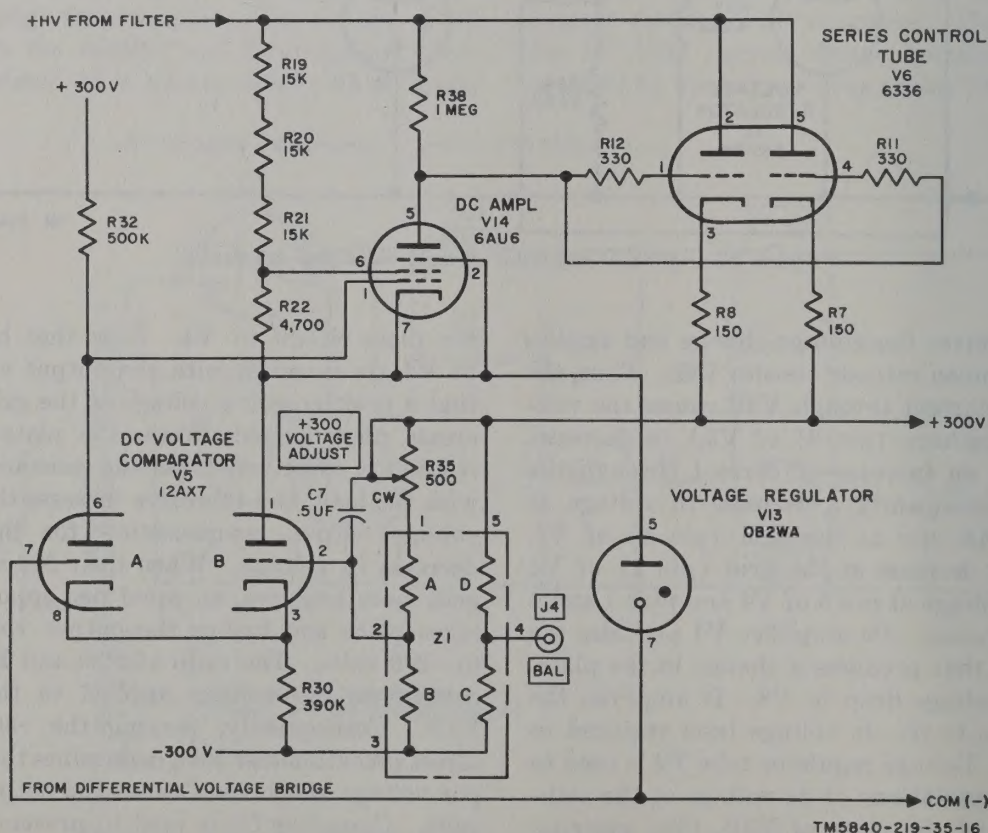


Figure 36. +300-volt regulator circuit, simplified schematic.

difference with respect to their common terminal. The +300 VOLTAGE ADJUST potentiometer R35 is used to set the +300-volt output to match the -300-volt output.

76. The +75-Volt Regulated Output (fig. 184)

The +75-volt regulated output circuit consists of voltage regulator V7 and resistors R25, R26, and R27. The +75-volt output voltage is derived from the +300-volt output. Regulator tube V7 is connected in series with R25, R26, and R27 to

the +300 V DC and COM $\pm$ terminals of TB1. The +75-volt side of V7 is connected to the +75 V DC terminal of TB1. Capacitor C8 provides additional filtering.

77. Ballast Tube Regulator Circuit (fig. 184)

Ballast tube RT1, in conjunction with variable resistor R28, is used to maintain heater elements of the dc amplifier V14 and dc voltage comparator V5 constant for variations in line voltage.

Section III. LOW VOLTAGE POWER SUPPLY

78. Voltage Regulator VR1 (fig. 37)

a. General. The fundamental circuit of the voltage regulator operates on the principle of ferro-resonance (*b* below). The regulator consists of a voltage stabilizer circuit and a frequency compensating circuit. The voltage stabilizer circuit regulates the output voltage to within the limits required to compensate for changes in input voltage between 105 and 130 volts. The frequency compensating circuit compensates for any change in output voltage caused by a change in supply frequency between 58 and 62 cycles.

b. Ferro-Resonance. The term ferro-resonance refers to a nonlinear resonant circuit employing a capacitor and an inductor with a saturable core. Operation equivalent to that of resonance is achieved by varying circuit voltage (or current) at a specified frequency to some critical value which causes the nonlinear inductance to have the correct value of reactance to resonate with the capacitor. At the point of resonance the current (or voltage) jumps abruptly to a much higher value.

c. Voltage Stabilizer Circuit (fig. 37). The basic stabilizer circuit consists of linear inductor T2 and nonlinear inductor T1 in parallel with capacitor C1. Inductor T2 is an autotransformer; a normal current flowing through section A induces a voltage in section B that adds vectorially to the input line voltage. The voltage drop across T2 increases or decreases, depending on the magnetizing current through section A. Nonlinear inductor T1 operates in the circuit in the saturation region above the knee of its magnetizing curve, but not far enough above to cause excessive losses and heating. Because T1 is operating in

saturation, any increase or decrease in voltage across the winding changes the inductance of the coil. This inductance change in the parallel circuit of T1 and C1 appears to section A of T2 as capacitive at normal and low line voltage, and as inductive at high line voltages. At voltages below those for which the stabilizer is designed, the T1 and C1 parallel circuit is capacitive, and draws a large magnetizing current which induces a large voltage across T2. This voltage adds vectorially to the low line voltage V_L and holds V_o constant. When V_L is higher than the specified limit, the T1-C1 parallel circuit is inductive, which decreases the magnetizing current flow through section A of T2. This decreases the voltage drop across T2 and transformer T3, which decreases the output voltage V_o . This basic stabilizer circuit has one disadvantage; it is also sensitive to frequency variations as it is to amplitude variations. When the line frequency is 62 cycles, the parallel circuit appears capacitive to the linear inductance, which appears as an increase in line voltage to T3. When the line frequency is 58 cycles, the parallel circuit appears inductive to the linear inductance and results in a decrease in line voltage to T3. Therefore, a frequency compensating circuit is required to compensate resulting for the increase and decrease in the voltage output of the stabilizer circuit when the line frequency varies.

d. Frequency Compensating Circuit (fig. 37). Inductor L1, capacitor C2, and transformer T3 constitute a frequency compensating circuit. At the nominal input frequency of 60 cycles, C2 and L1 are series resonant. When the input frequency increases from its nominal value to 62 cycles, the inductive reactance of L1 becomes greater than

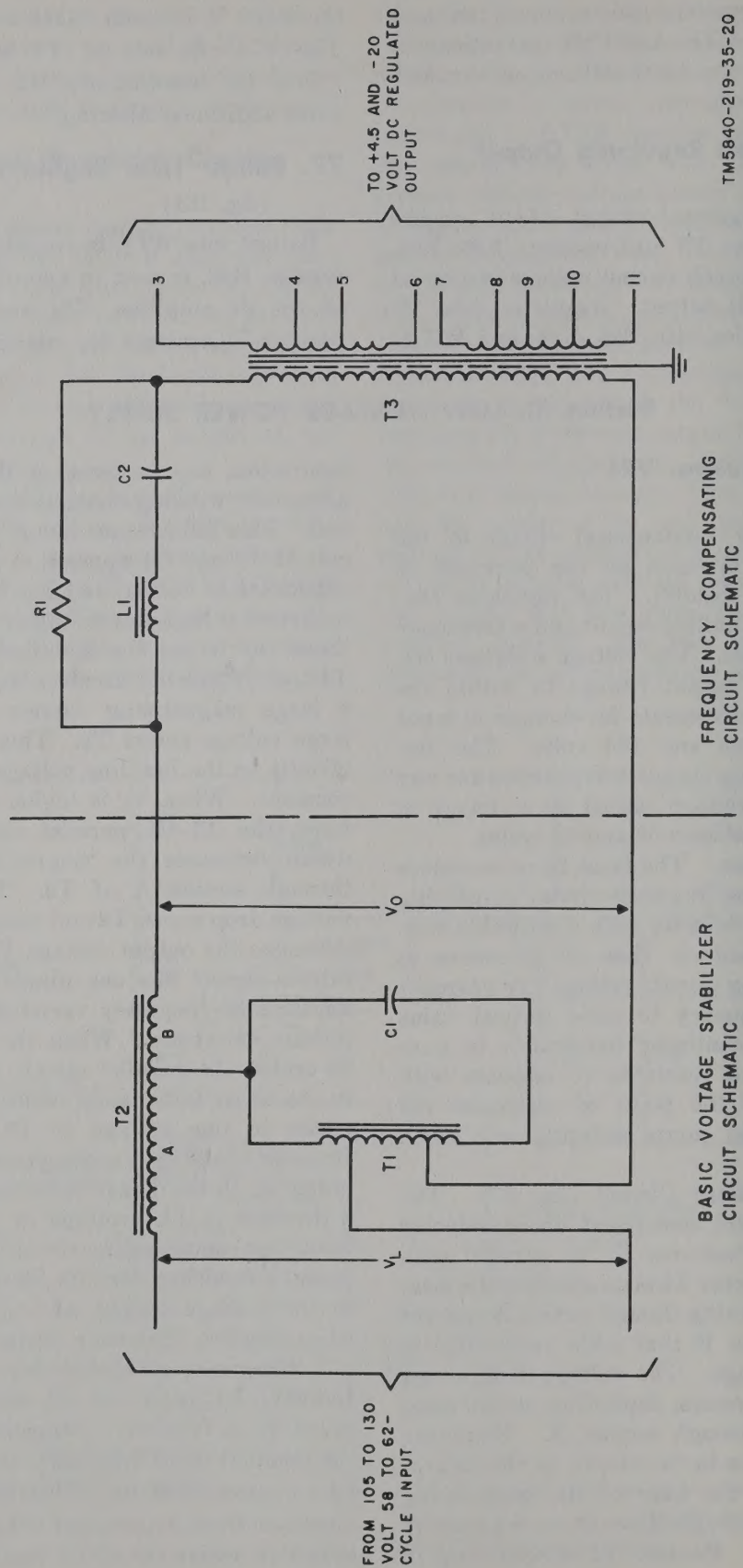


Figure 37. Voltage regulator, low voltage power supply, schematic.

the capacitive reactance of C2. This reduces the voltage across the primary of T3 as a result of the lagging current drawn by T3. This compensates for the increase in voltage out of the voltage stabilizer circuit because of the increase in input frequency. Conversely, when the input frequency drops below its nominal value to 58 cycles, the capacitive reactance of C2 becomes greater than the inductive reactance of L1, and the net reactance of C1 and L1 partially resonates with the inductive reactance of T3. This results in an increase in voltage across T3 and thus compensates for the drop in voltage out of the voltage stabilizer circuit due to the decrease in input frequency. The addition of the frequency compensating circuit sometimes causes instability resulting from subharmonic oscillations which are sustained in the voltage stabilizer and frequency compensating circuits. Resistor R1 is connected across L1 and C2 to suppress these oscillations.

79. The +4.5-Volt Rectifier

(fig. 38)

The secondary winding between terminals 4 and 6 of voltage regulator VR1 output transformer supplies regulated 6.4 volts rms to bridge rectifier CR1. The positive dc output appears at the red terminal (designated R) of the rectifier. The negative dc output appears at the black terminal (designated BK) of the rectifier. The

choke input filter, consisting of inductor L1 and capacitors C1 and C2, filters the rectifier output. Bleeder resistor R1, connected across the output of the choke input filter, limits the no-load voltage and protects the filter capacitors from insulation break-down. The 4.5-volt output of the filter is connected across the winding of relay K1, whose contacts are in series with the output of the -20-volt rectifier.

80. The -20-Volt Rectifier Circuits

(fig. 39)

The secondary winding between terminals 7 and 11 of voltage regulator VR1 output transformer supplies regulated 50 volts rms to full wave rectifier CR2. The negative 20-volt dc output is obtained at terminal 9 of the output transformer and the positive 20-volt dc is returned to the red terminal (designated R) of CR2. The choke input filter, consisting of inductor L2 and capacitors C3 through C10, filters the rectifier output. Bleeder resistor R2, connected across the output of the filter, limits the no-load voltage and protects the capacitors from insulation breakdown. The -20-volt output of the filter is connected to terminals 2 and 5 of relay K1. The winding, terminals 7 and 8 of K1, is connected across the 4.5-volt output. Connecting the 4.5-volt output to the energizing coil of K1 ensures that -20 volts cannot be applied to the data set in the absence

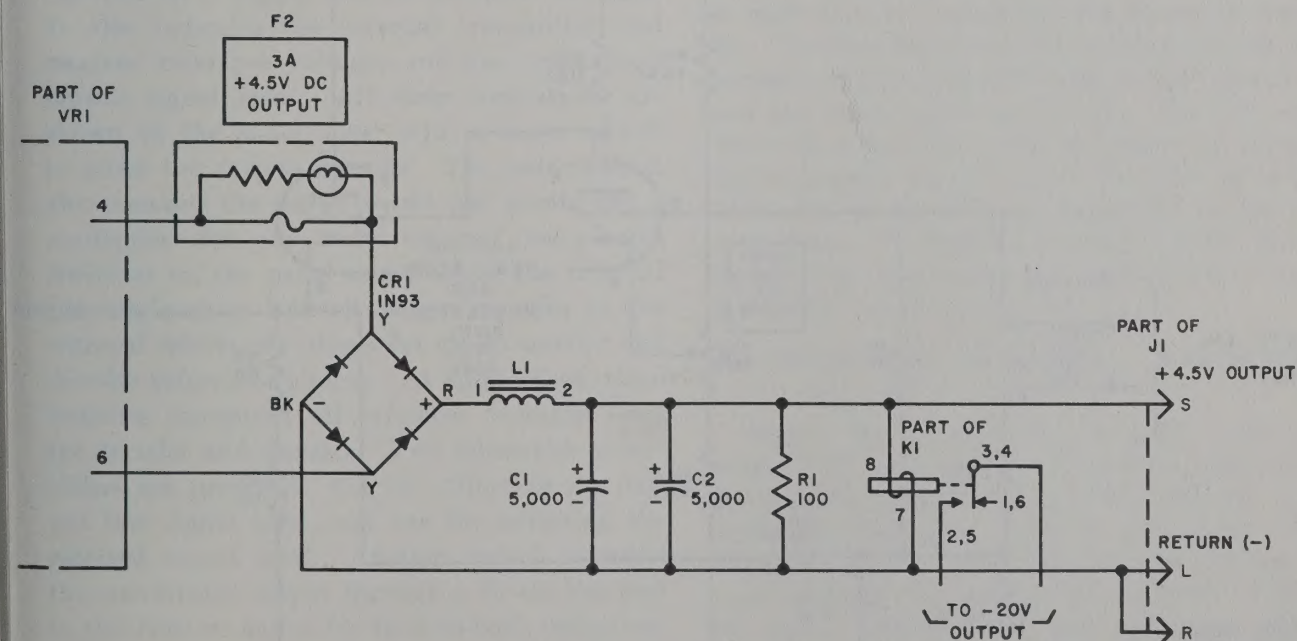


Figure 38. +4.5-volt rectifier circuit, simplified schematic.

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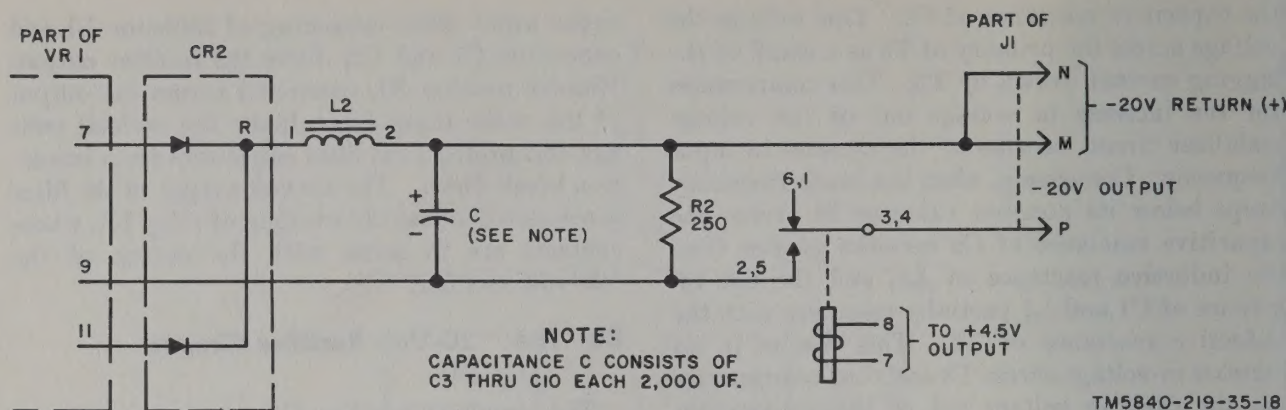


Figure 39. -20-volt rectifier circuit, simplified schematic.

of the 4.5-volt output. This is a protective measure to prevent damage to transistors in the data set.

81. The -70-Volt Lamp Supply (fig. 40)

a. The -70-volt circuit provides a regulated dc voltage with a superimposed half-wave sinusoidal voltage for firing and extinguishing the neon indicator lamps. These functions are performed by the triode 5687, V2. Section A, pins 1, 2, and 3, amplifies the dc voltage changes caused by load variations that appear across the voltage divider

network consisting of resistors R5 through R8, and the half-wave sinusoidal signal from the detector circuit consisting of rectifier CR3 and resistor R4. The output of section A controls section B, pins 6, 7, and 9. Section B acts as a shunt regulator that controls the dc level. Resistors R10, R3, and R9 comprise a voltage divider from -300 volts to ground and establish the cathode voltage and hence the gain of V2A. The gain of the stage is therefore dependent on the setting of the arm of the LAMP SUP ADJ VOLTS potentiometer R3. Grid bias for V2A is determined by the voltage divider network

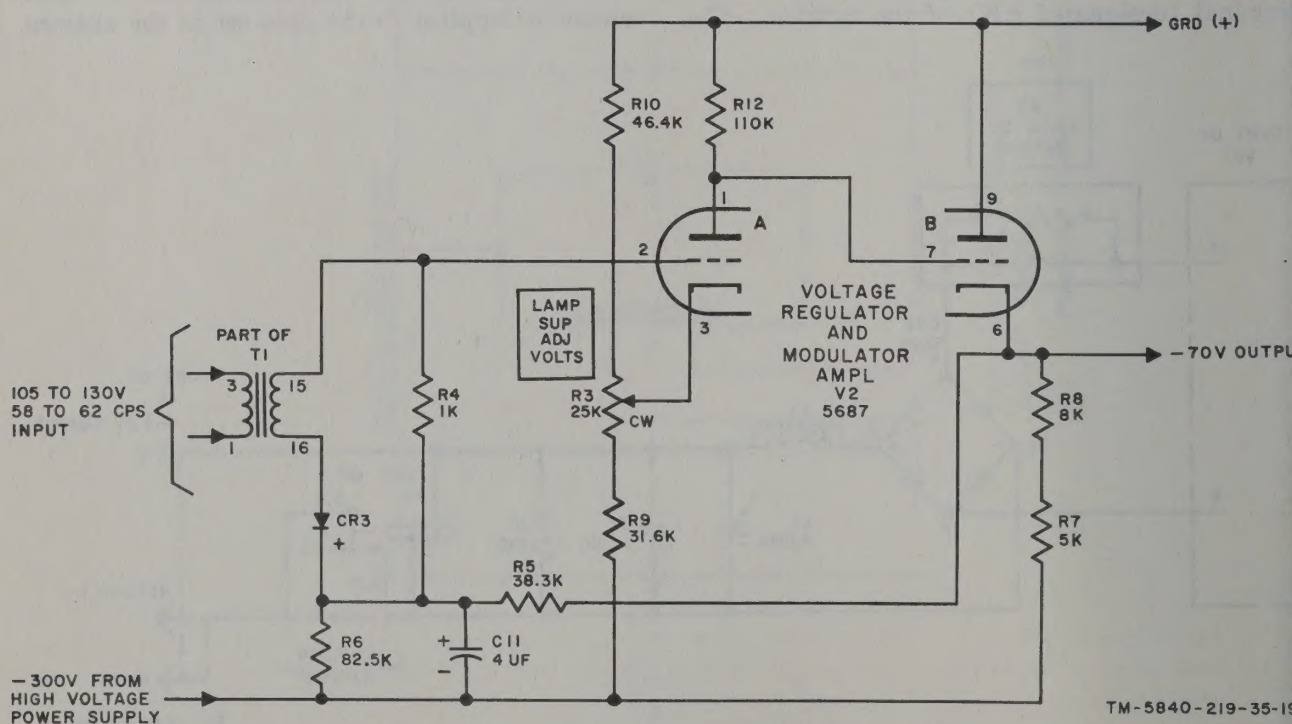


Figure 40. -70-volt circuits, simplified schematic.

consisting of the plate-to-cathode resistance of V2B, and R5 through R8, all of which are also connected to the -300-volt supply from the high voltage power supply. Any variation in the load at the -70-volt output causes a change in the voltage applied to the grid of V2A, which in turn controls the grid of V2B. If the load current increases, the voltage drop across V2B and the voltage divider network R5 through R8 decreases, causing the grid of V2A to go less negative. This drives the plate of V2A and consequently the grid of V2B more negative, thus increasing its plate-to-cathode resistance of V2B and restoring the output voltage to its original value. Conversely, a decreasing load current will act to decrease the resistance of V2B, thus again restoring the output voltage to normal.

b. The circuit, comprising the secondary winding (terminals 15 and 16) of transformer T1, rectifier CR3, and resistor R4, provides a half-wave sinusoidal signal to the grid pin 2 of V2A. The signal is then amplified and superimposed on the grid of V2B, changing the dc output grid

bias, and causing the output to vary between -62 volts and -80 volts at the supply line frequency.

82. The +150-Volt Regulated Circuit (fig. 181)

The +150-volt dc regulated output is furnished by voltage regulator tube V1 connected across the +300-volt input from the high voltage power supply through resistor R11. The characteristics of the OA2 regulator tube V1 are such that for any change in load current within the limits of 5 to 30 milliamperes the voltage drop across the tube remains constant at approximately 150 volts.

83. The 6.4-Volt Ac Unregulated Output (fig. 181)

The 6.4-volt ac outputs supply unregulated heater power for units of the data set. This power is obtained from three secondary windings of power transformer T1. The voltage at these terminals is .1 volt above the nominal 6.3 volts required for the heaters of the electron tubes in circuits of the data set. This allows for the small voltage drop in the wiring to the various units.

Section IV. TEST PANEL

84. General

The test panel provides means for measuring all the internal power supply voltages except the -70-volt lamp supply and the ac heater voltages. It also indicates the external transmitter and receiver reference voltages and the transmitter output signal level. All these indications are shown on the panel meter with a meter switch to select the various circuits. The meter switch also connects the meter to two test points and a multiplier for use with external test leads. Switches on the panel select either the internal plus and minus 300-volt power supplies or the external reference voltages for use as encoder and decoder reference voltages. At midposition, these switches disconnect all reference voltages from the encoder and decoder. Two adjustable attenuators are provided: one for adjusting the output line signal level, and one for adjusting the received signal level. Another switch connects the transmitter output through a 20-db loss pad to the receiver input for back-to-back operation. Isolation coils are provided for both the transmitting and receiving lines.

85. Meter Switch S1 (fig. 41)

Meter switch S1 has 10 active positions and an OFF position. The functions of the switch at each of the 11 positions are shown in figure 41. The drawing shows the switch positions, the contacts of S1A and S1B used in each position, and the panel markings for S1. On the same line with each switch position is shown a simplified schematic of the circuit for that position. Meter M1 has a full scale sensitivity of 200 microamperes. Diode CR1 is used to rectify the ac signals for measuring the transmitter output level with the dc meter.

86. 0-6V TEST Switch S6 (fig. 41)

Switch S6 (position 4), is used with test points TP1 and TP2 for connecting the meter for general purpose use as a dc voltmeter with full scale reading of either 6 volts or 30 volts. With the switch in the normal (not depressed) position, and meter switch S1 at 0-30V TEST, the meter reading is 30 volts full scale. With the switch depressed, the meter reading is 6 volts full scale.

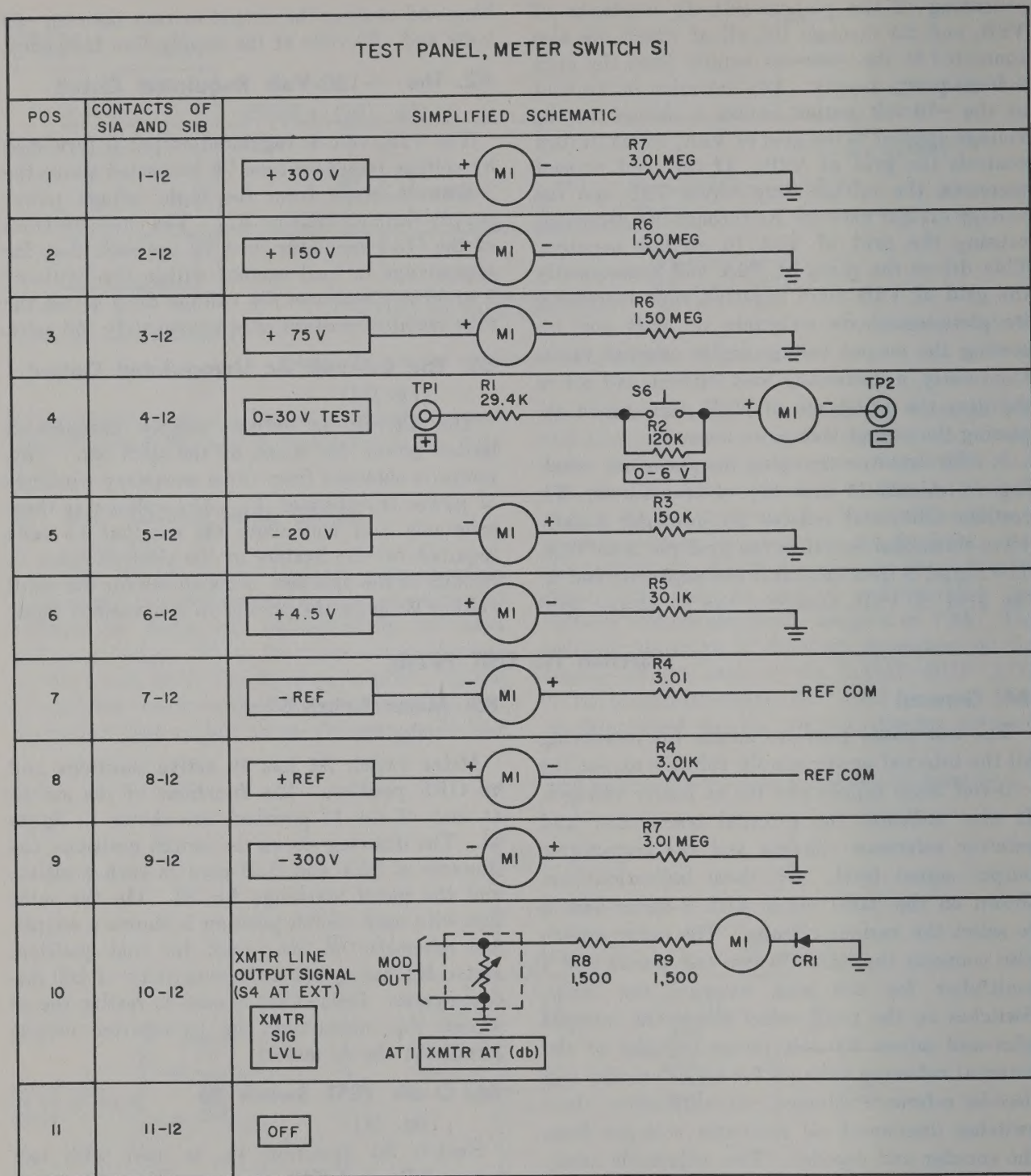


Figure 41. Test panel, meter switch S1, simplified schematic.

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87. ENC REF Switch S2 and DEC REF Switch S3 Circuits (fig. 42)

Switches S2 and S3, set in the EXT position, connect the positive and negative external ref-

erence voltage to the encoder and decoder, respectively. This is the position for normal operation. With these switches in the INT position, the external reference voltages are disconnected from the encoder and decoder, and the

positive and negative 300 volts from the data set high voltage power supply are connected as reference voltages. The switches are set in the center position to disconnect all reference voltages from the encoder and decoder.

88. REC LINE Switch S4 Circuits

(fig. 42)

Switch S4 connects the output of the transmitter either to the transmitter line or to the input of the receiver. When the switch is at the EXT position (E of fig. 42), the modulator (transmitter) is connected through adjustable attenuator AT 1, through part of S4, and through T1 to the transmitter line. The receiver line is connected through T2, AT2, and S4 to the amplifier synchronizer. In the LOCAL position (D of fig. 42), the modulator output is connected through AT 1, switch S4, the fixed 20-db pad, to the input of the amplifier synchronizer (receiver). Used this way, the transmitter and receiver can be tested together.

89. ENC REF—DEC REF Switch S5 Circuits (fig. 42)

Switch S5 connects either the external reference voltages or the internal reference voltages to meter switch S1 -REF and +REF positions.

90. REC LINE TP4

(fig. 42)

Test point TP4 is used as a convenient point to connect a VTVM (ac) or db meter when measuring the input signal level to the amplifier synchronizer. The meter should be connected from TP4 to chassis ground.

91. LOCAL XMTR LINE TP3

(fig. 42)

When the REC LINE switch S4 is at LOCAL, test point TP3 is used as a convenient point to connect a VTVM (ac) or db meter when measuring the modulator output level at the output of XMTR AT (db) attenuator.

Section V. PACKAGE DESCRIPTION

92. General

The nine basic package assemblies described in this section are of two types: bistable F/F circuits and monostable F/O circuits (app. III). Each package is identified as to type, whether F/F or F/O. Although all packages of the same type or identical, each of them may be triggered through different circuits built into it, not all of the available circuits being used for any one application. Similarly, output requirements for different applications vary, and not all output circuits are used for any one application. In each of the package descriptions which follows, the input and output circuits are described for the specific application being discussed; other inputs and outputs may be disregarded for the moment. All pulses referred to in the discussions, unless otherwise indicated, are actually negative with respect to ground (app. II). A "positive" pulse is a positive-going pulse and a "negative" pulse is a negative-going pulse. Schematic diagrams of all nine packages are shown in figure 133. The schematic drawing of the R/LC package is shown in figure 201.

93. Waveforms

(figs. 159(1)–159(10)).

Waveforms of the voltages appearing at terminals of the packages and of other important points of the data set are shown in figures 159(1) through 159(10). The waveforms illustrated are representative of typical circuits, but not every waveform of every terminal of the packages is shown. For example, a representative D package showing the output waveform for a typical package is shown, and it is understood that all other D packages having the same external circuits will have the same waveforms at the corresponding terminals. When checking a waveform at a terminal of a package not shown in the figure, refer to the package of the same kind which is shown, and use the representative waveform illustrated.

94. A Package

The A package is a bistable F/F switching circuit (app. III) and is used in the transmitter unit, the amplifier synchronizer, and the receiver unit. It is turned ON by a negative signal applied to the base circuit, and turned OFF by a

positive signal applied to the base circuit.

a. *Transmitter Unit RC F/F* (figs. 163(2), 133, and 159(2)). This package is a part of the transmitter unit and provides reset bias for the ring counters when it is in the ON condition. In this application the package is ON at all times except during TSG-57. At the end of TS 56 it receives a positive pulse from RT F/O which turns it OFF. This pulse is applied to the base of the transistor through terminal 10, L1, and R2. Two other input circuits are also used: terminal 5, where -12 volts is applied through R1 to back-bias CR1, and terminal 2, which carries clock pulses continuously and applies them to the cathode of CR1. Terminal 2 is also connected to terminal 6 so that when the package is OFF, the -17 volts at terminals 6 and 2 plus the negative clock pulse is great enough to overcome the -12 volts at terminal 5 and the +4.5 volts at the base received from the associated C package to turn the transistor ON. Two output circuits are used: terminal 3, which lights the indicator lamp, and biases the input gate to terminal 8 of RT F/O; and terminal 6 (externally connected to 2), which is approximately -2.5 volts when the circuit is ON and -17 volts when it is OFF. Terminal 1 is connected to -20 volts and the emitter is grounded at terminal 9.

b. *Transmitter Unit RTC F/F* (figs. 163(1), 133, and 159(2)). The RTC is an F/F circuit used to apply a positive-going pulse to the 600-cycle circuit of the modulator when the package is turned ON. The output to the modulator is taken from terminal 3 which is connected directly to the collector of the transistor. In this application there are three inputs. Positive bias is applied to the anode of CR1 through R1 and terminal 5. This allows the diode to pass the next negative clock pulse which is applied to the base through C1 and R2, turning the transistor ON. The transistor is turned OFF by a positive pulse applied at terminal 10 through L1 and R2 to the base. The positive pulse is of great enough duration to pass through L1. Terminal 1 is connected to -20 volts and terminal 9 is connected to ground.

c. *Transmitter Unit Shift Registers 1 through 13* (figs. 163(3), 133, and 159(2)). These are F/F circuits. Each one has a memory circuit connected to the input gate of the following stage. If the SR stage had been ON, its mem-

ory circuit would hold the input gate of the following stage open long enough for the next shift pulse to turn the following stage ON. If the SR stage had been OFF, the gate would be closed; thus at each shift pulse, the condition of each shift register stage is advanced until the data word has been shifted out to the modulator. In this application the terminals are connected to the circuits as follows: 1 is connected to -20 volts; 2 is connected to clock pulses; 3 is connected to the indicator lamp for SR 1 through SR 13 and is also the output to the modulator for SR 1; 4 and 9 go to ground; 5 is an input from the previous stage for SR 1 through SR 12, but is not used for SR 13; 6 is an output to the following stage for SR 2 through SR 13, but is not used for SR 1; 7 is an input requiring a clock pulse to turn the transistor ON; and 8 is an input for turning the transistor OFF by a set zero pulse. When the package is OFF, a positive bias on terminal 5 is required to bias diode CR1 to conduction through resistor R1. Under these circumstances the next clock pulse at terminal 2 passes through CR1 to the base through C1 and R2 and turns the transistor ON. When the positive set zero pulse is applied at terminal 8, diode CR2 allows it to pass directly to the base, turning the transistor OFF again. During the time the transistor is ON, the collector voltage is at -2.5 volts and discharges C2 to that voltage. Capacitor C2 is connected to the following stage through terminal 6 and maintains this potential long enough to open the gate of the following stage. A clock pulse applied at terminal 7 passes through R2 to the base, turning the transistor ON for an auxiliary digit for SR 1 through SR 10, or for the output from the binary counters for SR 1 through SR 13.

d. *Amplifier Synchronizer F/F No. 2* (figs. 170(2), 133, and 159(2)). This package supplies the receiver programmer and the reset control circuit with a receiver ready pulse in the form of an ON bias. Its OFF bias enables gates in the reset control and remote start circuits which require a negative voltage. Two inputs and one output are used. Terminal 1 has -20 volts connected through R3 to the collector; terminal 5 has -12 volts, which is a reverse bias for CR1; and terminal 9 grounds the emitter. A negative data pulse and a clock pulse are applied simultaneously at terminal 2. The combined voltage

of the two signals is greater than the -12-volt bias on CR1, allowing the clock pulse to pass through C1 and R2 to the base, turning the transistor ON. A positive reset pulse is applied at terminal 10 through R5-L1 and R2 to turn the transistor OFF.

e. Amplifier Synchronizer F/F No. 3 (figs. 170(2), 133, 159(2)). This circuit supplies the ON bias to the frequency divider and OFF bias to the divider reset circuit. The package has -20 volts applied to the collector through pin 1 and R3, and -12 volts applied to the anode of CR1 through R1, back biasing CR1. The emitter is grounded at terminal 9. The output at terminal 3 is connected to the collector directly and the potential there is -2.5 volts in the ON condition and -17 volts in the OFF condition. When the transistor is OFF, it applies a negative bias from terminal 3 to its own input at terminal 2, overcoming the back bias on CR1 at terminal 5. The next 6,000-pps pulse passes through CR1, C1, and R2 to the base, turning the transistor ON. The transistor is turned OFF by a positive pulse applied at terminal 10 through L1 to the base.

f. Amplifier Synchronizer F/F No. 5 (figs. 170(2), 133, and 159(2)). This package is used in the data sampling control circuit to produce regenerated auxiliary and data pulses based on receiver time slots. Three inputs and two outputs are used. A positive data signal is applied at terminal 5 which enables CR1 through R1. The receiver clock pulse at terminal 2 passes through CR1, C1, and R2 to the base, turning the transistor ON. A positive pulse on terminal 10 through L1-R5 and R2 to the base turns the transistor OFF. When the transistor is ON, it furnishes a positive bias at terminal 3. The collector receives -20 volts from terminal 1 through R3, and the emitter is grounded at terminal 9.

g. Amplifier Synchronizer F/F No. 6 (figs. 170(2), 133, and 159(3)). This package supplies ON bias to the ready control circuits and to the divider reset gates. Two inputs and one output are used. A negative pulse applied to terminal 2 passes through CR1 because terminal 5 is at ground potential and CR1 is not biased. The pulse passes through C1 and R2 to the base and turns the transistor ON. A positive bias at terminal 10 is applied to the base through L1-R5 and R2, turning the transistor OFF. When the transistor is ON, it applies positive bias to

terminal 3. The collector receives -20 volts from terminal 1 through R3, and the emitter is grounded at terminal 9.

h. Amplifier Synchronizer F/F No. 7 (figs. 170(1), 133, and 159(2)). F/F No. 7 is used to open the transmitter control gate. Two inputs and one output are used. The input at terminal 2 is a clock pulse and a negative bias. The negative bias puts a negative potential at the cathode of CR1 to overcome the -12 volts applied to the anode at terminal 5 through R1. The output at terminal 3 applies a positive bias to the transmitter start gate when F/F No. 7 is ON. The input at terminal 10 is a positive pulse which turns the F/F OFF. Terminal 9 is grounded, and the collector receives -20 volts bias from terminal 1 through R3.

i. Receiver Unit RC 1 F/F (figs. 172(1), 133, and 159(3)). This package controls the passage of clock pulses through the ring counter reset gates. Four inputs and two outputs are used. With the transistor turned OFF, a positive bias is applied at terminal 5, through R1, to enable CR1. A clock pulse at terminal 2 passes through CR1, C1, and R2 to the base, turning the transistor ON. An alternate enabling pulse is a negative pulse applied to terminal 7, where it passes through R2 to the base, turning the transistor ON. The F/F is turned OFF by a positive pulse at terminal 8. The collector receives -20 volts from terminal 1 through R3. Terminal 10 is connected to +4.5 volts, and the emitter is grounded at terminal 9. The output from the collector to terminal 3 lights the indicator lamp. The output through R4 to terminal 6 is a positive pulse.

j. Receiver Unit RC 2 F/F (figs. 172(1), 133, and 159(3)). This package opens the ring counter reset gates at the proper time. Two inputs and two outputs are used. Diode CR1 is biased at its anode by -12 volts from terminal 5 through R1. A negative pulse at terminal 2 from its own output terminal 6 through R12 overcomes the back bias and allows a clock pulse to pass through CR1, C1, and R2 to the base, turning the transistor ON. A positive pulse is applied to terminal 8 where it is passed by CR2 and applied to the base to turn the transistor OFF. A positive pulse from the collector appears on terminals 3 and 6 when the transistor goes ON. The emitter is grounded at terminal 9. The collector receives -20 volts from pin 1 through R3.

k. *Receiver Unit MS F/F* (figs. 172(1) and 133). This package biases the MS F/O which turns ON RT 1 F/F to reset the ring counters manually. Two inputs and two outputs are used. Terminal 9 is grounded, grounding the emitter. Terminal 5 is grounded, placing the anode of CR1 at ground potential. A negative pulse at terminal 2 passes through CR1, C1, and R2 to the base, turning the transistor ON. A positive pulse at terminal 10 passes through L1-R5 and R2 to the base, turning the transistor OFF. Terminal 3 is a positive output pulse from the collector to light the indicator lamp. Terminal 6 is a positive output pulse from the collector through R4.

l. *Receiver Unit PSR F/F* (figs. 172(2), 133, and 159(3)). This package stores serial parallax data (one digit at a time) and supplies the serial adder with this data at the proper time. There are four inputs and two outputs. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R3. The base is biased to +4.5 volts at terminal 10 through L1-R5 and R2. Positive bias from the previous SR stage is applied to the anode of CR1 through R1 at terminal 5. A negative pulse at terminal 2 passes through CR1, C1, and R2 to the base, turning the transistor ON. A negative clock pulse applied at terminal 7 also turns the transistor ON through L1-R5 and R2 to the base. A positive pulse at terminal 8 passes through CR2 to the base, turning the transistor OFF. When the transistor is turned ON, capacitor C2, having one side grounded at terminal 4 and the other side connected to the collector through R4, discharges to approximately -2.5 volts. When the transistor is turned OFF, C2 maintains this potential long enough to enable the gate of the next stage. Terminal 3 is a positive output to light the indicator lamp.

m. *Receiver Unit SPD F/F* (figs. 172(2), 133, and 159(3)). This package supplies bias to gate the shift pulse generator which supplies negative pulses for use as shift pulses for the shift register stages. Four inputs and two outputs are used. The collector receives -20 volts from terminal 1 through R3. The emitter is grounded at terminal 9. A positive pulse enables diode CR1 through terminal 5 and R1. A clock pulse passes through CR1, C1, and R2 to the base to turn the transistor ON. A clock pulse at terminal 7 through R2 to the base also turns

the transistor ON. The transistor is turned OFF by a positive pulse applied to the base through terminal 10, L1-R5, and R2. The output at terminal 3 controls the indicator lamp. The output at terminal 6 is a positive bias. Terminal 10 is biased to +4.5 volts through the associated C package.

n. *Receiver Unit OSD F/F* (figs. 172(2), 133, and 159(1)). This package is used in the off-scale detection circuits to shut off ALL DATA PRESENT control bias when the target is off-scale. In this application three inputs and two outputs are used. The emitter is grounded at terminal 9, and the collector receives -20 volts at terminal 1 through R3. Positive TSG voltage at terminal 5 is applied to the anode of CR1 through R1. The clock pulse applied at terminal 2 passes through CR1, C1, and R2 to the base, turning the transistor ON. The transistor is turned OFF by a positive pulse at terminal 10 to the base through L1-R5 and R2. The indicator lamp is triggered ON when the transistor is ON by the collector voltage through R4 to terminal 6. The output at terminal 3 is a positive pulse taken directly from the collector.

o. *Receiver Unit CS F/F* (figs. 172(2), 133, and 159(4)). This package supplies the carry signal for the serial adder. In this application the package has three inputs and one output. The emitter is grounded at terminal 9. The collector receives -20 volts from terminal 1 through R3. Terminal 5 is at -2.5 volts in the presence of parallax and data digits from the serial adder. This enables CR1 through R1, allowing a clock pulse at terminal 2 to pass through CR1, C1, and R2 to the base, turning the transistor ON. A positive pulse at the base at terminal 10 through L1-R5 and R2 turns the transistor OFF. Terminal 3 is an output direct from the collector of the transistor.

p. *Receiver Unit SR 1 through 13* (figs. 172(2), 133, and 159(4)). These SR stages receive parallax data in parallel and shift it serially to the serial adder. They also receive data serially from the serial adder and release it in parallel to the auxiliary and data lockups. Each has four inputs: a direct input at terminal 7 (not used for SR 12); a positive enabling bias at terminal 5 (not used for SR 13); a negative pulse at terminal 2 (not used for SR 13); and the set zero pulse at terminal 8. The collector output at terminal 3 lights the indicator lamp, and the

output at terminal 6 is stored in C2. The emitter is grounded at terminal 9, and the base is biased to +4.5 volts at terminal 10. The collector receives -20 volts from terminal 1 through R3.

95. B Package

The B package is a bistable F/F switching circuit (app. III) and is used in the transmitter and receiver units. It is turned ON by a negative signal applied to the base circuit, and turned OFF by a positive signal applied to the base circuit.

a. Transmitter Unit TC F/F (figs. 163(2), 133, and 159(1)). In this application the package, part of the clock pulse generator circuits, supplies control bias to the test control gate for recycling. The transistor is normally ON. Three inputs are used: a voltage from the -20-volt source is applied to terminal 7 which charges C2 through CR3 to terminal 10 which is connected to +4.5 volts. C2 is charged with the positive side connected to the base through L1 and R2. An external switch grounds terminal 7, discharging C2, driving the base positive, and turning the transistor OFF. Upon application of a TSG positive signal at terminal 6, diode CR2 is enabled through R15, and the next clock pulse at terminal 2 passes through CR2, C1, and R2 to the base, turning the transistor ON. The output at terminal 5 is about -17 volts when the transistor is OFF, and about -2.5 volts when the transistor is ON. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1.

b. Transmitter Unit Ring Counters (UR and TR) F/F (figs. 163(2), 133, and 159(4)). These stages are used as ring counters to produce time slot gates. Ten are units counters and six are tens counters, producing a maximum count of 60. There are four inputs and two outputs for each package. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. Terminal 10 is connected to +4.5 volts. A positive signal at terminal 6 through R3 enables CR2, allowing a clock pulse to pass through CR2, C1, and R2 to the base to turn the transistor ON. The transistor is reset to OFF by a positive pulse at terminal 4 through CR1 to the base. Terminal 8 is connected to terminal 7 of the preceding B package and to the lamp circuit. When the transistor is OFF, C2

of the preceding package charges until the base side is at a potential of +4.5 volts and the other side is at a potential of approximately -17 volts. When the transistor is turned ON, the potential at terminal 8 goes to -2.5 volts, turning the lamp on and causing C2 of the preceding package to discharge and apply a positive pulse to the base of the transistor through L1 and R2, turning the transistor OFF (see par. 106 for a description of the ring counter operation). Terminals 5 and 8 are connected directly to the collector.

c. Receiver Unit TC F/F (figs. 172(1), 133, and 159(1)). This package is part of the clock pulse generation circuits. It supplies control bias to the test control gate for recycling. In this application the operation is exactly the same as that described in *a* above.

d. Receiver Unit Ring Counters (UR and TR) F/F (figs. 172(2), 133, and 159(4)). These packages are used as ring counters to produce time slot gate voltages. Ten are unit counters and six are tens counters, producing a maximum count of 60. These stages are used in exactly the same way that the UR and TR stages are used in the transmitter unit (*b* above).

96. C Package

The C package is a monostable F/O circuit (app. III) and is used in the transmitter unit, the amplifier synchronizer, and the receiver unit. It is triggered ON by a negative pulse applied to the base, and returns to the OFF condition shortly after the cessation of the negative pulse. The output from terminal 3 is a positive-going pulse having an amplitude of 13 volts and a duration of 15 to 45 microseconds. This pulse extends into the positive region a few volts above ground, depending on the external voltages applied. The output at terminal 3 is a positive pulse. The C and L packages are identical except for the value of inductor L1, and for the duration of the output pulse. The output pulse for the L package has a duration of 4 to 7 microseconds.

a. Transmitter Unit RC F/O (figs. 163(2), 133, and 159(1)). This package turns off the reset control flip-flop (A package) at the end of each frame. In this application three inputs and one output are used. The emitter is grounded at terminal 9, and -20 volts is applied to the collector at terminal 1 through R1. Terminals 5 and 10 are connected to +4.5 volts. A positive

TSG voltage is applied to the anode of CR2 from terminal 7 through R3. A clock pulse at terminal 2 passes through CR2, C2, and R2 to the base, turning the transistor ON. The transistor also can be turned ON at other times by a negative pulse from terminal 8 through CR1 and R2 to the base. The output pulse at terminal 3 is formed in this manner: While the transistor is OFF, capacitor C1 is charged to about -17 volts at the collector side, and to +4.5 volts on the other side by the +4.5-volt supply at terminal 5 through CR3 in parallel with R4. When the transistor is triggered ON, the voltage at the collector rises to about -2.5 volts and the voltage at terminal 3 rises to about +18 volts and falls off to about +4.5 volts at the end of the pulse.

b. Transmitter Unit PFD F/O (figs. 163(2), 133, and 159(5)). This package generates one positive-going pulse for every other pulse applied to its associated F/F K package, thus dividing the 1,500 pps (par. 105c) by 2. Two inputs and two outputs are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. Terminal 5 is connected to -2.5 volts, and terminals 8 and 10 are connected to +4.5 volts. A negative pulse, gated in the associated K package (par. 100a) passes through CR2, C2, and R2 to the base to trigger the transistor ON. The output at terminal 3 is formed in the same manner as was done in the RC package (*a* above). The pulse amplitude is about 13 volts, but in this case it rises only to about +10.5 volts because of the -2.5 volts at terminal 5. The output from the collector appears at terminal 4.

c. Transmitter Unit ESP F/O (figs. 163(1), 133, and 159(5)). This package produces the encoder start pulse. In this application three inputs and one output are used. The emitter is grounded at terminal 9. The collector receives -20 volts from terminal 1 through R1. Terminal 10 is connected to +4.5 volts. A TSG is applied to terminal 7 which enables CR2 through R3. The clock pulse at terminal 2 passes through CR2, C2, and R2 to the base, triggering the transistor ON. At other times, clock pulses appear at terminal 8 through external gate circuits. These are applied to the base through CR1 and R2 to trigger the transistor ON. The output pulse at the collector appears at terminal 3 through C1. Terminal 5 is not used; consequently, CR3 and R4 are not used.

d. Transmitter Unit ERP F/O (figs. 163(1), 133, and 159(5)). This package produces the encoder reset pulse. The operation of the package for this application is identical to that of the ESP F/O described in *c* above.

e. Transmitter Unit RTC F/O (figs. 163(1), 133, and 159(5)). This package applies a reset pulse to the ready tone control flip-flop (A package). The operation of the package for this application is identical to that of the ESP F/O described in *c* above, except that only one input (terminal 2) is used, and for the output pulse at terminal 3. Terminal 5 is connected to +4.5 volts. While the transistor is OFF, capacitor C1 is charged to about -17 volts at the collector side, and +4.5 volts on the other side by the +4.5-volt supply at terminal 5 through CR3 in parallel with R4. When the transistor is triggered ON, the voltage at the collector rises to about -2.5 volts, and the voltage at terminal 3 rises to about +18 volts and falls off to about +4.5 volts at the end of the pulse.

f. Transmitter Unit BC 5 through 13 F/O (figs. 163(3), 133, and 159(6)). These packages are used as binary counters in the transmitter data processing section. Their operation is similar to that of the PFD F/O described in *b* above. Three inputs and two outputs are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. Terminal 5 is connected to -2.5 volts, and terminal 10 is connected to +4.5 volts. This package generates one positive-going pulse for every other pulse applied to its associated F/F K package, thus dividing the number of pulses by a factor of 2 for each BC stage. A negative pulse, gated in the associated K package (par. 100b) passes through CR2, C2, and R2 to the base to trigger the transistor ON. The output at terminal 3 is formed in the same manner as in the RC F/O package (*a* above). The pulse amplitude is about 13.5 volts, but in this case it rises only to about 11 volts because of the -2.5 volts at terminal 5. The output from the collector appears at terminal 4.

g. Amplifier Synchronizer F/O No. 1 (figs. 170(2), 133, and 159(6)). This package is part of the ready delay circuit. In this application one input and one output are used. Terminal 9 grounds the emitter, and -20 volts from terminal 1 through R1 is applied to the collector. Terminal 5 is grounded, and terminals 8 and 10 are

connected to +4.5 volts. Terminal 6 is connected to -12 volts, which biases CR2 heavily in the reverse direction. Two voltages are applied simultaneously to terminal 2: a negative bias and a negative 6,000-pps pulse. The combined amplitude of the two voltages exceeds the -12-volt bias on CR2, allowing the pulse to pass through CR2, C2, and R2 to the base, triggering the F/O ON. While the F/O is OFF, capacitor C2, connected from the collector to the cathode of CR3 and terminal 3, is charged on the collector side to about -16.5 volts, and on the CR3 side to ground potential through CR3 to terminal 5. When the F/O is triggered, the collector voltage rises to about -2.5 volts. The rise through C2 is a positive pulse output at terminal 3.

h. Amplifier Synchronizer F/O No. 2 (figs. 170(2), 133, and 159(6)). This package, part of the receiver ready control, supplies a set zero pulse to terminate the receiver ready pulse. One input and one output are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. Terminals 5, 8, and 10 are connected to +4.5 volts. Terminal 7 is connected to -12 volts, which biases CR2 heavily in the reverse direction. The input at terminal 2 is a negative bias occurring simultaneously with a 6,000-pps pulse. The combined voltage is great enough to overcome the -12-volt bias on CR2, allowing the pulse to pass through CR2, C2, and R2 to the base, triggering the F/O. The output pulse at terminal 3 is formed in the same way as the output pulse for RC F/O (*a* above).

i. Amplifier Synchronizer F/O No. 3 (figs. 170(2), 133, and 159(7)). In this application F/O No. 3 is part of the sync control circuit and supplies a set zero pulse to the reset F/F No. 3 (A package). The operation of the F/O is exactly the same as that of F/O No. 2 (*h* above).

j. Amplifier Synchronizer F/O No. 4 (figs. 170(2), 133, and 159(7)). This package supplies the delay F/F in the ready pulse generator with a set zero reset pulse. The operation of the F/O is the same as that of F/O No. 2 (*h* above), except that CR2 is biased to -12 volts at terminal 6 instead of terminal 7. Terminal 5 is grounded instead of being returned to +4.5 volts.

k. Amplifier Synchronizer F/O No. 5 (figs. 170(2), 133, and 159(1)). This package, part of the data sampling control, supplies the set zero to F/F No. 5 (A package). The operation of

this F/O is exactly the same as F/O No. 2 (*h* above).

l. Amplifier Synchronizer F/O No. 6 (figs. 170(2), 133, and 159(7)). In this application the package, part of the ready control circuit, supplies a set zero pulse to F/F No. 6 (A package). The operation of this F/O is the same as that of F/O No. 2 (*h* above), except that terminal 8 is an additional input which receives a negative pulse applied to the base through CR1, triggering the F/O, and terminals 5 and 10 are returned to +4.5 volts instead of to ground.

m. Amplifier Synchronizer F/O No. 7 (figs. 170(1), 133, and 159(7)). This package, part of the remote start control circuit, supplies a set zero pulse to F/F No. 7 (A package). The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. Terminals 5, 8, and 10 are connected to +4.5 volts. Two inputs and one output are used. A TSG is applied at terminal 7 which applies a positive bias to the anode of CR2 through R3. A clock pulse at terminal 2 passes through CR2, C2, and R2 to the base, triggering the F/O. Capacitor C1 is charged to -16.5 volts on the collector side and to +4.5 volts through CR3 on the other side. When the F/O is triggered, the collector voltage rises to -2.5 volts momentarily and passes a positive output pulse through C1 to terminal 3.

n. Amplifier Synchronizer BC 1, BC 2, and BC 3 F/O (figs. 170(2), 133, and 159(6)). In this application, the packages form a three-stage, 8:1 frequency divider, which produces 750-pps clock trigger pulses from the 6,000-pps pulses. The operation of these packages is identical to that described in *b* above.

o. Receiver Unit MS F/O (figs. 172(1) and 133). This package produces a single manual start pulse to assure that the ring counters receive ring start pulses. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. Terminals 5, 8, and 10 are connected to +4.5 volts. Two inputs and one output are used. A positive signal at terminal 7 is applied to the anode of CR2 through R3. A clock pulse at terminal 2 passes through CR2, C2, and R2 to the base, triggering the F/O. The output at terminal 3 is formed in the same way as described in *a* above.

p. Receiver Unit RC 1 F/O (figs. 172(1), 133, and 159(7)). RC 1 F/O, part of the start-stop

control circuit, supplies a set zero pulse to turn OFF F/F No. 1 (A package) after the ring reset gates are opened. One input and one output are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. Terminals 8 and 10 are connected to +4.5 volts, and terminal 5 is connected to -2.5 volts. Diode CR2 is biased heavily in the reverse direction by -12 volts from terminal 7 through R3. The input at terminal 2 is a negative signal voltage and a clock pulse whose combined amplitude is great enough to pass the clock pulse through CR2, C2, and R2 to the base to trigger the F/O ON. The output pulse at terminal 3 is formed in the same way as described in *g* above, except that terminal 5 is returned to -2.5 volts instead of to ground.

q. Receiver Unit CCS F/O (figs. 172(2), 133, and 159(1)). In this application CCS F/O resets the carry storage F/F for the serial adder. There are two inputs and one output used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. Terminals 5 and 10 are connected to +4.5 volts, and terminal 7 is connected to -15 volts. A large amplitude negative pulse at terminal 2 is applied through CR2, C2, and R2 to the base, overcoming the bias on terminal 7 and triggering the F/O. A negative pulse, biased to +4.5 volts through an external gate, also triggers the F/O at terminal 8. Capacitor C1 is charged to about -16.5 volts on the collector side and +4.5 volts through CR3 to terminal 5 on the other side. The pulse at the collector appears at terminal 3 with an amplitude of 13 volts, starting from +4.5 volts.

r. Receiver Unit OSD F/O (figs. 172(2), 133, and 159(1)). This package, part of the off-scale detection circuit, supplies a set zero pulse to the off-scale data F/F (A package). Three inputs and one output are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. A TSG is applied at terminal 7 to the anode of CR2 through R3. A clock pulse from terminal 2 is applied to the base through CR2, C2, and R2, triggering the F/O. Clock pulses at different times applied to the base from terminal 8 through CR1 also trigger the F/O. The output at terminal 3 is the same as CCS F/O (*q* above).

s. Receiver Unit SPD F/O (figs. 172(2), 133,

and 159(1)). The SPD F/O is part of the advance pulse control circuit that supplies the shift registers with shift pulses. Also it supplies the SPD F/F with set zero pulses. Terminal 1 is connected to -20 volts, terminals 5 and 10 are connected to +4.5 volts, and terminal 9 is ground. Three inputs and one output are used. At TS 10 the gate voltage is applied at terminal 7 through R3 to enable diode CR2. A clock pulse then passes through CR2, C2, and R2 to trigger the F/O. At other time slots clock pulses are applied at terminal 8 through CR1 and R2 to the base. Since CR1 is not biased, the clock pulses pass through to trigger the F/O. The output pulse at terminal 3 is formed in the same way as described in *b* above.

97. D Package

The D package is a bistable switching circuit (app. III) and is used in the transmitter and receiver units to energize certain relays. It is turned ON by a negative pulse applied at the base circuit and turned OFF by a positive pulse applied at the base circuit. The output at terminal 6 for all applications is externally connected to a negative voltage supply through the relay winding. When the transistor is turned ON, the collector-to-emitter resistance is reduced, increasing the current through the transistor and the external relay. This causes the relay armature to operate through external circuits, described in paragraph 112.

a. Transmitter Unit HRLU, XRLU, YRLU, and ECRLU F/F (figs. 163(1), 133, and 159(7)). The first three of these packages control the on-off time of the three multiplexing relays, and the ECRLU F/F controls the on-off time of the earth curvature relay. These four applications are identical. Three inputs and two outputs are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R5 and R4. A TSG, applied at terminal 5 through R1 to CR1, allows a clock pulse to pass through CR1, C1, and R2 to the base, turning the transistor ON. A positive pulse at terminal 8 through CR2 to the base turns the transistor OFF. The output at terminal 6 operates the external relay (par. 112), and the output at terminal 3 turns on the indicator lamp.

b. Receiver Unit DLU 1 through 9 F/F (figs. 172(3), 133, and 159(1)). These packages energize data relays when ON. Three inputs and

two outputs are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R5 and R4. Terminal 10 is connected to +4.5 volts. Positive bias voltage is applied to the anode of CR1 from terminal 5 through R1. A clock pulse at terminal 2 passes through CR1, C1, and R2 to the base, where it turns the transistor ON. A positive pulse to the base from terminal 8 through CR2 turns the transistor OFF. The output at terminal 6 operates the external relay. The output at terminal 3, direct from the collector, turns the indicator lamp on.

c. Receiver Unit DLU 10 F/F (figs. 172(3), 133, and 159(1)). DLU 10 F/F is also a data lockup unit. This application is the same as the other DLU's (*b* above), except that terminal 7 is another input. A clock pulse at terminal 7 is applied to the base through R2, turning the transistor ON.

d. Receiver Unit ALU 1 through 10 F/F (figs. 172(3), 133, and 159(1)). These packages energize auxiliary data relays when ON. The application is exactly the same as the DLU 1 through 9 (*b* above).

e. Receiver Unit ECC F/F (figs. 172(3), 133, and 159(1)). This package energizes the earth curvature relay when ON. Three inputs and two outputs are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R5 and R4. Terminal 10 is connected to +4.5 volts. A TSG at terminal 5 applies a positive bias to the anode of CR1 through R1. A clock pulse at terminal 2 passes through CR1, C1, and R2 to the base, turning the transistor ON. A positive signal at terminal 8 is applied to the base through CR2 to turn the transistor OFF. The output at terminal 6 operates the external relay; the collector output through terminal 3 turns on the indicator lamp.

f. Receiver Unit SLU HG, SLU HF, SLU XG, SLU XF, SLU YG, and SLU YF F/F (figs. 172(3), 133, 159(8), and 182(9)). These packages energize storage relays when ON. For each package three inputs and two outputs are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R5 and R4. A positive bias is applied to the anode of CR1 from terminal 5 through R1. A clock pulse from terminal 2 passes through CR1, C1, and R2 to the base, turning the transistor ON. A positive signal applied to

the base from terminal 8 through CR2 turns the transistor OFF. The output from the collector appears at terminal 3 and controls the indicator lamp. The output from terminal 6 controls the external relay (par. 112).

g. Receiver Unit FLU F/F (figs. 172(3), 133, and 159(8)). FLU F/F energizes the feedback relay when ON. Three inputs and one output are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R5 and R4. Terminal 10 is connected to +4.5 volts. A positive signal is applied to the anode of CR1 through R1, and a clock pulse at terminal 2 passes through CR1, C1, and R2 to the base to turn the transistor ON. A positive signal applied to the base from terminal 8 through CR2 turns the transistor OFF. The output appears at terminal 6 through R3.

98. E Package

The E package is a monostable F/O used primarily as a regenerative pulse amplifier. The input is a negative signal at the base to trigger it ON. The output at terminal 7 from differentiating transformer T1 is a negative pulse with an amplitude of approximately 8 volts and a duration of 1.5 microseconds. Diode CR4 dissipates the overshoot at the trailing edge of the collector output pulse. R3 provides a return circuit to ground when terminal 6 is not used. Capacitor C1 is a dc blocking capacitor. CR3 and CR5 limit the amplitude of the output pulse at terminal 7 to the external voltage applied at terminal 3.

a. Transmitter Unit CP 1 and CP 2 F/O (figs. 163(1), 133, and 159(1)). These packages, part of the clock pulse generation circuits, produce clock pulses 1 and 2. One input and one output are used on each package. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R2. Terminal 3 is connected to -10.5 volts, and terminals 8 and 10 are connected to +4.5 volts. A negative pulse is applied to the base from terminal 2 through C2 and R1 to trigger the F/O. The negative pulse output appears at terminal 7. This pulse is generated at the collector as a positive pulse and is inverted by transformer T1.

b. Transmitter Unit SRC F/O (figs. 163(3), 133, and 159(8)). This F/O provides read-in pulses for the SR stages at selected times during the message frame. One input and one output

are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R2. Terminal 5 is connected to -2.5 volts. Terminals 8 and 10 are connected to +4.5 volts. A clock pulse applied to the base from terminal 2 through C2 and R1 triggers the F/O. The output at terminal 7 is the same as described for CP 1 and CP 2 F/O in *a* above.

c. Receiver Unit CP 1, CP 2, and CP 3 F/O (figs. 172(3), 133, and 159(1)). These packages are part of the clock pulse generation circuits. They produce clock pulse outputs 1, 2, and 3. The operation for this application is identical to that described in *a* above.

d. Receiver Unit SPG F/O (figs. 172(3), 133, and 159(1)). The function of the SPG F/O is to reinforce the SR shift pulses. The operation for this application is identical to that described in *b* above, except that C2 inside the package is used with an external diode and resistor to form the gate for terminal 2.

e. Receiver Unit, Pulse Amplifier (figs. 172(2), 133, and 159(1)). The function of this package is to amplify the clock pulses from the serial adder for use by associated equipment. The operation is the same as that of *b* above, except that terminal 3 is connected to -10.5 volts, making CR 3 and CR 5 clamping diodes to clamp the output at terminal 7 to -10.5 volts.

99. J Package

The J package, a monostable F/O, produces a single pulse which is initiated by the operation of an external switch connecting terminal 7 to either terminal 10 or ground. It has one input and one output. The output at terminals 8 and 3 is transformer-coupled from the collector circuit. It is a pulse, negative at terminal 3, having an amplitude of 10 volts.

a. Transmitter Unit SP F/O (figs. 163(2) and 133). In this application, the package produces a pulse for performance check purposes. The emitter is connected to ground at terminal 9, and the collector receives -20 volts from terminal 1 through R2 and R4. Terminal 8 is connected to -2.5 volts, and terminal 7 is connected to +4.5 volts. The external switch S4 is connected so that in the normal position terminals 7 and 10 are connected together. Depressing S4 connects terminal 7 to ground and causes C1 to start charging to an amount determined by the voltage divider action of R1 and R5 from -20

volts to ground. The charging current is divided between R1 and R5 with most of it going through R1. This causes a voltage drop across R1 with the base end positive. As C1 charges, the charging current decreases, decreasing the voltage drop across R1 with an increasingly larger percentage of the charging current going through R5 from the -20-volt supply. When the charge on C1 reaches 4.5 volts (putting the base of the transistor at ground potential), all of the charging current comes from the -20-volt supply and is accompanied by another current going through R1 to ground, making the base end of R1 drop into the negative region. This negative potential increases to about -.5 volt, turning the transistor ON. When switch S4 is released, terminal 7 again is connected to +4.5 volts, and C1 discharges toward about +.5 volt, with the discharge current through R1 decreasing until the base becomes positive 4 volts, turning the transistor OFF. Terminal 8 being connected to -2.5 volts sets the level for the most positive point of the output pulse.

b. Receiver Unit SP F/O (figs. 172(1) and 133). This package produces a pulse for performance check purposes. The operation for this application is the same as that described in *a* above.

c. Receiver Unit MS PG F/O (figs. 172(1) and 133). This package produces a single pulse for manual start. The operation for this application is the same as that described in *a* above, except that terminal 8 is connected to -2.5 volts instead of ground. The effect of this is to make the output pulse at terminal 3 more negative by 2.5 volts.

100. K Package

The K package is a bistable F/F switching circuit used as a part of the binary counter circuits and as a pulse frequency divider in the transmitter and receiver units. The transistor is turned ON by a negative signal applied to the base, and turned OFF by a positive signal applied to the base. Transformer T1 couples pulses from terminals 4 and 8 to terminals 2 and 3. This package is always used in association with either a C or L package (pars. 96 and 101). The -12 volts at terminal 4 of the K package prevents the collector of the C or L package from being more negative than -12 volts because of CR5 in those applications where the collector of

the C or L package is connected to terminal 8 of the succeeding K package. R6 and C2 of the K package pass the positive pulse from the C or L package, because CR5 is disabled for a pulse more positive than -12 volts. CR3 is part of the gate circuit for the associated C or L package (pars. 96 and 101). CR2 becomes back biased when a positive reset pulse is applied to the base from terminal 5 through CR1, thus inserting R5 in the circuit. Capacitor C1 is a dc blocking capacitor.

a. Transmitter Unit BC 1 F/F (figs. 163(3), 133, 159(9), and 159(10)). This BC is used as a binary counter first stage in data processing. Three inputs and two outputs are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R1. Terminal 10 is connected to +4.5 volts, terminal 3 is connected to -2.5 volts, and terminal 8 is grounded for single scale operation. BC 1 is not used for double scale operation. A negative pulse applied at terminal 4 of the package induces a negative pulse at terminal 3 of transformer T1. This negative pulse is applied to the base through CR6, C1, and R5, turning the transistor ON. The ON bias at terminal 6 from the collector through R4 passes through a diode in the associated package, back to terminal 2, enabling CR3. The next pulse applied to terminal 4 has no effect on the K package transistor since it is already ON, but it passes through T1 and CR3 and triggers the associated package. The positive pulse from the associated package is applied to the base of the transistor in the K package from terminal 5 through CR1, turning the transistor OFF. The K package is left either ON or OFF, depending on whether the total number of pulses applied to terminal 4 is an odd or an even number.

b. Transmitter Unit BC 2 through BC 13 F/F (figs. 163(3), 133, and 159(9)). These packages are used as binary counters in transmitter data processing. This application is identical in operation to that described in *a* above, except for one difference. In this application the input pulse is positive instead of negative; consequently, in order to correct for this, and have the circuit work the same, the input pulse is applied at terminal 8 instead of terminal 4. Terminal 4 is returned to -12 volts for BC 3 through 13. Terminal 8 of BC 2 is the input during single scale operation and terminal 4 is the input during

double scale operation. During single scale operation terminal 4 of BC 2 is returned to -12 volts.

c Transmitter Unit PFD F/F (figs. 163(2), 133, and 159(9)). This package is used as a pulse frequency divider in conjunction with the C package. The operation of the package is identical to that described in *a* above.

d. Amplifier Synchronizer BC 1, BC 2, BC 3 F/F (figs. 170(2), 133, and 159(9)). In conjunction with three C packages, these packages are used to comprise an 8:1 frequency divider to produce 750-pps clock trigger pulses. The operation of these packages is identical to that described in *a* above.

101. Transmitter Unit L Package, BC 1 Through BC 4

(figs. 163(3), 133, and 159(9))

The L package is identical to the C package described in paragraph 96 and is used in the same way. The only difference is in the value of L1, which is lower than the equivalent inductance used in the C package. The lower value inductance in the L package results in a shorter ON time, and consequently a shorter output pulse.

102. M Package

The M package is a monostable F/O circuit (app. III). It is triggered by a negative pulse applied to the base. There are two outputs: one at terminals 4 and 6, which is positive at terminal 6 and lasts for 40 microseconds; and a negative pulse from terminal 8 which has an amplitude of 7.5 volts and lasts about 1.5 microseconds.

a. Transmitter Unit CLR F/O (figs. 163(1), 133, and 159(1)). CLR F/O supplies a clearing pulse to the multiplexing and earth curvature lockups (D packages). Two inputs and one output are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R4. Terminal 4 is connected to -.5 volt, terminal 10 to +4.5 volts, and terminal 3 to -12 volts. A TSG enables CR1 from terminal 5 through R1, allowing a clock pulse to pass through CR1, C1, and R2 to the base, triggering the transistor ON. When the transistor goes ON, the current through L1 and R5 develops a negative voltage at the base. When the clock pulse ceases, the transistor remains ON for a length of time determined by L1 and R5. Diode CR2 prevents the base of the transistor from

going more positive than +4.5 volts when the field of L1 collapses. In the OFF condition the collector is at a potential of about -17 volts. C2 is charged to -20 volts on one side through R3, and to -12 volts through T1 primary to the -12 volts at terminal 3. When the transistor is turned ON, the collector impedance drops suddenly. There is a sudden current flow from -12 volts through the primary of T1, C2, and CR4 to the collector, inducing a pulse across the secondary of T2 and at terminals 6 and 4. Since terminal 6 is positive, no current flows through R6 and CR3, but at the end of the pulse the field of T1 collapses, the voltage across the secondary is dissipated in CR3 and R6, and the voltage across the primary is dissipated in CR5. This output pulse has a duration of 40 microseconds.

b. Transmitter Unit SZ F/O (figs. 163(2), 133, and 159(1)). This package, part of the clock pulse generation circuits, produces a shift register set zero pulse. It also triggers an E package to produce CP 1. Two inputs and two outputs are used. The emitter is grounded at terminal 9, and the collector receives -20 volts from terminal 1 through R4. Diode CR1 is back biased by -2.5 volts from terminal 5 through R1. A negative pulse, which is biased at -2.5 volts by an external circuit, passes through CR1, C1, and R2 to the base, triggering the transistor ON. The circuits from the base to terminal 10 and the output circuits to terminal 6 are identical to those described in *a* above. The output at terminal 8 is a negative pulse of 7.5 volts amplitude which is delayed 40 microseconds after the transistor is triggered ON. When the transistor is ON, the collector voltage, and the potential at terminal 8 rises to -2.5 volts as C2 charges. When the transistor in the M package goes OFF, the voltage from the collector and terminal 8 of the M package and terminal 2 of the E package goes in the negative direction and is differentiated by C2, R1, and L1 of the E package to form a negative pulse to trigger the E package (par. 98a).

c. Transmitter Unit TRR F/O (figs. 163(2), 133 and 159(1)). In this application the package produces reset pulses for the tens ring counters. One input and one output are used. This output is at terminal 6 and is the same as described in *a* above. The input at terminal 2 is a negative bias and a negative clock pulse, the sum of the two having an amplitude great enough to

overcome the -12-volt bias on CR1 from terminal 5 through R1, and to pass the clock pulse through CR1, C1, and R2 to the base, triggering the F/O. Other circuits are as described in *a* above.

d. Transmitter Unit URR F/O (figs. 163(2), 133, and 159(1)). The operation of this stage is identical to that described in *c* above.

e. Receiver Unit SZ F/O (figs. 172(1), 133, and 159(1)). This package is part of the clock pulse generation circuits. It produces a set zero pulse and also triggers an E package that produces CP 1. The operation of this stage is identical to that described in *b* above.

f. Receiver Unit TRR F/O (figs. 172(1), 133, and 159(1)). TRR F/O produces the tens ring counter reset pulse. The operation of this stage is identical to that described in *c* above, except that the input gate is enabled by a positive voltage at terminal 5.

g. Receiver Unit URR F/O (figs. 172(1), 133, and 159(1)). This unit produces the units ring counter reset pulse. The operation of this stage is identical to that described in *f* above.

h. Receiver Unit DLR F/O (figs. 172(3), 133, and 159(1)). DLR F/O produces the data lock-up release pulse. The operation of this stage is the same as that described in *a* above, except that the input is a clock pulse from terminal 7 through R2 to the base, triggering the F/O.

i. Receiver Unit ALR F/O (figs. 172(3), 133, and 159(1)). In this application the package produces the auxiliary lockup release pulse. The operation of this stage is identical to that described in *a* above.

j. Receiver Unit SLR F/O (figs. 187(3), 149, and 174(1)). SLR F/O produces a release pulse for the three storage lockup units. The operation of this stage is identical to that described in *a* above.

103. Receiver Unit R/LC

(figs. 201, 172(2) and 133)

This package acts as a clock pulse gate circuit. The input at terminal 6 is the slant coordinate data received from the associated equipment. This data appears as a ground level or a -6-volt bias, depending upon the sense of the digit (ONE or ZERO). A digit ONE causes Q1 to conduct and lowers the potential of the collector from -20 volts to less than -2.5 volts, thus enabling diode CR2. With diode CR conducting, a clock pulse passes through C1 and to the shift register as a ONE.

CHAPTER 7

THEORY—TRANSMITTER

Section I. PROGRAM GENERATOR

104. Block Diagram

(fig. 43)

The transmitter program generator comprises five principal circuits which provide timing for all transmitter functions required to build up the digital message frame. Figure 82 is a timing diagram for these functions and other transmitter functions described in this chapter. The following are the principal circuits of the program generator: (1) Clock pulse generator circuits, (2) ring counter circuits and time slot gates, (3) reset circuits, (4) ready tone control circuits, and (5) encoder control circuits. These circuits are all shown in figure 43.

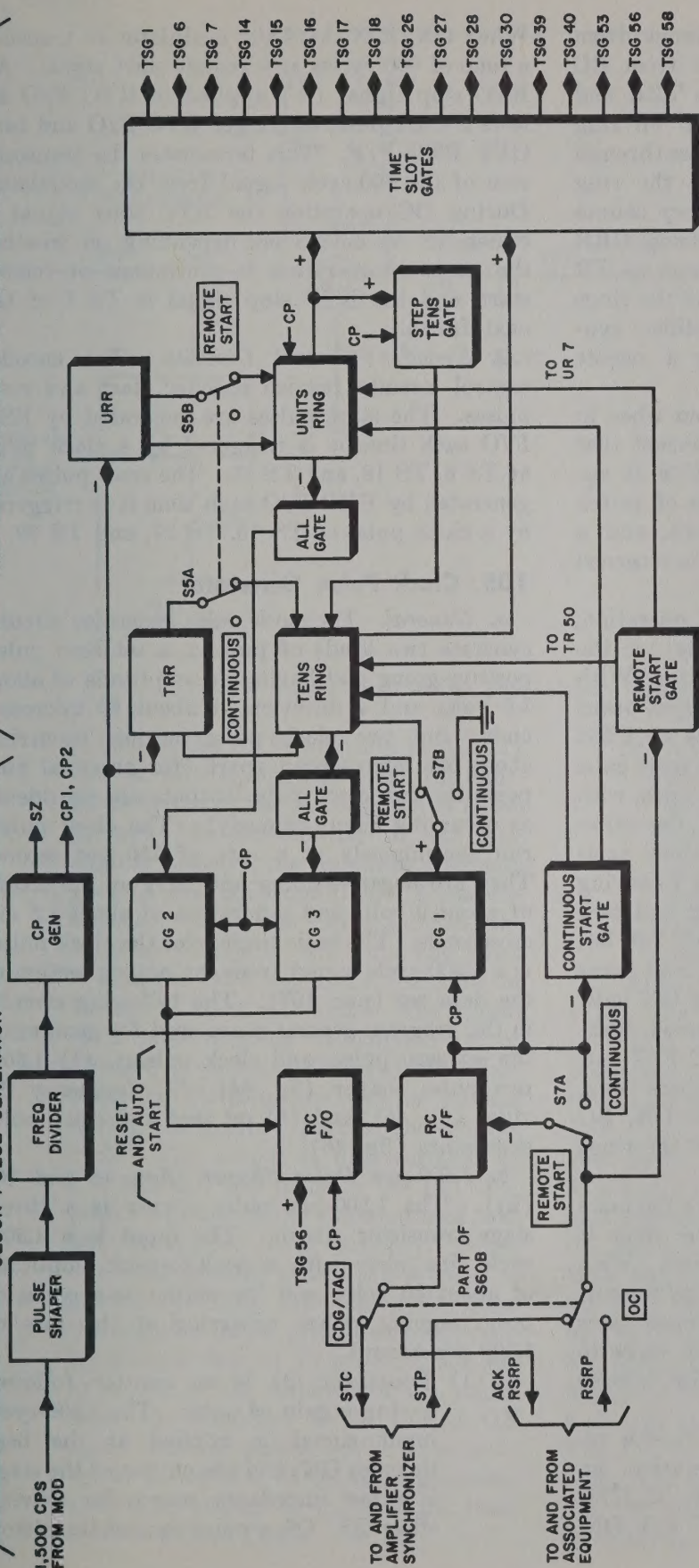
a. Clock Pulse Generator Circuits. The clock pulse generator circuits develop the clock pulses and the set zero pulses. The clock pulses are nine-volt, negative-going, $1\frac{1}{2}$ -microsecond pulses, and the set zero pulses are 3.5-volt, positive-going, 40-microsecond pulses. The 1,500-cycle output from the modulator is applied to the pulse shaper where the sine wave is converted to a rectangular wave. The shaped wave is then divided by one frequency divider stage where the 750-pps output is applied to the clock pulse and set zero pulse generators. Clock pulses are distributed to various circuits throughout the transmitter and to the associated equipment, and the set zero pulses are sent to the shift registers. The clock pulse generator runs continuously.

b. Ring Counter Circuits and Time Slot Gates. The ring counter circuits are composed of six tens ring stages and 10 units ring stages. Each ring is made up of transistor bistable stages. Each stage is turned ON by a clock pulse passed through its input gate. The input gate of a ring stage is opened by the positive output of the preceding stage. At the instant a stage is turned ON, it sends a pulse back to the preceding stage

to turn the preceding stage OFF. Assume the first stage of a ring, UR 0, is ON. Its output opens the gate to UR 1. The next clock pulse turns on UR 1 which sends a pulse to UR 0 to turn OFF UR 0. The output of UR 1 now opens the gate to UR 2, the next clock pulse turns on UR 2, and UR 2 send a pulse back to turn OFF UR 1. In this way the ring progresses through UR 9 and UR 0 again, until at some time, all the stages of the ring are reset by the reset circuits. The positive outputs of each units and tens ring stage are applied to the time slot gates. Coincidence of a tens ring and a units ring stage generates a time slot gate voltage; for example, coincidence of UR 5 and TR 10 generates TSG 15.

c. Reset and Automatic Start Control.

- (1) These circuits start and stop the ring counters which are normally under control of associated equipment. However when required, the ring counters will run continuously. In the normal or remote start condition, RC F/F is OFF and its negative output opens a gate in the amplifier synchronizer through the CDG/TAC contacts of S60B. The gate in the amplifier synchronizer also requires a remote start signal to open it. The gate passes a clock pulse, which is biased negatively, and returns it to the remote start gate of figure 49. This gate passes the pulse to UR 7 and TR 50, starting the ring counters at TS 57. The pulse also turns ON RC F/F making its output positive. When the rings go through a complete cycle and arrive at TS 56, the clock pulse at the end of TS 56 triggers RC F/O which turns OFF RC F/F. Combination gate CG1,



NOTES:
1. INDICATES A BIAS OR GATE CONTROL VOLTAGE.
2. INDICATES A PULSE.
3. INDICATES DIRECTION ONLY.

ENCODER CONTROL CIRCUITS

READY TONE CONTROL

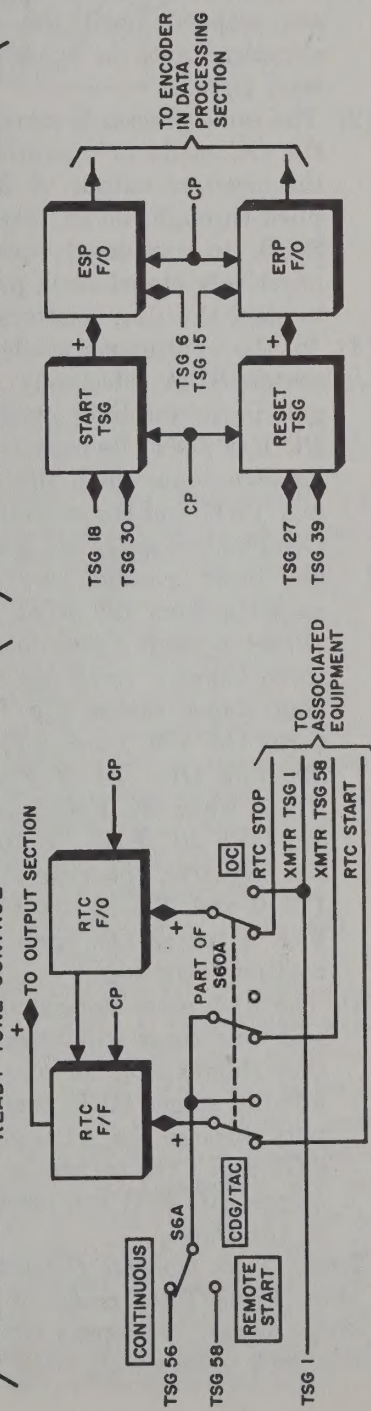


Figure 43. Program generator, transmitter, block diagram.

which requires a positive input from TR 50 and a negative input from RC F/F, passes a clock pulse to TRR and URR F/O's which turn OFF all ring stages. A clock pulse also passes through the continuous start gate to the ring counters to start them, but they cannot start while the reset pulses from URR and TRR are present. As soon as TR 50 is reset, CG1 is disabled and the rings are stopped until the amplifier synchronizer gate is opened by a remote start signal.

- (2) The same process is carried out when in the OC mode of operation, except that the negative output of RC F/F is applied through the OC contacts of switch S60B, to associated equipment, and a negatively biased clock pulse is returned to start the ring counters.
- (3) In the continuous mode of operation, switch S70A effectively shorts out the gate in the amplifier synchronizer. With RC F/F OFF, its negative output opens its own input gate, the gates of URR and TRR, and the continuous start gate. Combination gate CG1 is now open, with one input ground (+) and the other negative from RC F/F. A clock pulse passes through it and does the following three things: resets all units and tens ring stages except UR 0 and TR 00; turns ON UR 0 and TR 00; and turns RC F/F ON. RC F/F stays ON until TS 56 when RC F/O is triggered, turning OFF RC F/F. With RC F/F output negative, the ring stages are reset, UR 0 and TR 00 are turned ON, RC F/F is turned ON again, and the rings continue counting.
- (4) The ALL gates associated with the units and tens rings will restart the rings if they should stop for any reason. With all ring stages OFF, their negative outputs through the ALL gates open gates CG2 and CG3 to pass a clock pulse to trigger RC F/O and restart the rings as in (3) above.

d. Ready Tone Control Circuits. In the remote start CDG/TAC mode of operation, an RTC start signal (+) opens the gate of RTC F/F to a clock pulse which turns RTC F/F ON.

When ON, RTC keys the modulator to transmit a tone of 600 cycles as a remote start signal. An RTC stop signal (+) applied to RTC F/O allows a clock pulse to trigger RTC F/O and turn OFF RTC F/F. This terminates the transmission of the 600-cycle signal from the modulator. During OC operation the RTC start signal is either TS 56 or TS 58, depending on whether the mode of operation is continuous or remote start, and the RTC stop signal is TS 1 of the next frame.

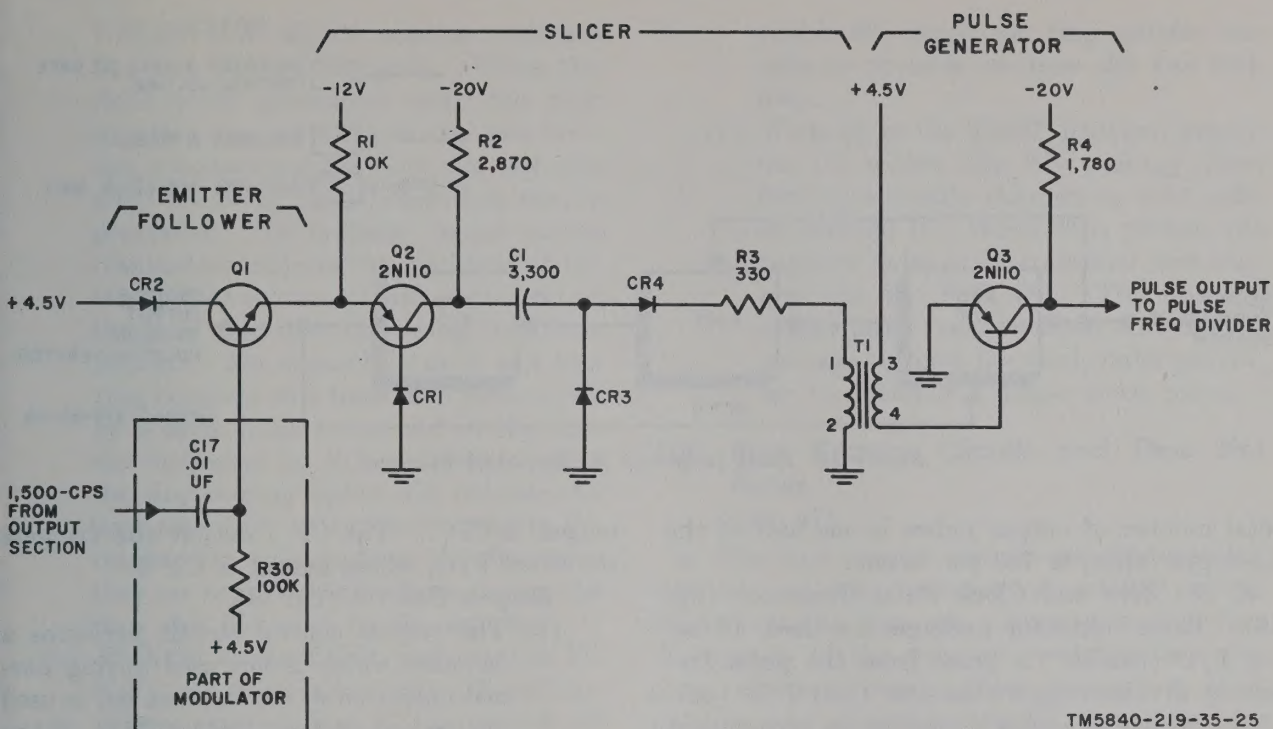
e. Encoder Control Circuits. The encoder control circuits furnish encoder start and reset pulses. The start pulses are generated by ESP F/O each time it is triggered by a clock pulse at TS 6, TS 18, and TS 30. The reset pulses are generated by ERP F/O each time it is triggered by a clock pulse at TS 15, TS 27, and TS 39.

105. Clock Pulse Generator

a. General. The clock pulse generator circuits generate two kinds of pulses: a set zero pulse, positive-going and having an amplitude of about 3.5 volts and a duration of about 40 microseconds; and two clock pulse outputs occurring about one microsecond apart (for practical purposes the two clock pulse outputs are considered as occurring simultaneously). The clock pulses run continuously at a rate of 750 per second. They are negative-going and have an amplitude of about 9 volts and a duration of about 1.5 microseconds. The basic timing for the clock pulses is a 1,500-cycle signal from the output section of the data set (par. 127). The following circuits in the program generator are used for generating the set zero pulses and clock pulses: (1) 1,500-pps pulse shaper (fig. 44), (2) frequency divider (fig. 45), and (3) set zero and clock pulse generators (fig. 46).

b. 1,500-pps Pulse Shaper (figs. 44 and 163 (2)). The 1,500-pps pulse shaper is a three-stage transistor circuit. The input is a 1,500-cycle sine wave with a peak-to-peak amplitude of about 10 volts, and the output is a series of positive-going pulses occurring at the rate of 1,500 per second.

- (1) Transistor Q1 is an emitter follower having a gain of unity. The 1,500-cycle input signal is applied at the base through C17, and the output of the stage is a low impedance source for driving slicer Q2. Q2, a point contact transistor,



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Figure 44. 1,500-pps pulse shaper, simplified schematic.

is held in the OFF condition (app. III) by -12 volts through R1 until the emitter is driven in the positive region above ground. As the emitter of Q2 goes slightly positive, the transistor suddenly goes to the ON condition. When the transistor is in the ON condition, the collector voltage is -2.5 volts, and when it is in the OFF condition, the collector voltage is about -17 volts. The output is a positive-going rectangular wave. Diode CR1 prevents damage to the transistor by limiting the emitter current during the positive part of the driving cycle. The output is differentiated by C1, R3, and the primary of T1. The positive pulses of the differentiated output are applied to T1 primary. Negative differentiated pulses are shunted to ground by CR3. CR4 and CR3 shunt the negative pulses generated by the collapse of the field of T1 which, if allowed to appear at the collector of Q2, might cause the transistor to be turned ON again between pulses. When the voltage at the emitter of Q2 again goes negative with respect to its base, the transistor is turned OFF.

- (2) The voltage at the secondary of T1 is a series of pulses negative at terminal 4. Q3 is held in the OFF condition by positive bias applied to terminal 3 of T1. As the voltage at terminal 4 of T1 goes slightly negative with respect to ground, the transistor is turned ON. The output is a series of positive-going pulses.

c. *Pulse Frequency Divider* (figs. 45 and 163 (2)). The pulse frequency divider divides the 1,500-pps output from the pulse shaper by 2, providing positive pulses at the rate of 750 per second. Two transistor packages are used: PFD F/F (par. 100c) and PFD F/O (par. 96b). The gate shown in the figure is a part of the F/F. The first pulse of the 1,500 pps is applied to the gate and the F/F input. It cannot pass through the gate because the gate requires a positive bias from the F/F to open it. The first pulse turns the F/F ON. The F/F then applies a positive bias to the gate. The second pulse passes through the open gate to the F/O, triggers it, and causes it to generate a pulse at its output. It also sends a set zero pulse back to the F/F to turn it OFF. The F/F is not affected by the second pulse because it is already ON. The F/F then is turned ON for each odd-numbered pulse, and the F/O is triggered by each even-numbered pulse. The

NOTES:

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2.  INDICATES A PULSE.
3.  INDICATES DIRECTION ONLY.

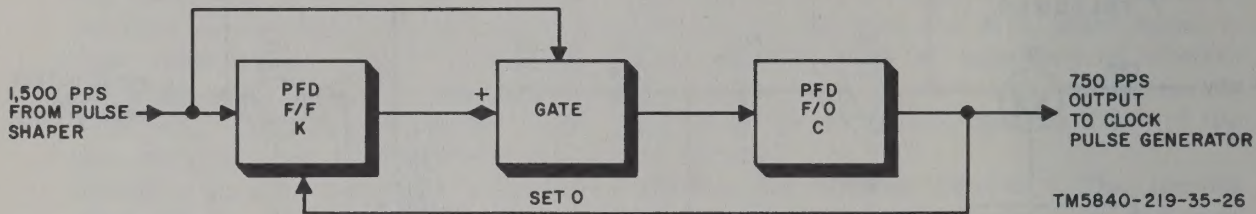


Figure 45. Pulse frequency divider, block diagram.

total number of output pulses is one half of the 1,500-pps input, or 750 per second.

d. *Set Zero and Clock Pulse Generator* (fig. 46). Three transistor packages are used, all being F/O circuits. A pulse from the pulse frequency divider triggers the first (SZ) F/O (par. 102b), which generates a positive set zero output pulse having a duration of about 40 microseconds. This pulse is also fed to the second (CP 1) F/O (par. 98a) through a differentiating gate (part of the CP 1 F/O). The differentiated trailing edge of the set zero pulse (40 microseconds later than the leading edge) triggers the second F/O, whose

output is CP 1. The CP 1 output also triggers the third F/O, whose output is CP 2.

e. *Recycle Control* (fig. 46).

(1) The recycle control circuit performs a function which is not used during normal operation of the data set but is used during certain tests (table VII). When RECYC button S3 is pressed, and PC switch S9 is at TEST, this circuit starts the clock pulse generators which permit the transmitter to run until the ring counters (par. 106) arrive at the time slot determined by the settings of the

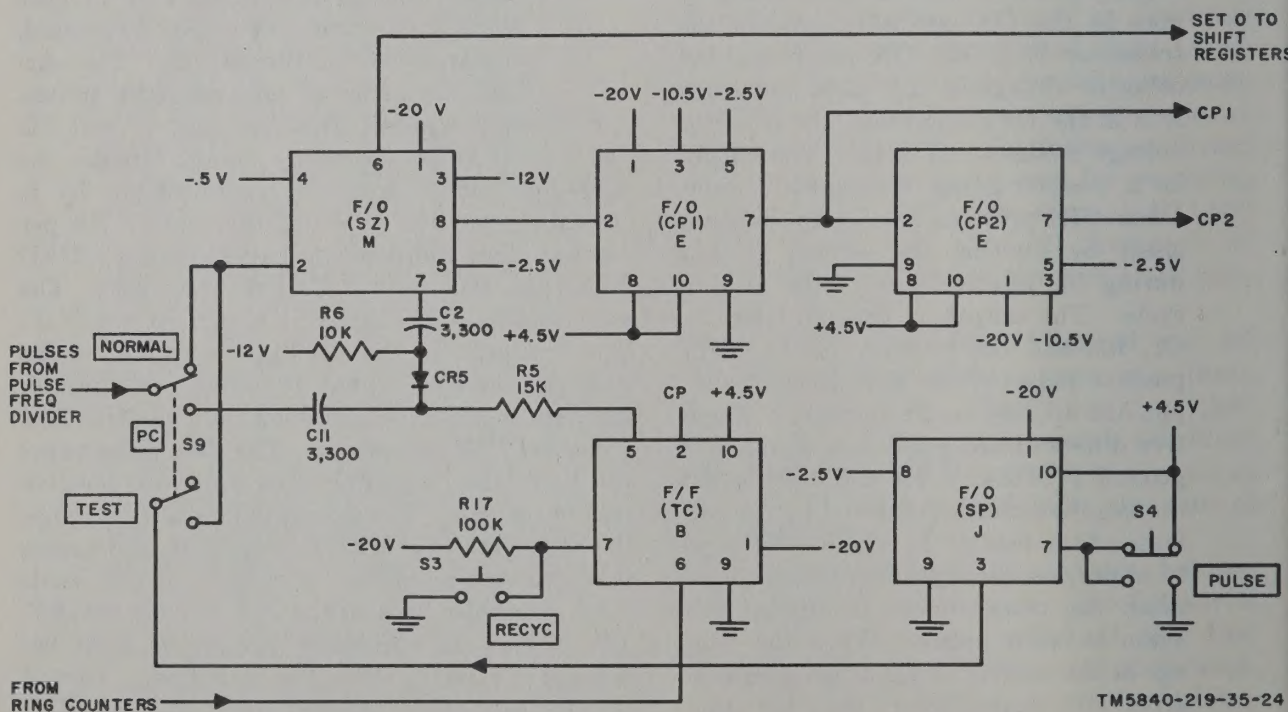


Figure 46. Set zero and clock pulse generator, transmitter, schematic.

UNITS and TENS selector switches S11 and S10 (2, fig. 163). When the clock pulse generators stop, the ring counters stop but a continuous gate voltage, representing the time slot immediately following the selected time slot, is generated. The indicator lamps on the transmitter indicate the condition of the transmitter control circuits at the end of the time slot that the switch positions indicate. The succeeding units and tens ring counters will have been turned ON by a clock pulse at the end of the time slot indicated by S11 and S10, so that the ring counter lights will indicate the next time slot. All other circuits in the transmitter will perform the functions they are supposed to perform during the time slot indicated by the switches.

- (2) With S9 in the TEST position, the TC F/F (par. 95a) is normally ON and applies a positive bias to the cathode of CR5. This bias, and the negative bias from -12 volts through R6, disables CR5. Under this condition, pulses from the pulse frequency divider cannot pass through CR5 and C2 to trigger the clock pulse generator. In the TC package, capacitor C2 is charged negatively at terminal 7. When S3 is pressed, terminal 7 is grounded. This discharges C2 and sends a positive pulse to the base of the transistor through L1, turning the F/F OFF. With TC F/F OFF, CR5 conducts because of the negative (OFF) bias at its cathode, and passes pulses to SZ F/O, starting the clock pulse generator. TC F/F remains OFF until a positive pulse, resulting from the coincidence of a units and tens ring stage (app. II, A, fig. 211), arrives at terminal 6, enabling the gate within the package and permitting the next clock pulse to turn TC F/F ON. With TC F/F ON, diode CR5 is again disabled, and pulse frequency divider pulses are prevented from triggering the clock pulse generator.

f. Pulse Control Circuit.

- (1) This circuit is used only for testing in conjunction with the recycle control circuit. Operation of PULSE pushbutton

switch S4 causes the ring counter circuits to advance one time slot and then stop.

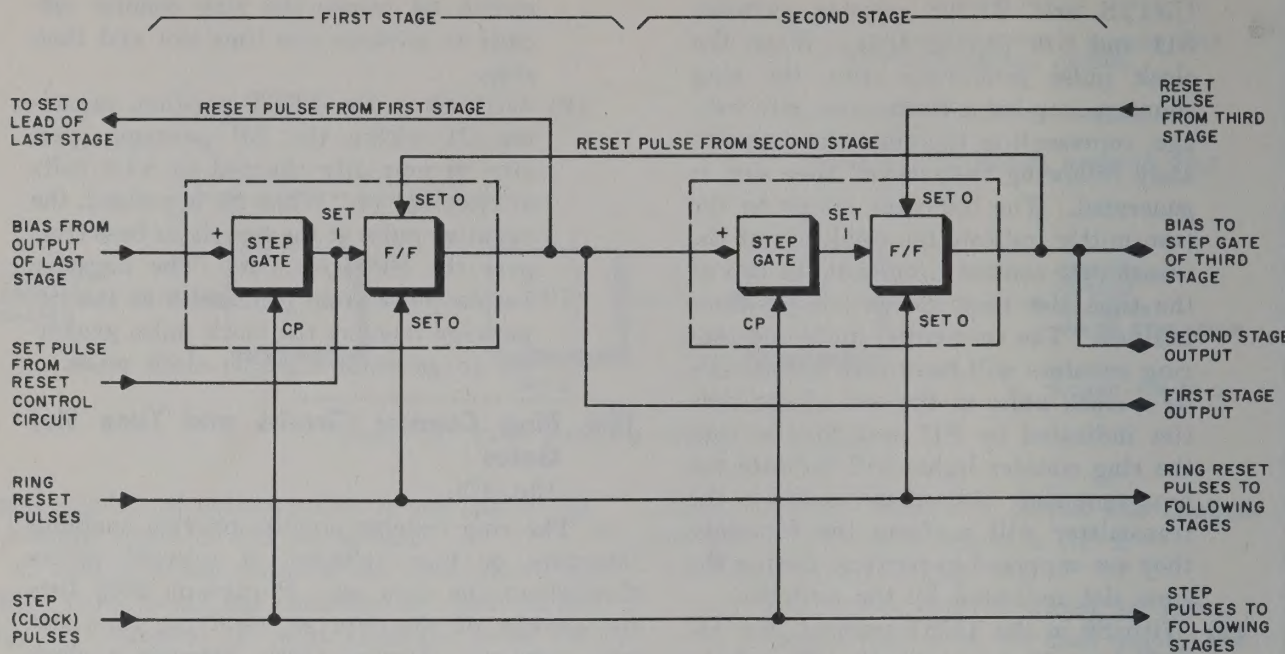
- (2) With S9 in the TEST position, capacitor C1 within the SP package (par. 99a) is normally charged to +4.5 volts at terminal 10. When S4 is pressed, the negative pulse at the transistor base triggers the SP F/O ON. The negative output pulse from terminal 3 of the SP package triggers the clock pulse generator to generate a single clock pulse.

106. Ring Counter Circuits and Time Slot Gates

(fig. 47)

a. The ring counter circuits provide enabling intervals, or bias voltages, at selected points throughout the data set. Paragraph 200b lists the circuits of the data set receiving time slot gate voltages. During these intervals a clock pulse may be applied to trigger a transistor circuit and thus time the performance of a circuit function. The ring counter circuits are bistable transistor circuits arranged in two counting chains: a units ring (UR) and a tens ring (TR). The units ring steps ONE for each clock pulse counting from 0 through 9. The tens ring steps every tenth clock pulse. There are 10 bistable circuits in the units ring and six in the tens ring. The two form a decade counter able to count to 60. To provide for counting to 58 (0-57), the maximum number of time slots used in the data set frame, a monostable F/O transistor circuit (TRR-URR) is provided for each ring to reset the ring to zero at the end of the time slot 56 (par. 107). (For remote start operation the rings are started at time slot 57 and go to time slot 59, making a total of 60 time slots.)

b. At the beginning of the frame (time slot 0) transistor circuits UR 0 and TR 00 (par. 107) are both ON; all succeeding counter stages are OFF. An ON stage furnishes an enabling bias to the transmission-type gate in its next succeeding stage so that a clock pulse (applied simultaneously to the gates in all units ring stages) activates the next following stage as shown in figure 47. That stage, in turning ON, feeds a pulse back to the immediately preceding stage, which turns the preceding stage OFF. Thus the units counter is stepped from UR 0 to UR 1 and through UR 9. UR 9 is connected back to UR 0



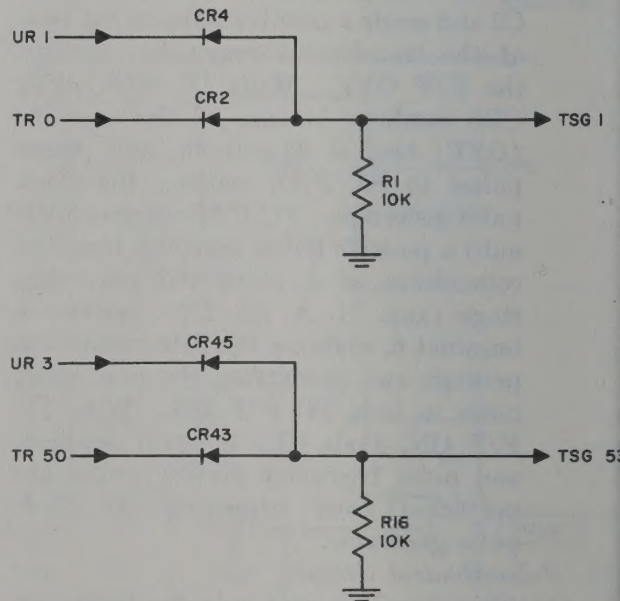
- NOTES:
1. ———> [] INDICATES A BIAS OR GATE CONTROL VOLTAGE.
 2. ———> [] INDICATES A PULSE.
 3. ———> [] INDICATES DIRECTION ONLY.

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Figure 47. Ring counter circuits, transmitter program generator, simplified block diagram.

and furnishes UR 0 with an enabling bias when UR 9 is ON. UR 0 also furnishes a pulse to UR 9 to turn it OFF when UR 0 goes ON. Thus the ring operates continuously. At the time UR 9 furnishes an enabling voltage to UR 0, a "step tens" gate (fig. 81) is enabled, allowing the same clock pulse which triggers UR 0 to trigger TR 10. In turning ON, TR 10 turns OFF TR 00. In this way the ring counters continue to advance to the count of 57 at the line signaling speed of 750 pps.

c. The time lot gates are AND, or coincidence, gates wired to appropriate outputs of the ring circuit stages. These gates are illustrated in appendix II. Figure 48 is a partial drawing of figure 187 and shows AND gates connected to various ring counters. TSG 1, for example, is formed by the coincidence of UR 1 and TR 00, and TSG 53 is formed by coincidence of UR 3 and TR 50. Each TSG is a positive pulse of gate control voltage for one time slot duration.



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Figure 48. Typical time slot gates, simplified schematic.

Thus TSG 1 is a positive pulse during TS 1, and is negative during all other time slots. The clock pulses occur at the end of every time slot so that a clock pulse passed through a gate by TSG 1 would start an operation at the end of TS 1, or could be considered as starting the operation at the beginning of TS 2. The outputs of other units and tens ring stages are similarly connected for as many time slots as are required to perform all transmitter functions in a selected time sequence. The ring counters would continue to count to 60 and recycle continuously if no further action were taken. It is desired, however, to provide a frame of only 58 time slots (60 for remote start operation) and reset the counters for the start of the succeeding message frame. TSG 56 is used to time this reset function.

107. Reset and Automatic Start Control (fig. 49)

a. General. The reset and automatic start control provides a ring counter circuit reset at the end of the frame and automatic start for the next succeeding frame when the continuous mode of operation is used. It provides for reset of the frame and restart under control of a remote start signal when the remote start mode of operation is in use (pars. 157-159).

b. Remote Start CDG/TAC Operation. During remote start CDG/TAC operation, switches S5 and S7 are in the REMOTE START position (fig. 49), and CDG/TAC-OC switch S60 is at CDG/TAC. The set zero pulses from TRR and URR, in addition to going to TR 10 through TR 50 and UR 1 through UR 9, also go to TR 00 and UR 0 by way of S5A and S5B to reset all ring counter stages. When TR 50 is reset, its OFF bias is applied through S7B and R6 to disable CR5, thus preventing clock pulses from passing through CR5. At the end of the ready signal, when F/F No. 7 in the remote start section comes ON (pars. 157-159), the STP signal, consisting of a negative bias and a clock pulse, is applied to CR6 and CR7 in the remote start gates. The negative bias enables CR6 and CR7, and the clock pulses pass through those diodes and through C6 and C7 to turn ON TR 50 and UR 7 for the new frame. This STP is also applied to terminal 2 of RC F/F by way of S7A and turns RC F/F ON. This disables CR5 so that the ring counters go from 57 to 58 to 59 and

then to 0 so that the ready tone control will operate properly (par. 108). The rings continue to count until, at the end of TS 56, RC F/O is triggered, turning RC F/F OFF. The next clock pulse resets all ring counter stages awaiting the next remote start signal for a new frame.

c. Remote Start OC Operation. During remote start OC operation, CDG/TAC-OC switch is at OC. The STC signal, instead of going to the amplifier synchronizer, is sent to associated equipment and is called the acknowledge transmit pulse (ACK XMIT). There it is one of the enabling biases for a gate that allows STP pulses to be sent to the transmitter. When RC F/F goes ON, the ACK XMIT signal becomes plus and inhibits the STP gate in the associated equipment. The ON output of RC F/F is the ACK XMIT signal.

d. Continuous Operation. In the continuous mode of operation, RC F/F (par. 94a) is ON at all times except during TS 57 (fig. 49). Clock pulses are passed continuously by CR5, but the ON condition of RC F/F disables the TCG's to TR 00 and UR 0 and the internal TCG's in TRR F/O and URR F/O. TSG 56 applies an enabling voltage to the time control gate terminal 7 of the RC F/O (par. 96a). The clock pulse at the end of TS 56 triggers the RC F/O from which a positive-going pulse is fed to terminal 10 of the RC F/F, turning the F/F OFF. In turning OFF, RC F/F applies a negative bias to its own pin 2, and to pin 2 of TRR F/O and URR F/O, as well as to the continuous start gates associated with UR 0 and TR 00. This permits the next clock pulse (which appears at the end of TS 57) to do the following four things: trigger TRR F/O, which sends a set zero pulse to all tens ring stages except TR 00; trigger URR F/O, which sends a set zero pulse to all units rings stages except UR 0; turn ON TR 00 and UR 0 through negative TCG's; and turn RC F/F ON again. In this way the new frame is started.

e. All Gates.

- (1) The purpose of the ALL gates (fig. 50) is to ensure that during continuous operation RC F/O gets a clock pulse even if a transient trouble condition occurs which may cause all stages of either the units ring or tens ring to be OFF. If this occurs, time slot gates are not being generated and the ring counters must be

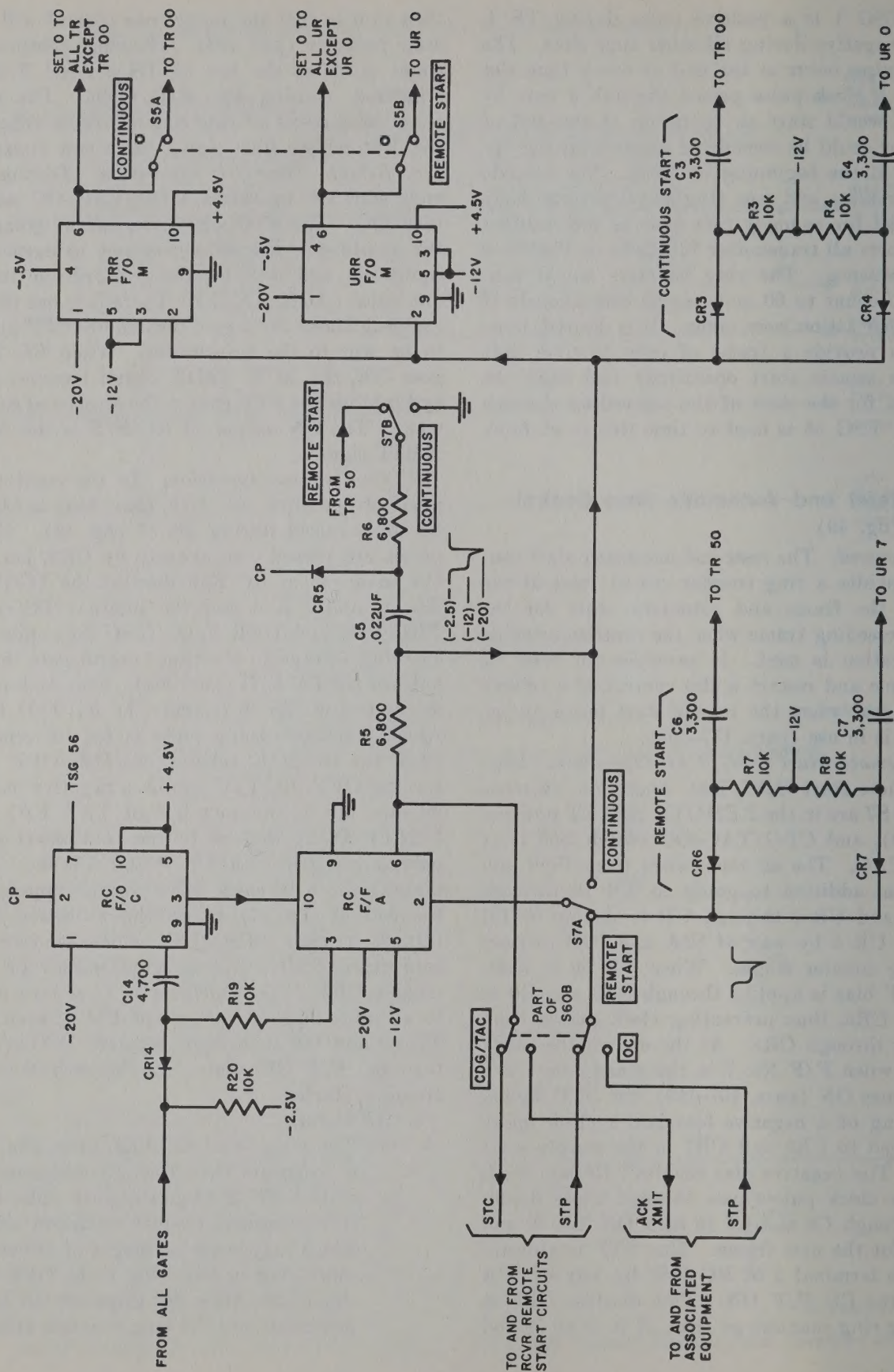


Figure 49. Reset control circuits, schematic diagram.

enabled and the ON bias from UR 6 and UR 8 enables CR19, allowing a clock pulse to pass through C13 to trigger RC F/O and reset the circuit. The same results are obtained if UR 6 and UR 9 are ON simultaneously.

108. Ready Tone Control

(fig. 51)

a. General. The transmitter output section (par. 125) supplies a ready and sync signal preceding each frame of data. The 600-cycle component of the dual-frequency ready signal is timed by the ready tone control of the program generator. The operation of this circuit depends upon the mode of operation of the data set and the associated equipment. When operated as operations central (OC), the ready tone control is used for generating the remote start signal to associated equipment, and the CDG/TAC-OC switch S60A is in the OC position. When the data set is at a battery site, S60A is in the CDG/TAC position. In either case the 600-cycle signal is released to the line when RTC F/F (par. 94b) is ON, and is terminated when RTC F/F is OFF.

b. CDG/TAC Operation. In this mode of operation TSG voltage is applied to terminal 5 of RTC F/F, through contacts of S6A and S60A. This occurs at TSG 56 for continuous operation and at TSG 58 for remote start operation. The

clock pulse at the end of the time slot turns RTC F/F ON, and the ON bias from the F/F is fed to the modulator to transmit a 600-cycle signal. At the end of TS 1 of the next frame, the gate voltage applied through S60A to terminal 7 of RTC F/O (par. 96e) allows the clock pulse at its terminal 2 to pass through to trigger the F/O. The output pulse from the F/O is applied to terminal 10 of the F/F turning the F/F OFF and terminating the 600-cycle transmission. Diode CR12 is used to clamp the output voltage at terminal 3 of RTC F/F to prevent it from going more negative than -15 volts. CR11, R15, and R16 work in conjunction with the 600-cycle input filter Z3 of the modulator to inhibit the generation of harmonic voltages which would affect the modulator operation.

c. OC Operation with Transmitter Off. The associated equipment sends a positive RTC start signal to the RTC F/F. The ON output of the F/F, called the RTC gate, is gated by associated equipment and delayed 3.6 milliseconds, then returned to the RTC F/O as the RTC stop signal. As in *b* above, the 600-cycle output of the modulator is keyed ON by the output of RTC F/F.

d. OC Operation with Transmitter On. Both TSG 58 and TSG 1 are sent to associated equipment where they are gated and become the RTC start and RTC stop for the 600-cycle ready signal.

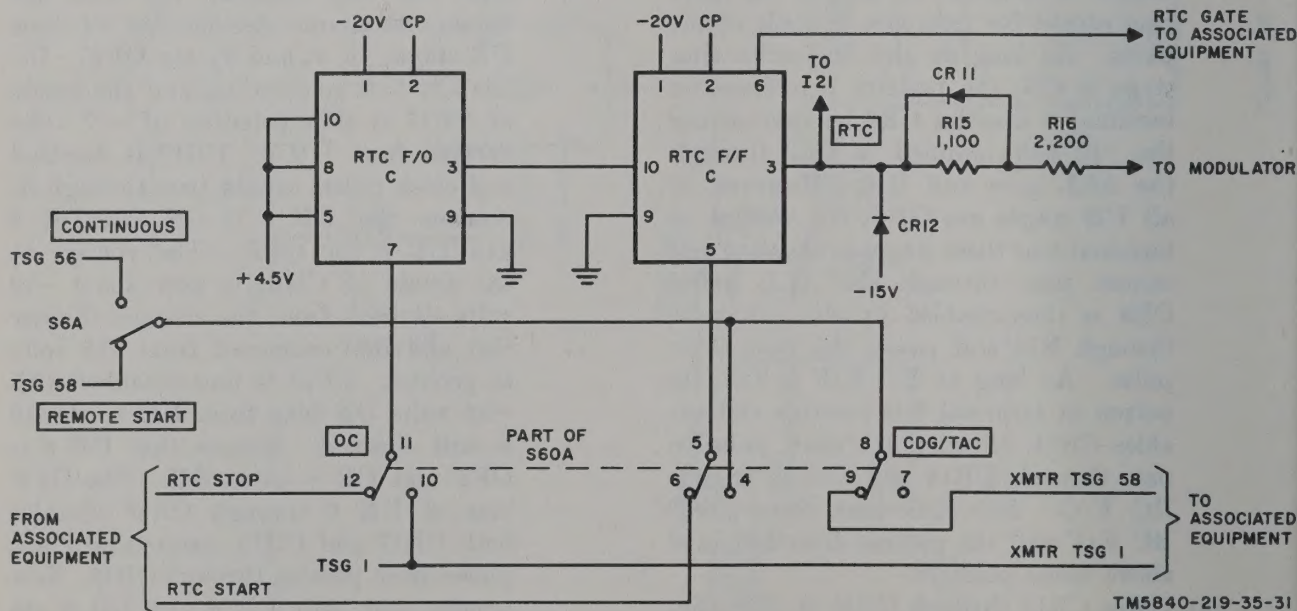


Figure 51. Ready tone control, schematic.

109. Encoder Control

(fig. 52)

The encoder control starts and stops the sweep generator in the encoder (par. 113a). Clock pulses pass through the encoder start gate to terminal 8 or are gated through terminal 2 during selected time slots to trigger the start ESP F/O (par. 96e). Similarly, clock pulses pass through the encoder reset gate to terminal 8 or are gated through terminal 2 during other selected time slots to trigger the reset ERP F/O

(par. 96d), which furnishes reset pulses to the reset multivibrator. The encoder sweep for the H coordinate is started at the end of time slot 6 and is reset at the end of time slot 15. The sweep for the X coordinate is started at the end of time slot 18 and is reset at the end of time slot 27. The sweep for the Y coordinate is started at the end of time slot 30 and is reset at the end of time slot 39. Diodes CR14 and CR11 prevent the voltage at terminal 8 of the two F/O's from going more positive than +4.5 volts.

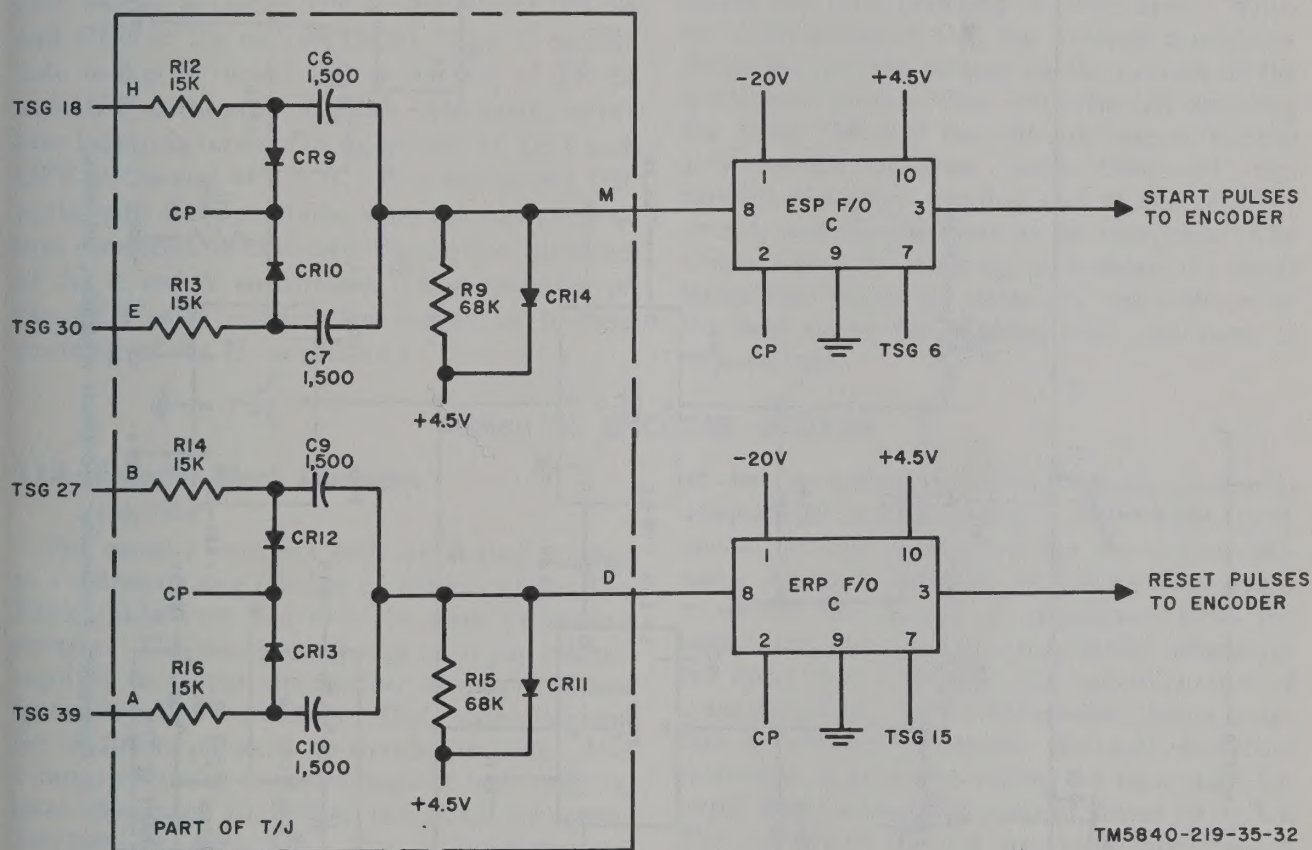


Figure 52. Encoder control, schematic.

Section II. COORDINATE MULTIPLEX

110. General

The coordinate multiplex (fig. 53) receives the three coordinate voltages, H, X, and Y, and connects them sequentially to the encoder through the contacts of three single contact reed-type relays. The relay operate and release sequence is timed by the program generator to present each coordinate voltage to the encoder in proper turn.

An additional relay, earth curvature relay (ECR), has contacts that short circuit the earth curvature correction potentiometer in the encoder during the encoding of the H coordinate.

111. Coordinate Lockup and Release Circuits (fig. 53)

Each of the coordinate relays and the earth curvature relay is operated by its associated tran-

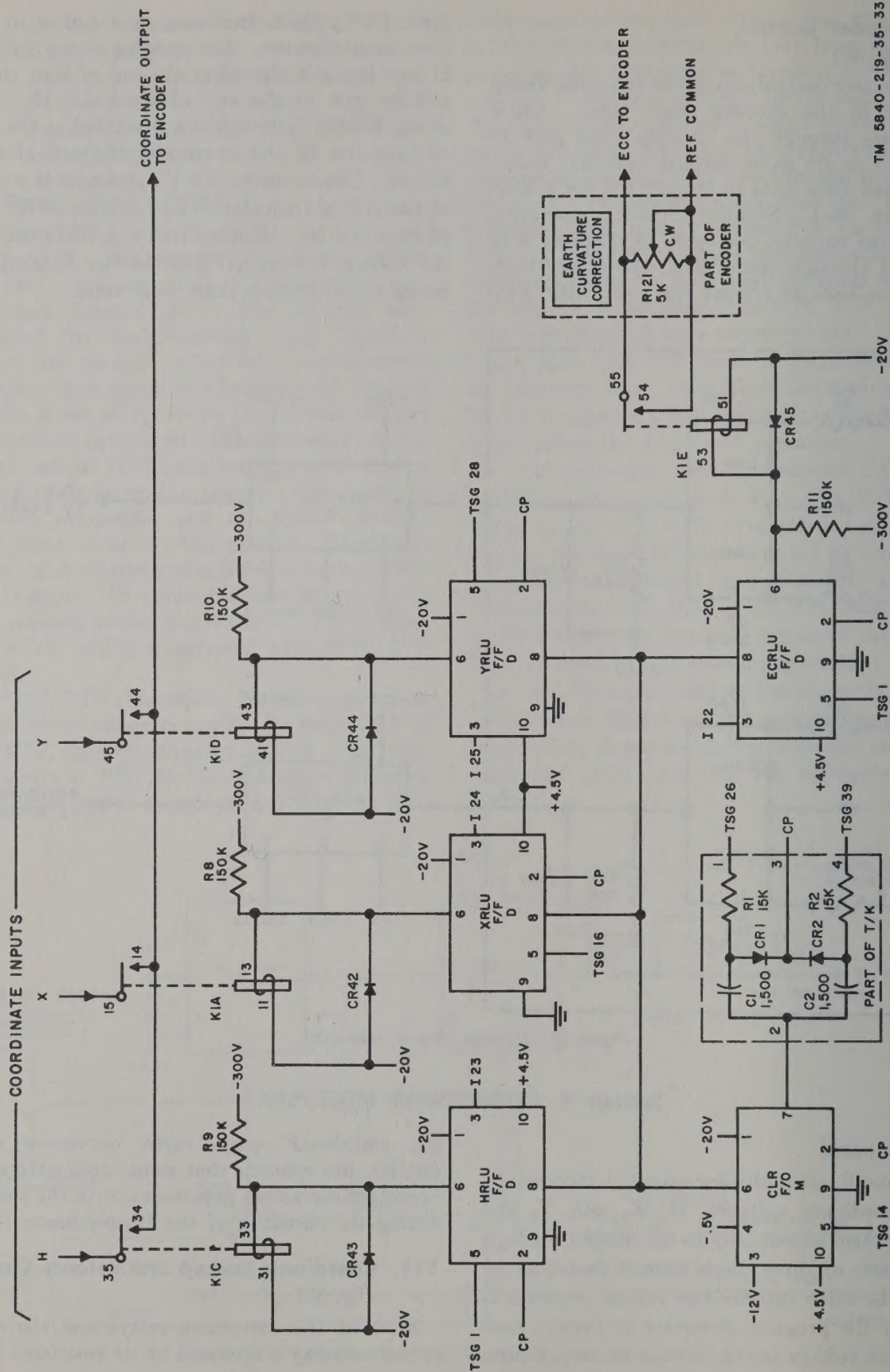


Figure 53. Transmitter coordinate multiplexer, schematic.

sistor lockup F/F (par. 97a). Each of the lockups has a gate circuit which allows a clock pulse to pass through it at appropriate times to turn the F/F ON (app. III). There is one coordinate relay lockup release F/O (CLR) (par. 102a) which has one gate circuit built into it, and two associated gates (TCG), all of which pass clock pulses to the F/O at appropriate times. This clock pulse triggers the F/O, which, in turn, turns all the lockups OFF. The H coordinate lockup is turned ON at the end of TS 1 and OFF at the end of TS 14. The X coordinate lockup is turned ON at the end of TS 16 and OFF at the end of TS 26. The Y coordinate lockup is turned ON at the end of TS 28 and OFF at the end of TS 39. The earth curvature lockup is turned ON at the end of TS 1 and OFF at the end of TS 14. It is not turned ON again until the next frame, since the earth curvature correction is used only during the encoding of the X and Y coordinates. (The operation of the ECR relay removes the correction for the encoding of the H coordinate.)

112. Relay Circuits

(fig. 53)

Two voltages are applied to each relay winding. One is -300 volts applied through 150,000 ohms at one end of the winding, and the other is -20 volts applied directly to the other end of the winding. The junction of the relay winding and the 150,000-ohm resistor is connected to terminal 6 of the lockups. When the lockup F/F is OFF, the collector impedance at terminal 6 is high, and the diodes shown across each relay winding (CR42 through CR45) hold the voltage across the relay winding at near zero. When the F/F is turned ON, the collector impedance drops, making the voltage on the cathode of the diode more positive than -20 volts and disabling the diode. Most of the collector current for the F/F in this condition passes from -20 volts through the relay winding and to the collector circuit, causing the relay to be energized. The diodes across the windings also damp any oscillation that might be caused by the collapse of the field across the winding when the relay is de-energized.

Section III. ENCODER SECTION

113. Encoder Block Diagram

(fig. 25)

The encoder converts each dc analog voltage to a corresponding number of 100-kc pulses. The 100-kc pulses are fed into the data processing circuits. The minimum change in input voltage required to change the number of output pulses by one is called a quantum. The maximum number of 100-kc pulses to be counted is 1,024. For a range of analog input voltage of ± 50 volts (a total change of 100 volts) one quantum equals 100/1024, or .0975 volt. For an input voltage range of ± 100 volts, the quantum is twice that value, or .195 volt. When +50 volts is applied to the encoder, 1,024 output pulses appear. When the input is zero volts, 512 pulses appear, and when the input is -50 volts, no output pulses appear. Thus, each decimal digit between 0 and 1,024 represents a particular voltage level, and the resulting data becomes digital data. The number of 100-kc pulses is counted on a binary rather than a decimal basis because a binary number is represented by a series of ONE's and ZERO's that may be sent to an electrical communication line as a series of ON and OFF pulses

of electric current. A 10-digit binary number is adequate to represent the desired 1,024 (2^{10}) quanta of input analog voltage for each coordinate. An earth curvature correction is provided to correct the X and Y coordinates when the transmitter and receiver are separated sufficiently far apart that a straight line approximation of these coordinates is in error greater than a quantum of positional reference. No earth curvature correction is necessary unless the separation between stations is of the order of 200 or 300 miles. The correction control provided introduces a change in the number of output pulses for a given value of input coordinate voltage.

a. Sweep Circuits. The sweep circuits in the encoder consist of the sweep generator and the reset multivibrator circuits. A positive start pulse (A of fig. 25) from the transmitter program generator triggers the reset multivibrator (a flip-flop circuit that stays in one state of operation until triggered into the other state). The reset multivibrator circuit applies a positive voltage (C, fig. 25) to the sweep generator circuit. This positive voltage causes the sweep generator output (D, fig. 25) to go from +55 volts to -55

volts at a rate determined by the circuit constants, the earth curvature correction potentiometer setting, and the positive reference voltage. At the end of a specified time after the start pulse, a reset pulse is applied to the reset multivibrator circuits, causing a negative voltage (C, fig. 25) to be applied to the sweep generator. This negative voltage causes the sweep generator output to change rapidly from -55 volts to $+55$ volts, at which point it remains until the next start pulse. The start and reset pulses occur alternately at specified times to enable the H, X, and Y coordinate positional data analog voltages to be changed to a proportional number of 100-kc pulses in sequence. The output of the sweep generator (D, fig. 25) is applied to the reference comparator and the target comparator.

b. Reference Comparator. The reference comparator has two inputs: the output of the sweep generator and a minus reference voltage. This reference voltage is derived from a source of either -250 or -300 volts and is divided down in the input circuit to a value of -50 volts. The two inputs are added algebraically in the input circuit of the reference comparator. When the sum of the two inputs passes through zero, a rapid change in the output takes place. This rapid change occurs when the sweep generator voltage reaches $+50$ volts as shown in D and E of figure 25. The output of the reference comparator (E, fig. 25) is fed to the reference coincidence pulse generator.

c. Reference Coincidence Pulse Generator. The input to the reference coincidence pulse generator is shown in E of figure 25. The input stage is biased so that it will not conduct until the input voltage reaches a predetermined level. The output stage contains a peaking network and a diode gate so that only a positive going voltage at the input will cause an output pulse. The output of the reference coincidence pulse generator (F, fig. 25) is coupled to the gate control multivibrator circuit.

d. Target Comparator. The target comparator receives two inputs: the output of the sweep generator (D, fig. 25) and the dc analog voltages from the coordinate multiplex circuits. These two voltages add algebraically in the target comparator input circuit. As in the reference comparator, a rapid change in the output occurs when the target voltage is equal and opposite in sign to the sweep generator voltage. The output

of the target comparator (G, fig. 25) is fed to the target coincidence pulse generator which feeds a pulse (H, fig. 25) to the gate control multivibrator circuit. This pulse is identical to the pulse from the reference coincidence pulse generator but is applied at a different time. The time interval between the pulse from the reference coincidence pulse generator and the pulse from the target coincidence pulse generator is controlled by the value of target voltage. This is shown in D, E, F, G, and H of figure 25. Note that the voltage for target No. 1 is $+50$ volts and that the gate remains open from time T1 to T2, whereas the voltage of target No. 2 is -25 volts, and the gate remains open from time T3 to T4.

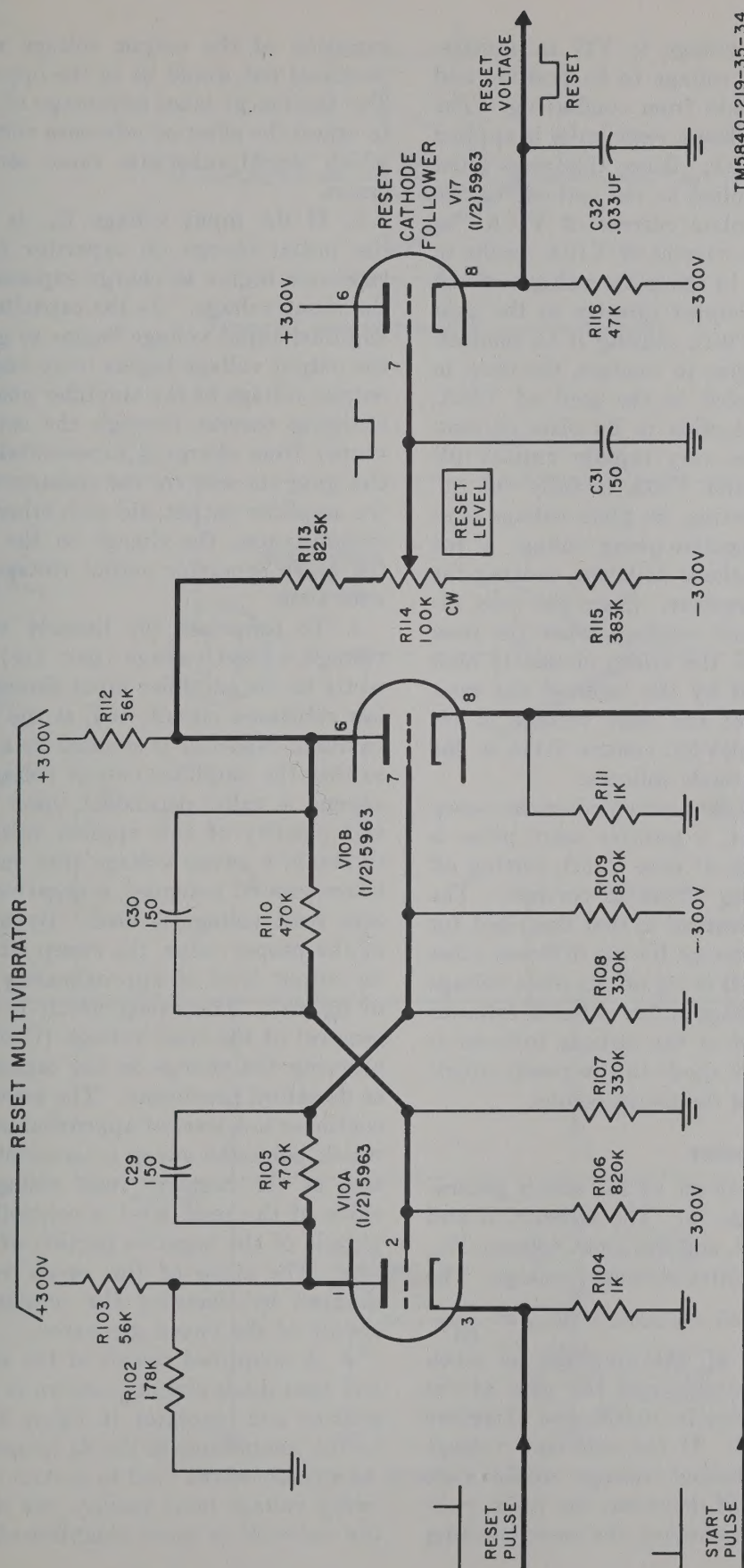
e. Gate Control Multivibrator and 100-kc Pulse Gate. The gate control multivibrator has the output of the reference coincidence pulse generator applied to the grid of one stage and the output of the target coincidence pulse generator applied to the grid of the other stage. This is a flip-flop multivibrator that stays in one state of operation until triggered into the other state. The output of the gate control multivibrator (J, fig. 25) is applied to the cathode of the 100-kc pulse gate diode. The 100-kc pulse gate is thus turned ON and OFF, allowing the 100-kc pulses to pass in an amount corresponding to the target voltage input (L, fig. 25).

f. 100-kc Crystal Oscillator and Pulse Generator. The 100-kc crystal oscillator supplies a 100-kc sine wave to the pulse generator. The pulse generator is operated class C, removing the negative half of the sine wave completely and part of the positive half. The remaining portion is shaped in a peaking circuit and is applied as a negative pulse to the 100-kc pulse gate. The output of the 100-kc pulse generator is shown in K of figure 25.

114. Reset Multivibrator

a. The schematic of the reset multivibrator and associated cathode follower circuit is shown in figure 54. Tube V10 is a conventional Eccles-Jordan multivibrator circuit whose output is coupled directly to the grid of the reset cathode follower V17A.

b. During the sweep interval, V10A conducts, causing V10B to be cut off by the direct coupling between the tubes of the multivibrator. When V10B is cut off, its plate voltage is relatively



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Figure 54. Encoder reset multivibrator and cathode follower, schematic.

high and the input voltage to V17 is positive. This causes the reset voltage to be positive and prevents the reset diode from conducting. The sweep is terminated when a reset pulse is applied to the cathode of V10A. Since this reset pulse is positive and is applied to the cathode of the tube, it reduces the plate current of V10A. A reduction in the plate current of V10A results in a corresponding rise in the plate voltage of the tube. This rise is coupled directly to the grid of the cut off tube V10B, causing it to conduct. As soon as V10B begins to conduct, the drop in plate voltage is coupled to the grid of V10A, causing a further reduction in its plate current. This process continues very rapidly until V10B is fully conducting and V10A is fully cut off. When V10B is conducting, its plate voltage is at a minimum and a negative-going voltage is fed to the grid of the cathode follower, causing the reset voltage to be negative. Since the reset diode in the sweep circuit conducts when the reset voltage goes negative, the sweep circuit is reset to a level determined by the level of the reset voltage. The level of the reset voltage is adjusted by RESET LEVEL control R114 in the grid circuit of the cathode follower.

c. In order to initiate a sweep after the sweep circuit has been reset, a positive start pulse is applied to the cathode of tube V10B, cutting off that tube and causing V10A to conduct. The process involved is identical to that described for the resetting process except for the different tubes involved. When V10B is cut off, its plate voltage is high, the input voltage to the cathode follower is positive, the output of the cathode follower is also positive, the reset diode in the sweep circuit is nonconducting, and the sweep begins.

115. Sweep Generator

a. An equivalent circuit of the sweep generator is shown in figure 55. The resistor, R and capacitor, C, are fixed, and the input voltage, E_{in} , is supplied by the positive reference voltage. The output voltage of such a circuit is $E_{out} = \frac{-t}{RC} \cdot E_{in}$ when the gain of the amplifier is much greater than one. In this case the gain of the amplifier is approximately 10,000, and therefore this relation is valid. If the reference voltage were constant, the output voltage would vary linearly with time. If, however, the input voltage were subject to variation, the corresponding

variation of the output voltage would be proportional but would be in the opposite direction. The equipment takes advantage of this condition to cancel the effect of reference voltage variations which would otherwise cause serious encoding errors.

b. If the input voltage E_{in} is applied when the initial charge on capacitor C is zero, the capacitor begins to charge exponentially toward the input voltage. As the capacitor charges, the amplifier input voltage begins to go positive and the output voltage begins to go negative. As the output voltage of the amplifier goes negative, the charging current through the capacitor is prevented from charging exponentially because the charging current via the resistor, and that from the amplifier output, aid each other. Under these circumstances, the charge on the capacitor and the sweep generator output voltage vary linearly with time.

c. To terminate the linearly varying output voltage, a reset voltage (par. 114) is applied directly to the amplifier input through a relatively low resistance circuit, and, at the same time, the feedback capacitor is shunted by a low resistance so that the amplifier output voltage is forced to assume a value dependent upon the amplitude and polarity of this applied voltage. In order to obtain a sweep voltage that varies above and below ground potential, a negative rather than a zero reset voltage is used. By using a voltage of the proper value, the sweep circuit is reset to an output level of approximately +55 volts (D of fig. 25). The sweep circuit is enabled by the removal of the reset voltage (C of fig. 25), thus allowing the charge on the capacitor to change as described previously. The sweep voltage then continues to a level of approximately -55 volts, at which point the sweep is terminated by application of the negative reset voltage. The exact value of the reset level is controlled by the amplitude of the negative portion of the reset voltage. The slope of the sweep voltage may be changed by changing the constants of the RC circuit of the sweep generator.

d. A simplified circuit of the sweep generator and reset diode circuit is shown in figure 56. The resistor and capacitor in figure 55 are replaced by the components in the Z1 integrating network. As a result of the need to control the slope of the sweep voltage more readily, the configuration of the network is more complicated than the RC

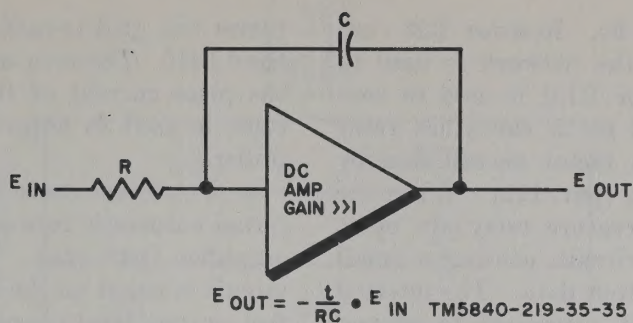
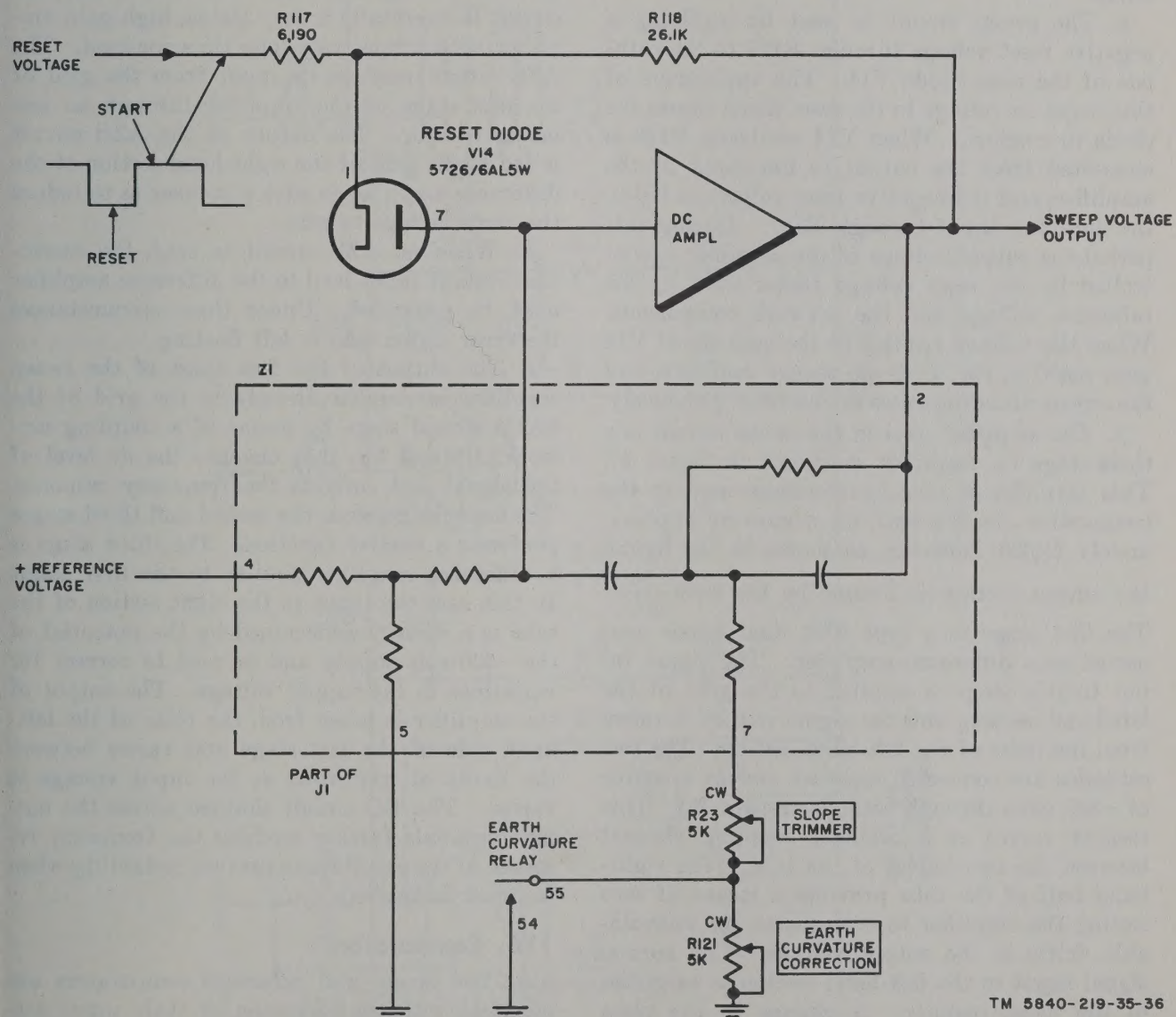


Figure 55. Sweep generator, equivalent circuit.



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Figure 56. Sweep circuits, simplified schematic.

network shown in figure 55. Resistor R23 connected to terminal 7 of the network is used to adjust the slope. Resistor R121 is used in connection with an external earth curvature relay to introduce a correction factor necessitated by the curvature of the earth (par. 111). When the contacts of the earth curvature relay are open, R121 is inserted in the circuit, causing a small change in the encoded output data. The internal resistor, terminal 5 of Z1, connected to ground causes the sweep rate to be such that the number of encoder output pulses per encoding cycle is 1,024 when the dc analog voltage input is maximum.

e. The sweep circuit is reset by applying a negative reset voltage through R117 to the cathode of the reset diode V14. The application of this negative voltage to the reset diode causes the diode to conduct. When V14 conducts, R118 is connected from the output to the input of the amplifier, and the negative reset voltage is fed to the amplifier input through R117. During this period the output voltage of the amplifier is controlled by the reset voltage rather than by the reference voltage and the network components. When the voltage applied to the cathode of V14 goes positive, the diode no longer conducts, and the sweep circuit operates as described previously.

f. The amplifier used in the sweep circuit is a three-stage dc amplifier as shown in figure 57. This amplifier is identical to those used in the comparator circuits and has a gain of approximately 10,000; however, as shown in the figure, the output voltage is limited by the term $\frac{-t}{RC}$.

The first stage is a type 5755 dual triode connected as a difference amplifier. The signal input to this stage is applied to the grid of the left-hand section, and the signal output is taken from the plate of the left-hand section. The two cathodes are connected together and to a source of -300 volts through cathode resistor R3. This resistor serves as a common coupling element between the two halves of the tube. The right-hand half of the tube provides a means of zero setting the amplifier to compensate for unavoidable drifts in the output voltage. The normal signal input to the left-hand section is amplified in the usual manner. A change in the plate current through the right-hand half of the tube causes a change in the total current through the common cathode resistor. This change in current

varies the grid-to-cathode potential of the left-hand half. The zero set control R7, which varies the plate current of the right-hand half of the tube, is used to adjust the zero set of the amplifier.

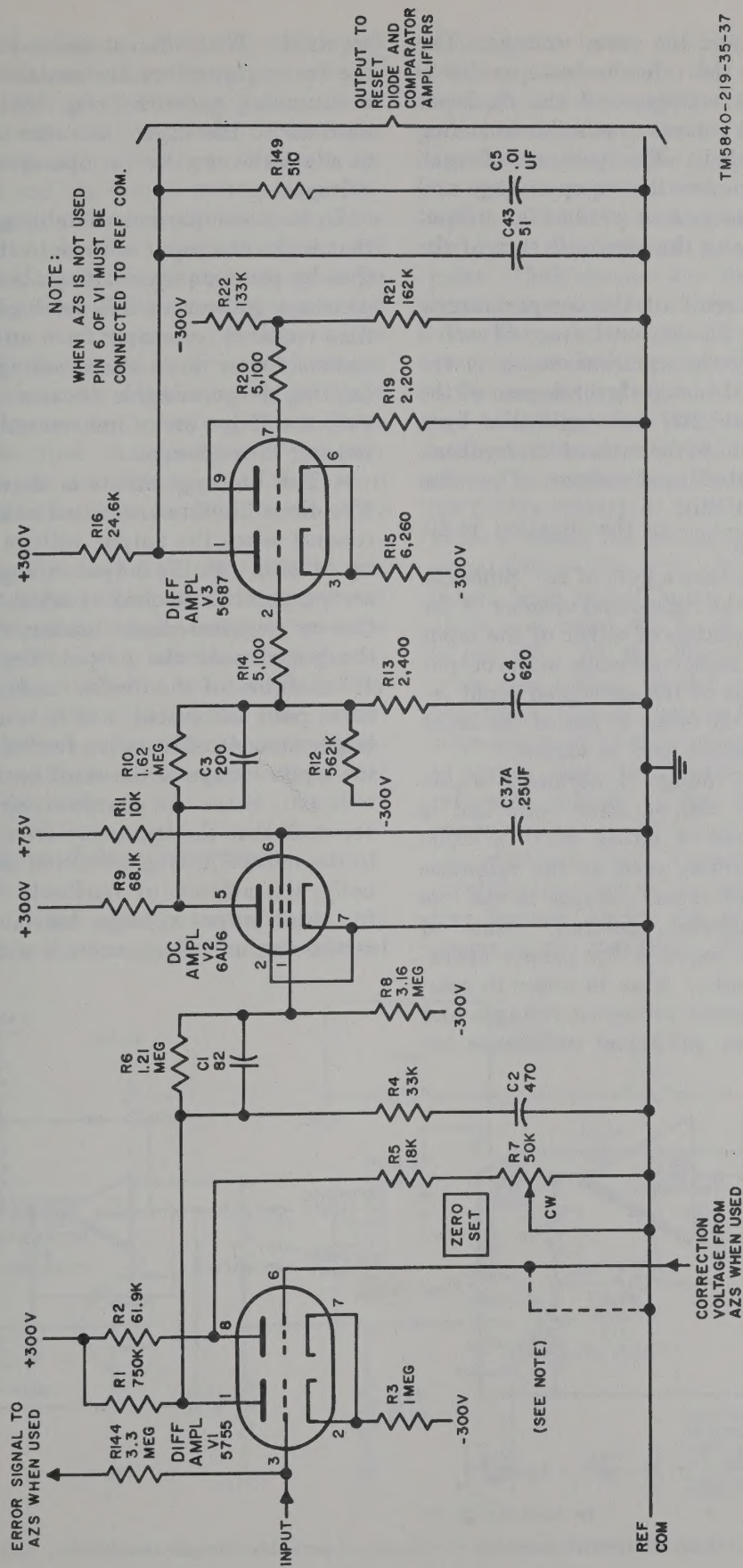
g. Provisions have been made to use an external automatic zero set (AZS) circuit with this amplifier (par. 133). The operation of the AZS circuit is based on the fact that, when the amplified output level changes due to amplifier drift, the input voltage also changes due to the feedback circuit. Thus, the average value of the input voltage may be used as a measure of the amount of amplifier drift or error. The AZS circuit is essentially a very stable, high gain amplifier with a relatively long time constant. The AZS circuit receives its input from the grid of the first stage of the amplifier through an isolating resistor. The output of the AZS circuit is fed to the grid of the right-hand section of the difference amplifier in such a manner as to reduce the error voltage to zero.

h. When no AZS circuit is used, the correction voltage input lead to the difference amplifier must be grounded. Under these circumstances the error signal lead is left floating.

i. The output of the first stage of the sweep amplifier is coupled directly to the grid of the 6AU6 second stage by means of a coupling network, R6 and C1, that changes the dc level of the signal and corrects the frequency response. The network between the second and third stages performs a similar function. The third stage is a difference amplifier similar to the first stage. In this case the input to the right section of the tube is a voltage determined by the potential of the -300-volt supply and is used to correct for variations in the supply voltage. The output of the amplifier is taken from the plate of the left-hand side of the last stage and varies between the limits of ± 60 volts as the input voltage is varied. The RC circuit shunted across the output terminals further modifies the frequency response of the amplifier to prevent instability when feedback is applied.

116. Comparators

a. The target and reference comparators are identical with the exception of their input networks. The amplifiers used in the comparator are the same as the one used in the sweep generator (par. 115f). Each comparator has two in-



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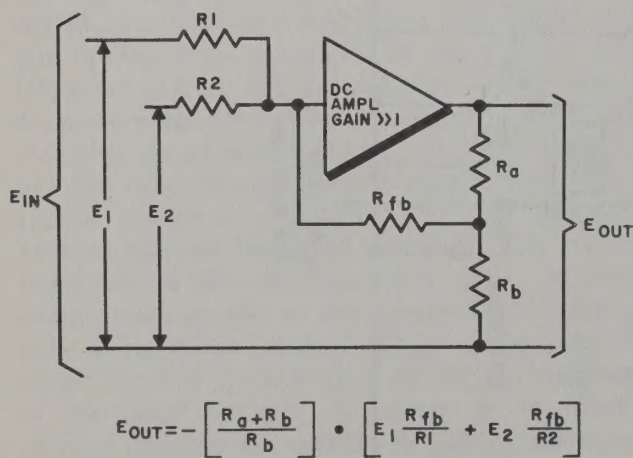
Figure 57. Sweep amplifier, schematic.

puts: a dc voltage and the sweep voltage. The dc voltage input to the reference comparator is the minus reference voltage, and the dc input voltage to the target comparator is the dc analog voltage to be encoded. The purpose of each comparator is to compare the sweep voltage and the dc input voltages and to produce an output signal corresponding to the algebraic sum of the two.

b. A simplified circuit of the comparators is shown in figure 58. The output voltage of such a circuit, expressed by the equation shown in the figure, is proportional to the algebraic sum of the input voltages E_1 and E_2 , each multiplied by a weighting factor equal to the ratio of the feedback resistor to the associated input resistor. The value of the term $-\frac{(R_a + R_b)}{R_b}$ in the equation is 20,

causing the circuit to have a gain of 20. Since the minus sign precedes the right-hand member of the equation, a positive change of either of the input voltages results in a negative change in the output voltage. If the value of the associated input resistance is changed, the effect of one of the input voltages upon the output may be varied.

c. The dc analog voltage is normally within the range of either ± 50 or ± 100 volts and is derived from a source of either ± 250 or ± 300 volts. The latter is also used as the reference voltage. Since the dc input voltages to the two comparators are different, different values of series resistances are required for proper operation of the two circuits. Also, in order to compensate for the different reference voltages and target voltage ranges, additional resistances are



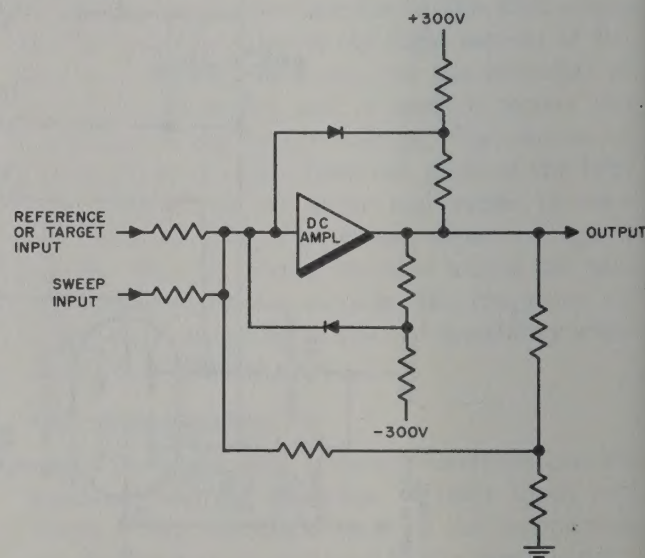
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Figure 58. Comparator, equivalent circuit.

required. The different resistances required for the two comparators are contained in the input, or summing networks (fig. 164(1)). The connections to the input networks may be changed to adapt the encoder for operation with different voltages.

d. Each comparator contains a limiting circuit that limits the input voltage to the amplifier and thereby prevents overloading the amplifier. It is necessary to prevent this overloading because the time required to recover from an overload would seriously slow down the encoding process. Such limiting is permissible because the comparator output voltages are of interest only when they are passing through zero.

e. The limiting circuit is shown in figure 59. The diode limiters are biased so that they do not conduct when the output voltage is in the vicinity of zero. As the output voltage deviates from zero, a point is reached at which either the positive or negative diode limiter, depending upon the polarity of the output, begins to conduct. When either of the diodes conducts, a new feedback path is created which results in a much larger amount of negative feedback. This causes the input voltage of the amplifier to be materially reduced. Since the characteristics of the diodes are such that the transition from the conducting to the nonconducting condition takes place gradually, the amount of feedback varies somewhat for small output voltages but increases radically as the output voltage exceeds a definite value.



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Figure 59. Comparator limiter, equivalent circuits.

g. Capacitors C46 and C47 (fig. 164(1)) are connected from output to input of the target and reference comparators, respectively, to provide an adjustment of the delay introduced by the individual amplifiers. The delays introduced by the amplifiers must be equal if the time difference between the two output signals is to represent the difference between reference voltage and target voltage precisely.

(fig. 60)

The schematic diagram illustrates the internal circuitry of the coincidence pulse generator and its connection to the gate control multivibrator. It features two vacuum tube sockets, V7A (1/2) 12AX7 and V7B (1/2) 12AX7, which serve as the coincidence pulse generator and pulse generator, respectively. The circuit is powered by a +300V supply and a -300V supply. Key components include resistors R122 (10K), R124 (50K), R125 (3.16 MEG), R126 (100K), R127 (100K), R128 (287K), R129 (61.9K), R130 (22K), R131 (22K), R132 (100K), and R133 (100K). Capacitors C33 (510) and C34A (.5UF) are also present. A transformer T2 is used for signal coupling. A diode CR8 (1N67A) is connected to the output of the pulse generator. A control line, labeled 'GATE CLOSE PULSE TO GATE-CONTROL MULTIVIBRATOR', is shown with a pulse waveform. A 'TARGET THRESH ADJ' control is connected to the circuit. The diagram includes a legend for equipment marking and a list of notes.

NOTES:

- UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
- INDICATES EQUIPMENT MARKING.

NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. INDICATES EQUIPMENT MARKING.

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b. The circuit of the target-coincidence pulse generator is shown in figure 60. The input signal is the target level signal (G of fig. 25), which is fed to the grid of V7A through resistor R122 and potentiometer R124, the threshold adjustment. In connection with R125 and R122, TARGET THRESHOLD ADJUST control R124 provides a means for adjusting the dc level of the signal fed to the grid of the tube. When the target level signal input is positive, V7A conducts, and when the input is negative, the tube is cut off. At the beginning of an encoding cycle, the output of the comparator is always negative. This is because the sweep voltage always starts out at approximately +55 volts, which is higher than the effective value of either the reference voltage or the target voltage at the comparator amplifier input (D of fig. 25). Since the resultant input voltage to the comparator amplifier is positive, the output voltage is negative because of the use of an odd number of stages in the amplifier. Thus, at the beginning

Figure 60. Encoder target coincidence pulse generator, schematic.

of each encoding cycle V7A is cut off. As the sweep voltage approaches a level opposite in polarity but equal in magnitude to the dc analog input voltage, the target comparator output voltage changes in a positive direction, passes through zero when the two comparator inputs cancel exactly, and then continues in a positive direction until the positive limit is reached. Since this action occurs very rapidly, V7A is driven from cut off to conduction very rapidly. Conduction occurs at very nearly the same time that the comparator inputs cancel, the precise time of conduction being controlled by the setting of TARGET THRESHOLD ADJUST R124.

c. During the time that V7A is cut off, V7B conducts because of the direct coupling from the plate of V7A and because the plate voltage of V7A is high during this period. When the first tube is driven to conduction by the target level signal, however, V7B is cut off and its plate current rapidly becomes zero. This sudden change in the plate current causes a large voltage to be induced in the secondary of pulse transformer T2. The characteristics of this transformer are such that the secondary voltage is in the form of a very short pulse. The polarity of this pulse is negative with respect to ground because of the transformer connections.

d. In order to eliminate any overshoot of the transformer output pulse due to resonant effects in the transformer itself, diode CR8 is inserted in the circuit to ensure that only the negative portions of the transformer output pulse appear on the output lead. Resistor R133 is necessary to provide a dc path to ground for the currents flowing through the diode. Resistor R132 is shunted across the primary of the transformer to provide damping and thereby assist in eliminating overshoot and any spurious pulses that otherwise might occur. Capacitor C33 is used to improve the speed of operation of the circuit by enabling rapid changes in the plate voltage of V7A to be coupled directly to the grid of V7B.

118. Pulse Gate Circuits

(fig. 61)

a. The pulse gate circuits control the number of 100-kc pulses produced by the encoder in response to the gate-open and gate-close pulses received from the reference and target-coinci-

dence pulse generators. The time difference between the gate-open and gate-close pulses is proportional to the value of the target analog voltage; therefore, the number of 100-kc output pulses allowed to pass through the pulse gate is also proportional to the target analog voltage.

b. The gate-control pulses are used to trigger the gate control multivibrator to either the gate-open or the gate-close condition. A voltage from the gate-control multivibrator is then fed through a cathode follower and is used to bias a diode gate circuit so that the diode either conducts or does not. Pulses from the 100-kc pulse generator are applied to this gate, and, if the gate is open, these pulses are allowed to pass to the encoder output terminal.

c. The gate-control multivibrator is a conventional Eccles-Jordan bistable circuit composed of tubes V9A and V9B and their associated components. In such a circuit one of these tubes conducts while the other tube is cut off. The circuit may be triggered to the opposite condition by the application of a negative bias to the grid of the tube that is conducting.

d. The pulse gate circuits are so arranged that the gate is open when V9B is conducting and closed when V9A is conducting. When V9A is conducting, the output voltage at the plate of V9B is high, and when V9B is conducting, the output voltage at its plate is low.

e. The output of the multivibrator is fed to the grid of the gate-control cathode follower V16A through resistor R88. R88 in conjunction with R89 lowers the dc level of the voltage fed to the grid of V16A. During the period when the gate is closed, the grid voltage on the cathode follower is positive, causing its output voltage to be positive also. When the gate is open and V9B is conducting, the grid voltage of V16A is negative, and its cathode voltage drops to a negative value determined by the current through the voltage divider R90-R91. The diode CR6 conducts when the cathode of V16A is negative, and does not conduct when the cathode is positive.

f. Transformer T1 continuously supplies negative 100-kc pulses to the pulse gate circuit from the 100-kc pulse generator circuit. The negative portion of these pulses is allowed to pass through CR10 and appears across R93. The pulses appearing across R93 are fed to the pulse gate CR6

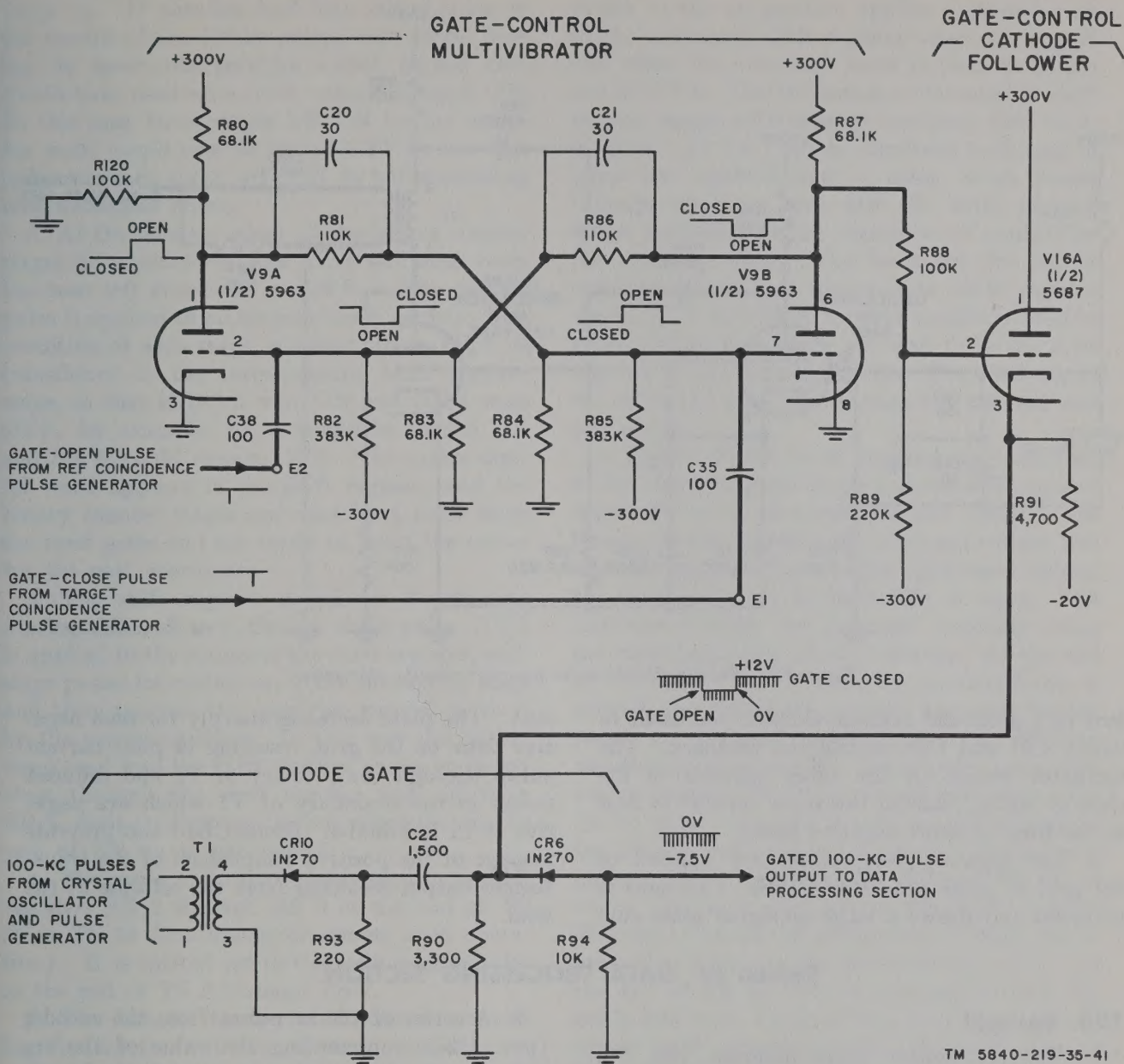


Figure 61. Encoder pulse gate circuits, schematic.

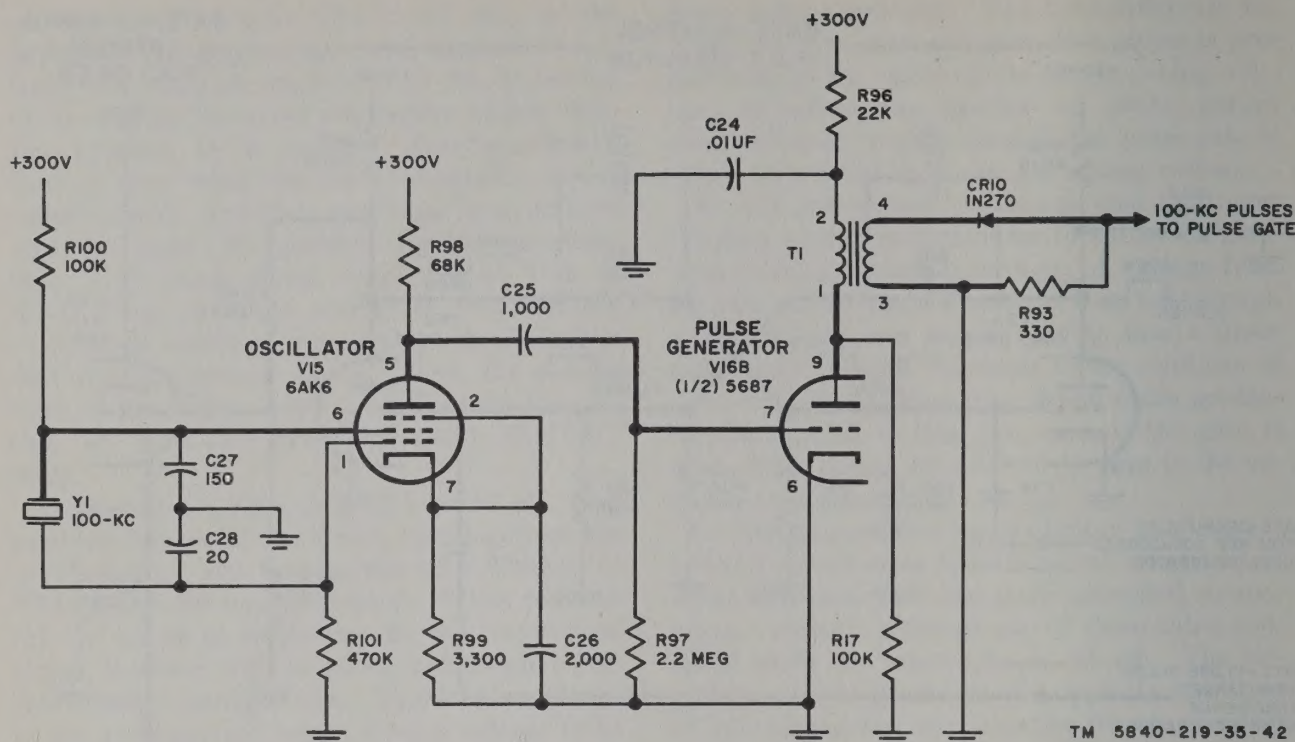
by way of C22. When the cathode of V16A is positive, CR6 is biased in the reverse direction, and the pulses are not allowed to pass through. When the cathode of V16A is negative, the negative pulses pass through CR6, appearing across R94. The time constants of this circuit are such that the gate opens and closes in less than two microseconds. The pulses appearing across R94 are the encoder output pulses, which are negative-going and have a peak amplitude of approximately 8 volts.

119. 100-kc Pulse Generator Circuits

a. The 100-kc pulse generator (fig. 62) continuously supplies negative-going 100-kc pulses to the pulse gate circuit. The generator consists of a 100-kc crystal oscillator, V15 and pulse generator V16B.

b. The 100-kc quartz crystal is connected between the screen grid and control grid of V15, which act in this case much as the anode and control grid of a triode. The circuit is equiva-

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Figure 62. Encoder 100-kc pulse generator circuits, schematic,

lent to a grounded cathode Colpitts oscillator in which C27 and C28 control the feedback. The oscillator section of the tubes operates in the class C region, causing the plate current to flow in the form of short negative pulses.

c. The negative-going pulses are applied to the grid of pulse generator V16B. This tube is unbiased and draws a large no-signal plate cur-

rent. The plate decreases sharply for each negative pulse on the grid, resulting in plate current pulses through the primary of T1 and induced pulses in the secondary of T1 which are negative at T1 terminal 4. Diode CR10 also prevents passage of the positive components of the transformer output resulting from the collapse of the field.

Section IV. DATA PROCESSING SECTION

120. General

a. The transmitter block diagram (fig. 81) shows the data processing section as a number of blocks, representing the active gates, binary counters, and shift registers. Figure 26 shows a condensed block diagram of the same elements illustrating that the parallax correction is added to the binary counters in parallel, the 100-kc count pulses are applied to the binary counters serially, the contents of the binary counters are passed to the shift registers in parallel, and the shift register shifts the data out to the output section serially. It also shows that the auxiliary data and the ready and sync pattern are passed to the shift registers in parallel and are shifted out of the shift registers serially.

b. A series of 100-kc pulses from the encoder (par. 113e), representing the value of the encoder coordinate voltage, is applied to the binary counters. Thirteen stages of binary counters are used, and each stage divides the number of pulses it receives by 2. If BC 1 receives 512 pulses at its input, its output is 256 pulses; the next stage, BC 2, receives 256 pulses at its input, and supplies 128 pulses at its output. If a stage counts an odd number of pulses, the last pulse it counts leaves the stage turned ON. If a stage counts an even number of pulses, the last pulse leaves the stage turned OFF. In this manner, the stages of the binary counter at the completion of the count are left turned ON or OFF to form a binary word of ONE's and ZERO's

(app. I). If parallax had been added prior to the receipt of the 100-kc pulses, each stage, having its associated parallax switch turned ON, would have received a clock pulse, turning it ON. In this case, those stages left ON by the parallax word would now be turned OFF by the first pulse to reach them, and ON by all succeeding even-numbered pulses.

c. At the moment when all the binary counter stages have completed the count and each stage has been left either ON or OFF, a data read-in pulse is applied to all stages simultaneously. The condition of each stage, whether ON or OFF, is transferred to the corresponding shift register stage, so that if BC 3 were ON and BC 4 were OFF, for example, SR 3 would be turned ON and SR 4 would remain OFF. The entire digital word appears in the shift register, and the binary counter stages are reset by a pulse from the reset gates and are ready to count the pulses for the next coordinate.

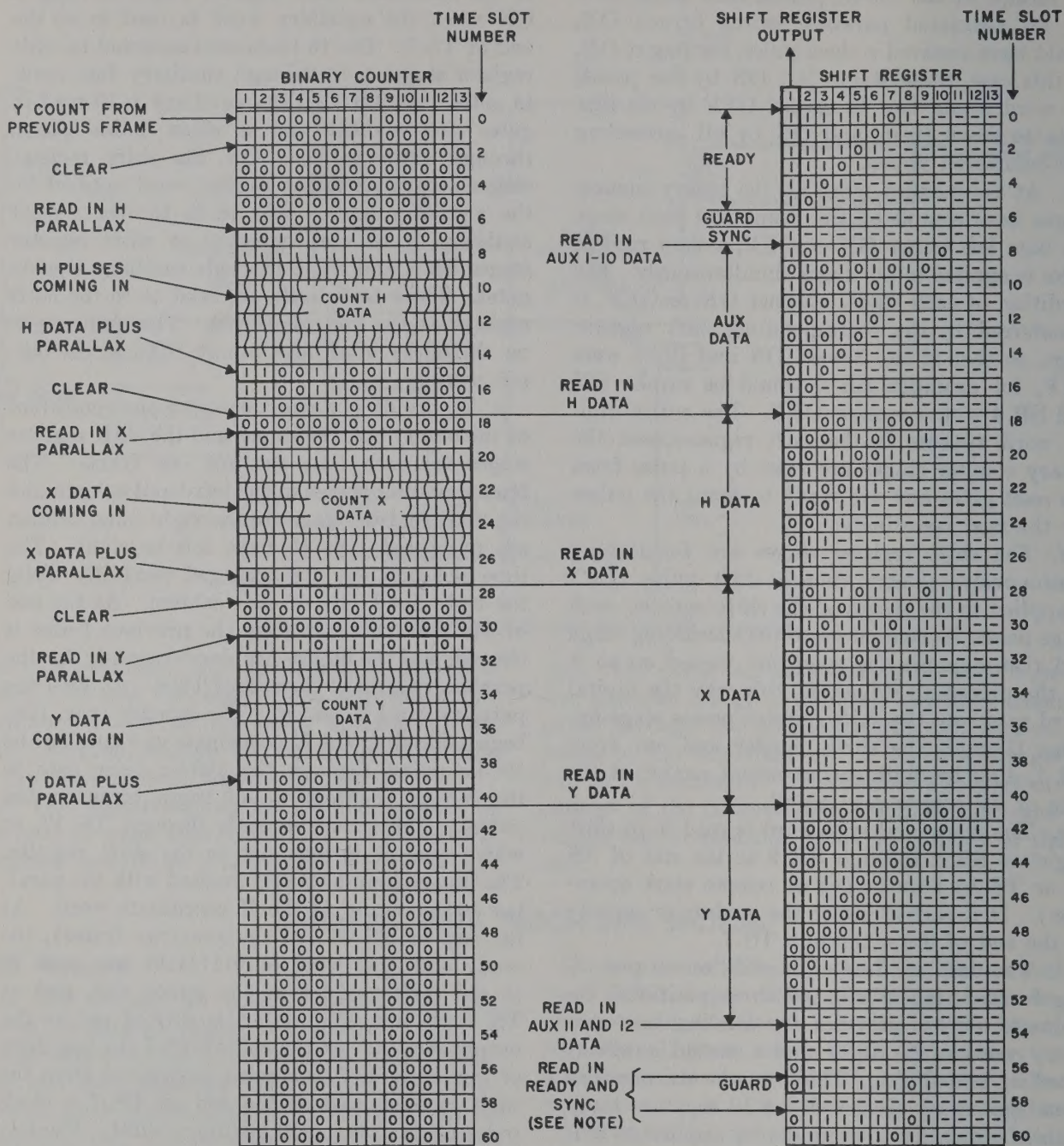
d. The shift register stages are functioning continuously. Every time a shift pulse (CP) is applied to the stages of the shift register, each stage passes its content on to the succeeding stage and then assumes the condition passed on to it by the preceding stage. In this way the digital word read into the shift register passes stage-by-stage through the shift register and out from SR 1, digit-by-digit, to the output section at the rate of 750 digits per second.

e. The ready and sync word is read in to shift registers SR 2 through SR 9 at the end of TS 56 or TS 58 (continuous or remote start operation). It is shifted out to the modulator serially at the end of TS 0 through TS 7.

f. The data set frame, in addition to providing for the transmission of three positional coordinate words, provides for sending one auxiliary word of 10 digits and a second auxiliary word of two digits. These words are obtained from associated equipment on 12 separate leads, each of which has a ground (+) applied to it if the digit associated with the lead represents a ONE. If the digit represents a ZERO, the lead has no bias (-) applied to it. During normal operation the auxiliary bias for each digit is obtained from associated equipment, or the first 10-digit auxiliary word can be set in by using the 10 auxiliary switches on the transmitter unit panel. With this arrangement, an auxiliary

switch in the up position applies a ground (+) to the associated shift register stage, turning it ON when the auxiliary word is read in at the end of TS 7. The 10 leads are connected to shift register stages 1-10 through auxiliary data read-in gates. At TS 7 all the auxiliary 1-10 read-in gates are enabled and a clock pulse passes through them to turn ON the shift register stages according to the digital word applied by the auxiliary leads. The leads for the 2-digit auxiliary word are connected to shift register stages SR 1 and SR 2 through auxiliary read-in gates. These two digits are read in to the shift register at the end of TS 53. The shift register shifts the word out through SR 1 to the output section.

g. Figure 63 is a chart showing the conditions of the binary counter stages and the shift register stages for each time slot for one frame. The binary counter stages in the left-hand column and the shift register stages in the right-hand column are numbered 1 to 13 from left to right. The time slot numbers are arranged vertically along the right-hand side of each column. At the end of TS 1 the Y count from the previous frame is cleared, and the binary counters are ready for the parallax read-in at the end of TS 6. At TS 7 the parallax word is read in. The encoder (par. 113) begins encoding the H coordinate and passing the 100-kc pulses through the 100-kc pulse gate to the binary counters which begin counting the pulses. The count proceeds through TS 17, at which time it is read out to the shift register. The binary counter stages proceed with the parallax and counting of the X coordinate word. At the end of TS 56 (of the previous frame), the ready and sync word of 011111101 was read in to the shift register at the guard slot, and at TS 0 the first digit ONE is shifted out to the output section. At the end of TS 7 the last digit of the ready and sync word has passed from the shift register, and at the end of TS 7 a clock pulse reads in the 1-10 auxiliary word. The last digit of this word is shifted out in time for the shift register to accept the H coordinate word from the binary counters at the end of TS 17. This process goes on in the same way through the X and Y coordinates and the 11, 12 auxiliary word to the end of the frame. The guard slot at the end of the frame is needed at the receiver for proper operation of the input section.



NOTE:

FOR CONTINUOUS OPERATION, READY AND SYNC IS READ-IN AT THE END OF TIME SLOT 56.
 FOR REMOTE-START OPERATION, READY AND SYNC IS READ-IN AT THE END OF TIME SLOT 58.

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Figure 63. Binary counters and shift register, transmitter data processing section, timing diagram.

121. Binary Counters

a. Figure 64 shows the basic elements of a binary counter. This figure shows only 2 of the 13 tandem stages used. The 100-kc pulses are fed directly into the bistable F/F (par. 100a) of the first stage. This first negative-going 100-kc pulse turns the F/F ON. The ON bias from the F/F enables the gate within the F/F which follows it. When this gate is enabled, it passes the succeeding negative-going 100-kc pulse. This pulse acts as a clock pulse to the following F/O (par. 101). The F/O fires to send a set zero pulse back into the F/F of the BC stage, turning it OFF, and on the succeeding BC stage where the pulse is inverted, turning its F/F ON. The F/F of the first BC stage is now in its original OFF condition and is ready to be turned ON by the next negative-going 100-kc pulse.

b. With the binary counter at rest and with no input pulses applied, the following conditions prevail (fig. 65):

- (1) Transistor Q1 of the F/F is in the OFF

condition and a negative pulse applied to the base is necessary to trigger it to the ON condition.

- (2) The voltage at the collector of the F/F is approximately -15 volts. This voltage is applied across R4 of the F/F, CR2 of the F/O, and R2 of the F/F, making the voltage at the anode of CR3 of the F/F approximately -12 volts.
- (3) Transistor Q1 of the F/O is in the OFF condition and requires a negative pulse applied to its base to trigger it into the ON condition.

c. When the first input pulse is applied to pin 4 of the F/F, it is developed across the primary of T1 and is coupled across T1 without a polarity reversal. This negative pulse is applied through CR6, C1, and R5 to the base of the transistor, overcoming the reverse bias and turning the transistor ON.

- (1) This same pulse is blocked from passing through CR3 by the bias applied to the

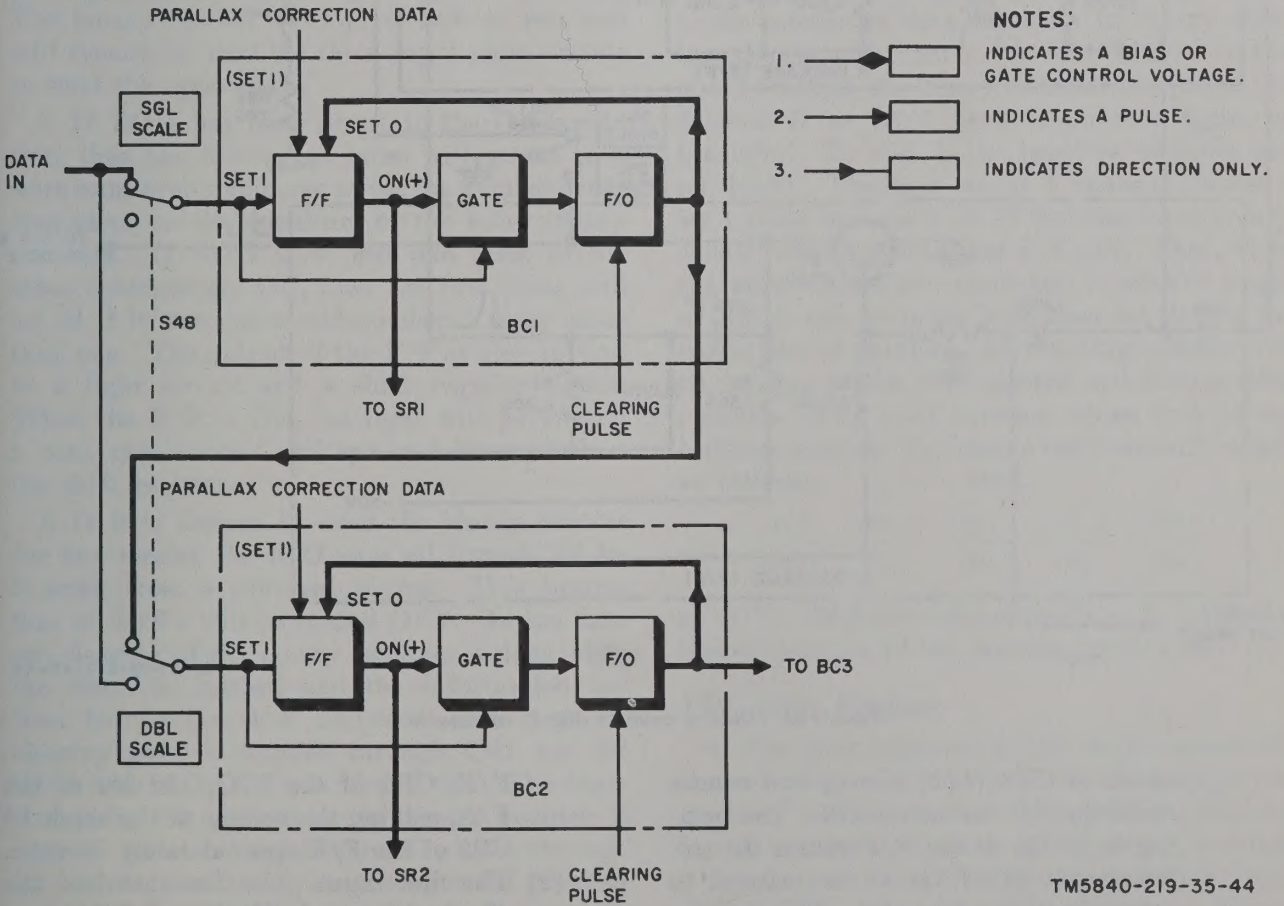
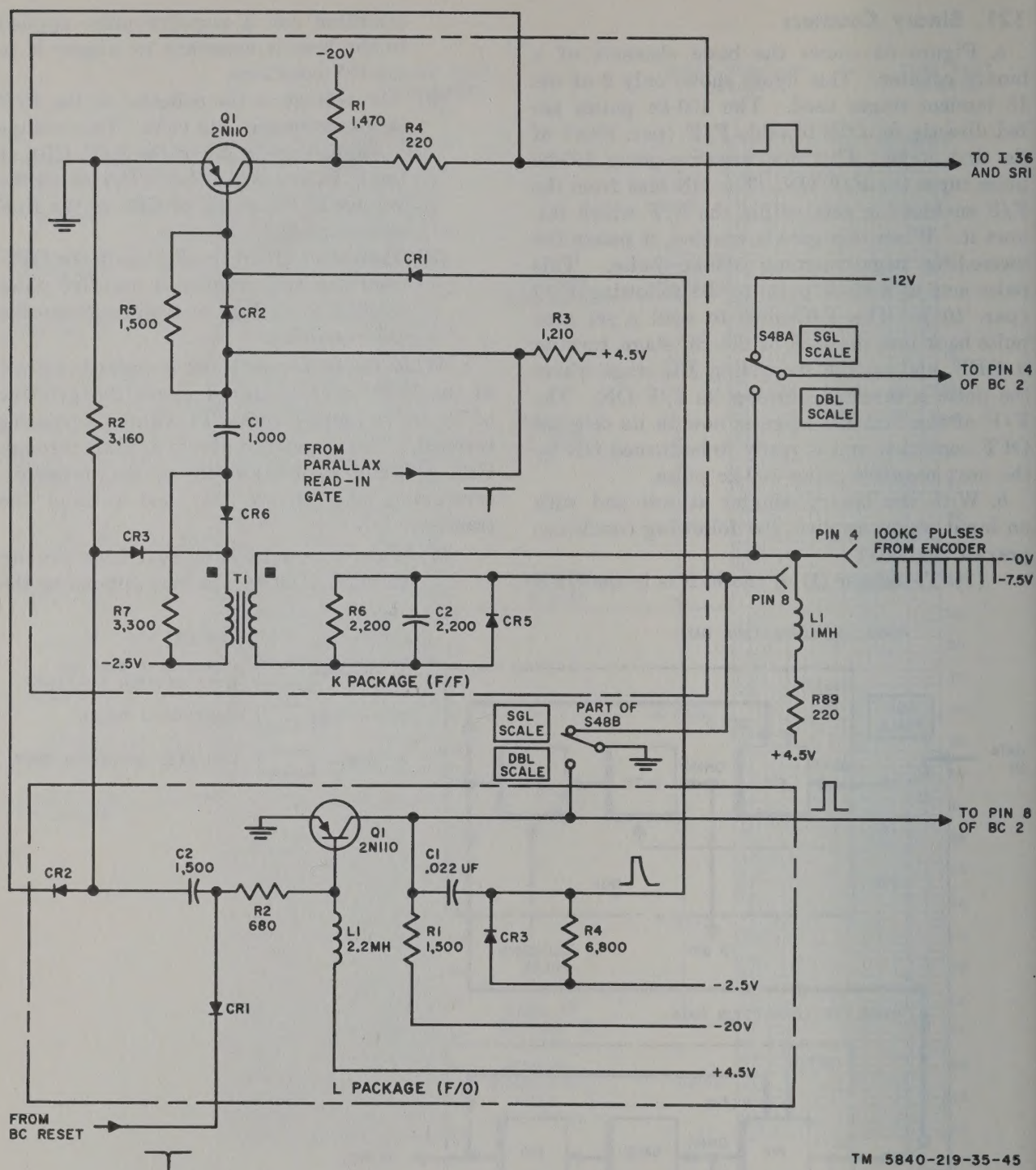


Figure 64. Binary counters, transmitter data processing section, simplified block diagram.



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Figure 65. Binary counter BC 1, schematic.

anode of CR3 (b(2) above) and cannot reach the F/O to turn it ON. The turning on of Q1 of the F/F causes the collector voltage of Q1 to be reduced to approximately -2.5 volts. This voltage will likewise be applied across R4 of the

F/F, CR2 of the F/O, and R2 of the F/F, making the voltage at the anode of CR3 of the F/F approximately -2 volts.

(2) The first input pulse has then had the effect of turning ON Q1 of BC 1 corresponding to a binary ONE and of

equalizing the potentials of the anode and cathode of CR3 of the F/F.

d. The second input pulse will find the conditions stated in c(2) above. This pulse will also be coupled across T1 and applied to the base of the F/F transistor. The negative pulse will have no effect on the F/F transistor as it is already in the ON condition; however, the negative pulse developed across the secondary of T1 will pass through CR3 of the F/F and C2 and R2 of the F/O to the base of Q1 of the F/O, turning it ON. The positive-going pulse output of the F/O is applied through CR1 to the base of the F/F transistor, turning it OFF. The output of the F/O is also applied to pin 8 of BC 2. Pin 8 in series with R6 is at the opposite end of transformer T1 from pin 4 and the pulse is therefore coupled across the transformer with polarity reversal so it will be of the correct polarity to turn ON the F/F of BC 2. The F/O will turn itself OFF in a period of time determined by its circuit constants. This is very short for the L package and somewhat longer for the C package. The binary counter (BC 1) is now at rest and will remain so until the third input pulse arrives to start the cycle again.

e. If BC 1 has been preset to the ON condition, then the first input pulse will act as if it were some even-numbered pulse, the number being dependent on the condition of the other binary counters. If BC 1 is at rest and some of the other counters are ON, then the first pulse will act as if it were some odd-numbered pulse other than one. The output of the F/F is also applied to a light circuit and a shift register circuit. When the F/F is ON, the light will go on and a bias, gate control, voltage will be applied to the shift register.

f. If it is desired to clear the binary counter for any reason, the F/O's are all turned ON by a pulse from a different source. This insures that all F/F's will be turned OFF. In the data set, clearing of the binary counters is done when the count is finished and the information has been fed to the shift registers. The negative clearing pulse is applied through CR1 and R2 to the base of the F/O, turning it ON. The negative pulse for presetting the binary counter is applied from the parallax read-in gate through R5 to the base of the F/F, turning it ON when an outside gating circuit is set for this to happen. This presetting is done just after the clearing

of the binary counter and just prior to the application of the input pulses from the encoder. The input pulses from the encoder have a prf of 100 kc and the number is determined by the amplitude of a voltage applied to the encoder.

g. The succession of events for five tandem-connected binary counter stages is illustrated in figure 66. In this figure it is shown that the F/F of BC 1 counts every other 100-kc pulse. BC 2 operates at one-half the frequency of BC 1, and the succeeding stage BC 3 halves the frequency again. For a decimal count of 25 100-kc pulses, the five stages are left as follows:

BC 1	BC 2	BC 3	BC 4	BC 5
ON	OFF	OFF	ON	ON

This corresponds to the binary number 10011. The data set stores the least significant digit at the left, which is the reverse of conventionally written numbers (appendix I). Written conventionally the above number would read 11001, which is the binary equivalent of the decimal 25.

h. Assume that a parallax of 5 is to be added to the coordinate data number. In binary notation the decimal number 5 is written 101. In the above example the binary counters completed the decimal 25 as 10011 (least significant figure at the left). To add 5, the parallax switches are set 10100. The keys set at 1 (closed) throw a set 1 pulse into the F/F of the associated binary counter stage, turning that F/F ON. Thus, when the 100-kc pulses are counted on a series of stages of which one or more have been set by the introduction of parallax, the resulting number will be the sum of the data number and the parallax number. With 5 of parallax added to a 25 coordinate number, the binary counters will be left as follows:

BC 1	BC 2	BC 3	BC 4	BC 5
OFF	ON	ON	ON	ON

or 01111. Written conventionally, it is 11110, the binary notation of the decimal number 30.

122. Shift Register

a. The basic elements of the shift register are shown in figure 67. Only 2 of the 13 stages are shown. As indicated in paragraph 120c, the binary number completed on the binary counters is at once gated into the shift registers by a single clock pulse. For each digit ONE in a binary stage, a ONE is read into the corresponding shift

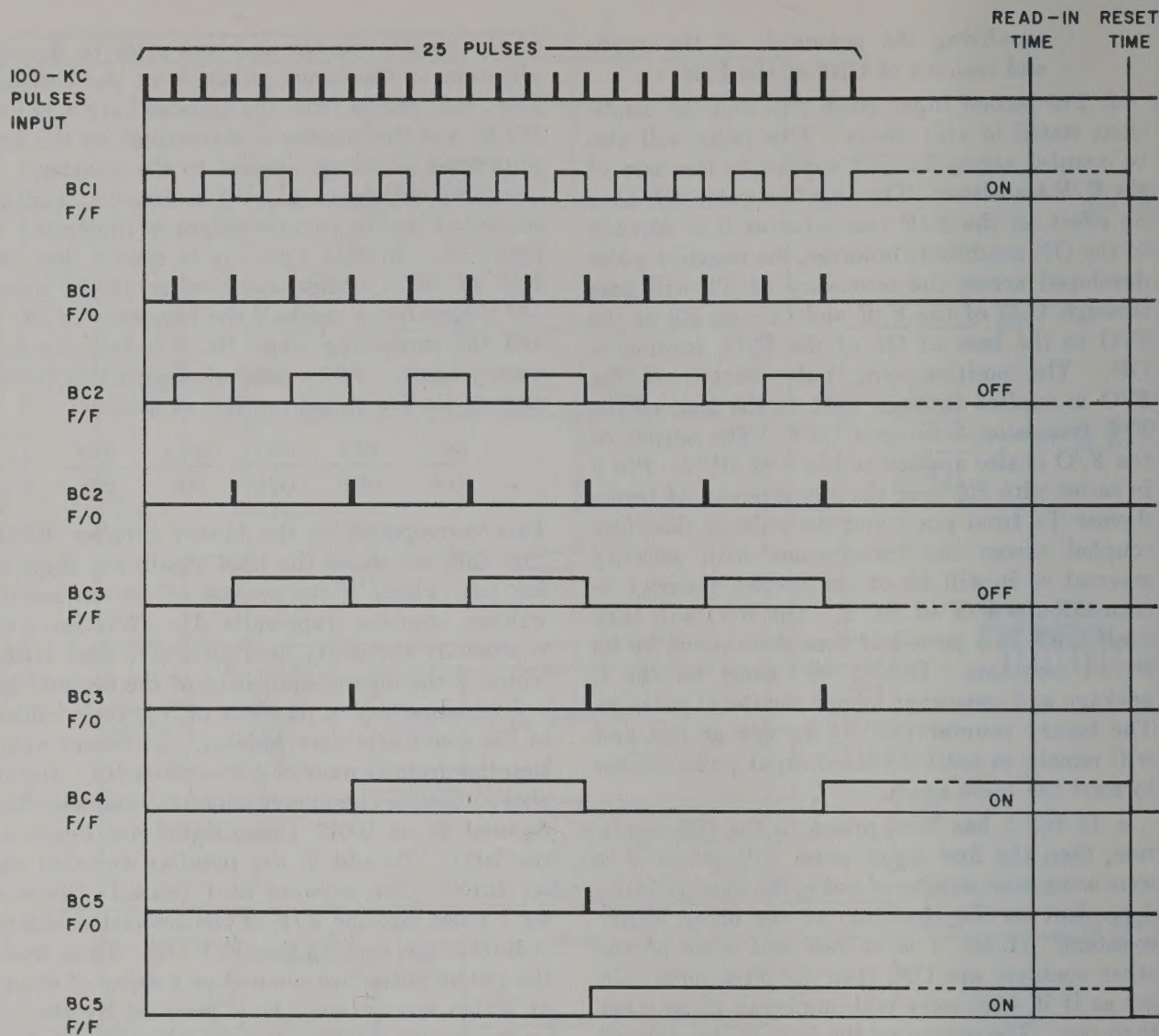


Figure 66. Binary counters, transmitter data processing section, timing diagram.

register stage, turning the F/F (par. 94c) of the SR stage ON. When a binary counter stage contains a ZERO, the coordinate data read-in gate associated with that stage is not enabled, and the SR F/F remains OFF. One output of the shift register stage is a memory circuit with a time constant long enough to store the enabling bias for a fraction of a time slot. The input to the stage is a time control gate which is enabled by bias received from the memory circuit of the preceding stage. If the gate is enabled, a shift pulse (CP) passes through the gate and turns the F/F ON.

b. On the transmitter block diagram (fig. 81) it is shown that the shift pulses are applied over a common bus to all 13 SR stages. Likewise the

set zero (SZ) pulses are applied to all 13 stages. The timing of these pulses is such that the SZ arrives to turn OFF all F/F's before the CP is applied to the gates. The time constant of the memory circuits is such as to remember the ON condition of its own F/F (if it had been ON) until the CP arrives at the gate of the succeeding stage. With this arrangement the SZ turns the F/F of all 13 stages OFF simultaneously, and the CP, arriving about 40 microseconds later, turns ON the F/F of each stage whose gate is held open by the memory circuit of the preceding stage. Thus the ONE's and ZERO's stored in the shift register stages, when the data is transferred into them from the binary counters, are read out from one shift register stage into the

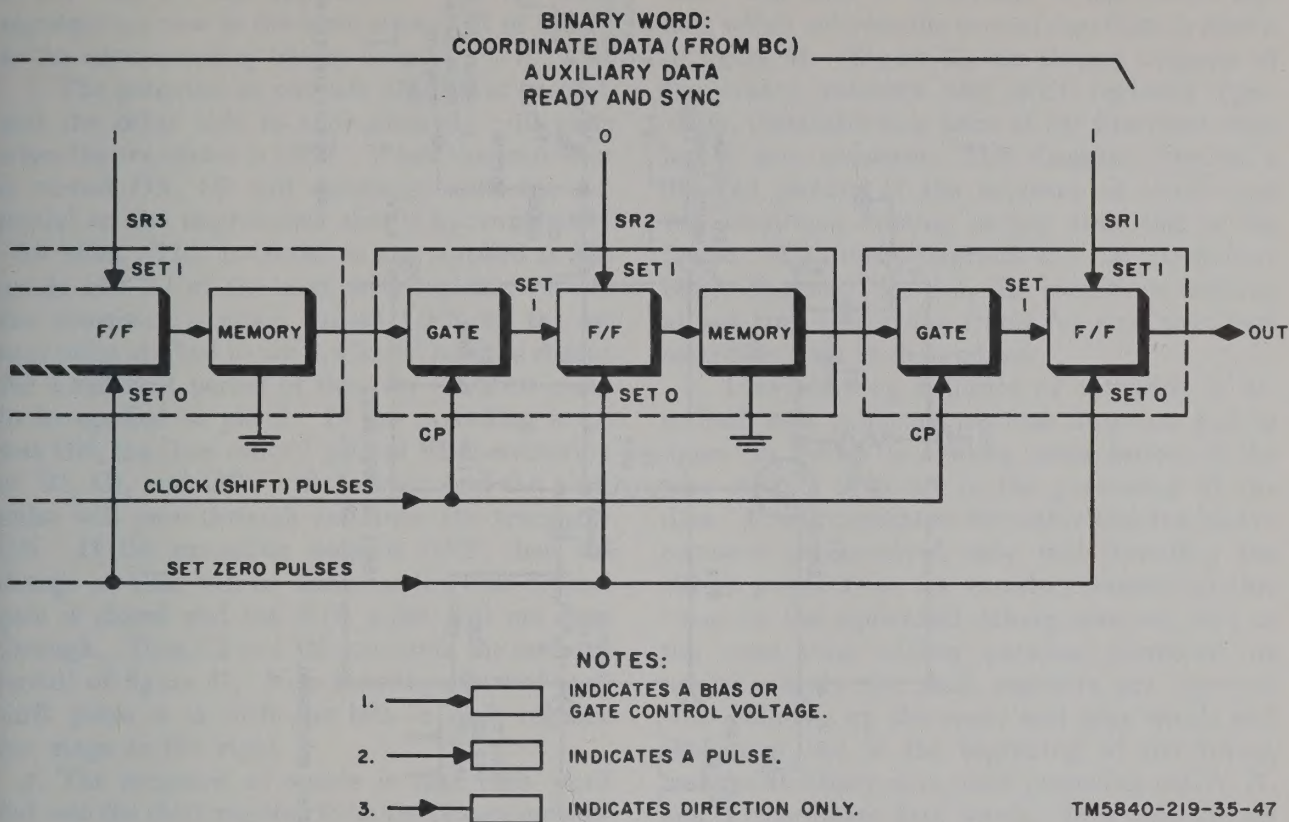


Figure 67. Shift register, transmitter data processing section, simplified block diagram.

next succeeding stage until all the digits are read out from SR 1 to the output section. The output is read out directly from SR 1 as the memory circuit is not used.

c. Two stages, SR 1 and SR 2, that are shown in block diagram form in figure 67 are shown schematically in figure 68. Those components shown inside the dotted lines comprise the gate, F/F, and memory circuit shown in the block diagram. The external gate is part of the data read-in circuitry. The numbers just outside the dotted lines indicate pin numbers on the plug-in package.

d. Assume that all of the shift register stages Q1 are in the OFF condition. In this case, the set zero and shift pulses will have no effect on the shift register. Gate control voltage from the corresponding binary counters is always applied to the time control gate shown connected to pin 7 of each A package. This voltage will be positive-going when the binary counter is ON and negative-going when the binary counter is OFF. The positive-going voltage is the gate opening voltage. The state of the gate control voltage is of im-

portance only at selected times during the transmission of the message. These times are when an input is received from the data read-in gate. This input is a negative-going pulse and is allowed to pass through the data read-in gate and be applied to the time control gate when it is desired to transfer the binary bits (which make up the binary word) from the binary counters to the associated shift registers.

e. When the negative-going pulse is allowed to pass through the time control gate by the gate control voltage, it will be applied to the base of the transistor through R2, overcoming the reverse bias applied from pin 10. The negative-going pulse will turn the transistor ON. The output of the transistor in SR 1 will be applied to the output circuit from pin 3 of the A package (in this case to the associated light and to the modulator). The output from pin 3 of SR 2 will be applied only to the light. The operation of SR 2 is identical to that of all the other shift registers except SR 1 and is identical to SR 1 except for the application of the outputs from pins 3 and 6. The output from pin 6 of SR 1

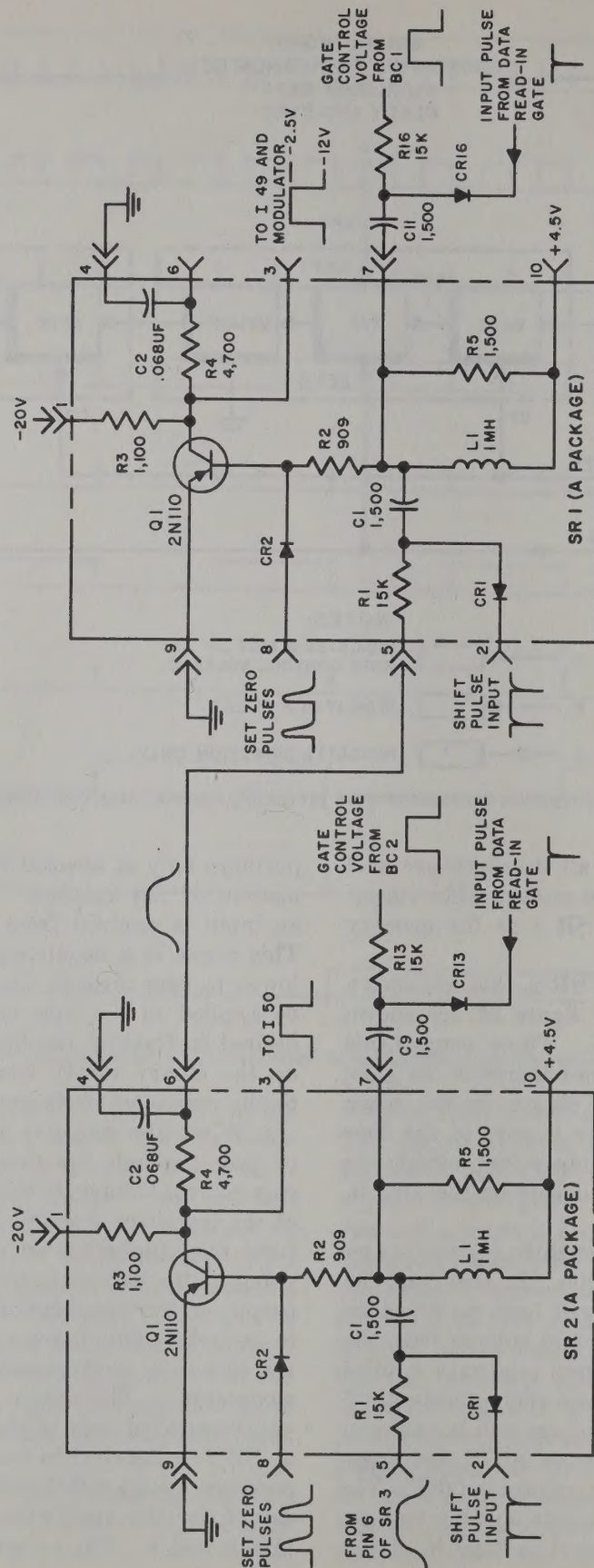


Figure 68. Shift register, schematic.

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is not used in this application. All the shift registers are now in the same state (ON or OFF) as the corresponding binary counter.

f. The potential on one side of C2 is at ground, and the other side is approximately -12 volts when the transistor is OFF. When the transistor is turned ON, C2 will discharge until the potential on the ungrounded side is approximately -2.5 volts. This potential is also applied to the anode of CR1 of the next shift register. When the transistor is again turned OFF by the set zero pulse applied to pin 8, C2 will hold its charge for a sufficient period of time for the shift pulse to be applied to pin 2. If the preceding stage was ON, the time control gate of SR 1 consisting of R1, C1, and CR1 will be open and the shift pulse will pass through and turn the transistor ON. If the preceding stage is OFF, then the charge on CR2 will be such that the time control gate is closed and the shift pulse will not pass through. Thus C2 and R4 constitute the memory circuit of figure 67. Note that the effect of each shift pulse is to shift the bits in each register one stage to the right.

g. The sequence of events is that each word fed into the shift register from the binary counter is shifted out, one bit at a time, to the output circuit, in this case I 49 and the modulator. If it were desired to feed a word into the shift register one bit at a time, the word could be transferred out all at once by furnishing gate control for another circuit. In this case, the output would be from pin 6.

123. Operation of Data Processing Section

a. The basic control elements provided for scheduling the functions to be performed by the binary counters and the shift registers are time control gates of the type described in appendix II. Some of these gates derive their enabling bias from selected time slot gates of the program generator. These gates serve the function of timing control. Others derive their enabling biases from elements signaling the information to be contained in the message. An example of these are the read-in gates for the coordinate and auxiliary data. These gates signal the shift registers whether the pulse to be passed to the line is a ONE or a ZERO.

b. Figure 2 shows the 58 time slots of the data set frame and designates the time slot numbers allocated to each element of the message to be

sent. The time of occurrence of the control signals which activate the several functions is shown in figure 69. Figure 63, the timing diagram of the binary counters and shift registers (par. 120*f*), illustrates how some of the functions overlap in time sequence. This diagram provides a detailed picture of the sequence of events and the conditions existing at any time slot in the frame. With these diagrams and the transmitter block diagram (fig. 81), the conditions existing at any time slot in the frame for any functional component can be determined.

c. The following sequence of operation is described with reference to these diagrams and to figure 70, which is a block presentation of the gate circuits involved in the processing of the data. It is important to remember that the binary counters are involved only with counting the 100-kc pulses from the encoder, translating this count to the equivalent binary number, and at the same time adding parallax correction as needed. Only the shift registers are involved with building up the ready and sync words and the guard slot at the beginning of the frame, and the auxiliary data word preceding the H, X, and Y coordinate data words. It is only during the counting and translation, and the shifting out of the coordinate data to the output section that both the binary counters and the shift registers are involved together. This being the case, the shift registers are available for 18 time slots before they are required to accept the first (H) coordinate data word from the binary counters. During this time they are used to build up the synchronizing pattern and the auxiliary data word.

d. Refer to figure 2, to the transmitter frame diagram (fig. 82), and to the transmitter block diagram (fig. 81). The synchronizing word consists of three time slots of a 600-cycle signal. Because the delay characteristics of the transmitter wire circuits to the receiver may be greater for 600 cycles than for 1,500 cycles, the ready tone control of the program generator is timed to release the 600-cycle tone at the end of TS 56. The ready and sync read-in gate applies a set one (ON) bias to SR's 2, 3, 4, 5, 6, 7, and 9 (D, fig. 70). Since SR 1 is skipped, the shift registers start the 1,500-cycle signal at the end of TS 57, the last time slot of the preceding frame. Thus, the shift registers, stepping under control of the shift pulses, apply six time slots of ON

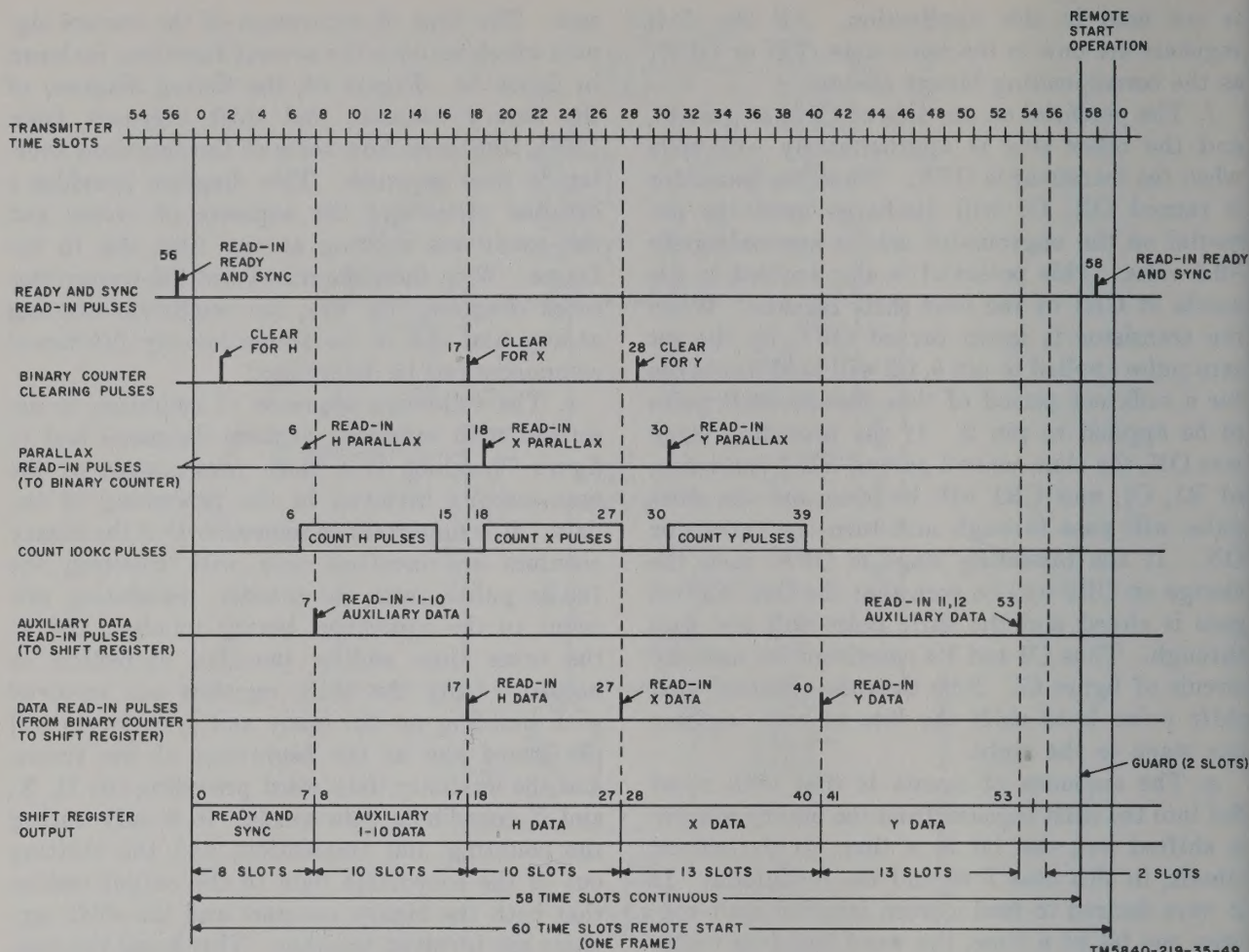


Figure 69. Transmitter data processing section, simplified timing diagram.

to the modulator followed by one time slot of OFF (note that SR 8 did not receive a set one bias) to provide the guard slot preceding the sync pulse which was sent into SR 9.

e. While the synchronizing word was being stepped out of the shift registers, other functions were being performed under control of the program generator section. The clock pulse at the end of TSG 1:

- (1) Reset the binary counters through the BC reset gate (fig. 70).
- (2) Operated the H coordinate lockup circuit (HRLU) in the coordinate multiplex section to apply the analog coordinate voltage to the encoder (fig. 53).
- (3) Operated the earth curvature relay lockup (ECRLU) so that the earth curvature correction would not be applied to the H coordinate (fig. 53).

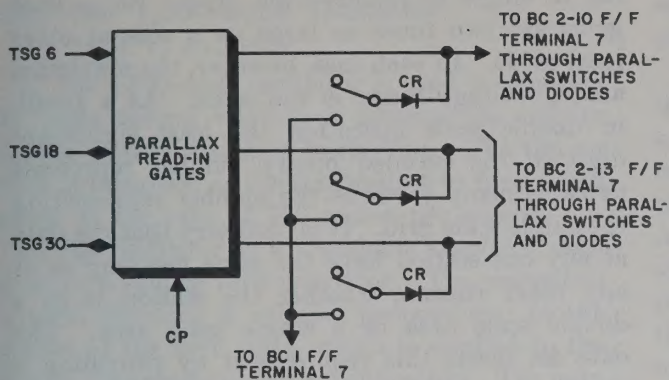
f. While the sync word is being sent to the

line, the clock pulse at the end of TS 6 is applied to the encoder control (ESP F/O) in the program generator section (par. 109) through the encoder start TCG to send a start pulse into the encoder reset multivibrator (par. 114). This pulse starts the sweep generator for the encoding of the H coordinate.

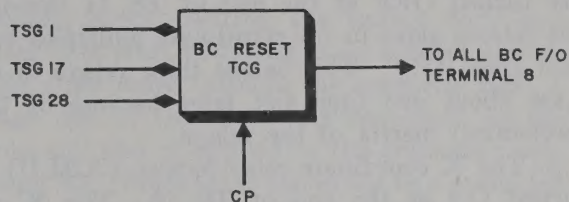
g. A clock pulse is also applied to the H parallax read-in gate (A of fig. 70) in the data processing section at the end of TS 6 to read H parallax into the binary counters.

Note. The encoder will not begin putting out pulses immediately, since the sweep generator goes from +55 to +50 volts before the pulse gate is open so that pulses can be fed into the encoder (par. 118). This requires less than one time slot but is long enough so that the parallax can be read into the binary counters and no confusion will be caused by parallax being applied to the binary counters simultaneously.

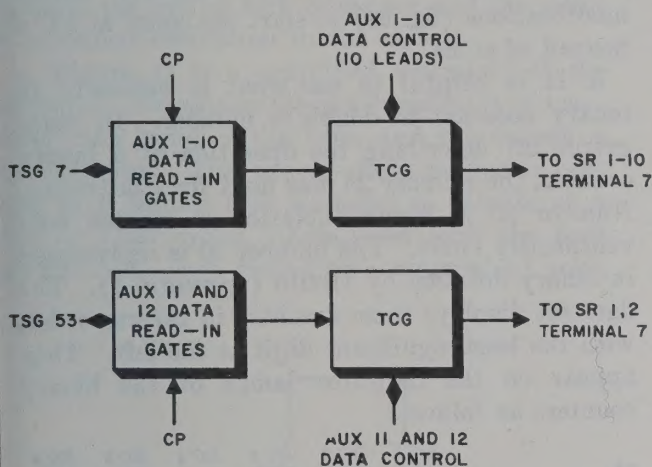
h. One time slot later, just as the sync signal is being completed at time slot 7, a clock pulse is



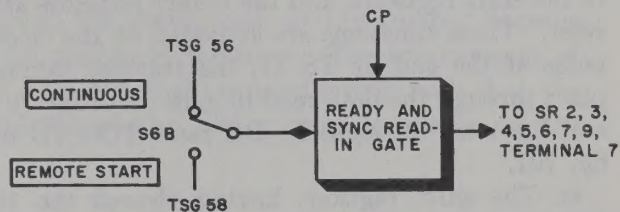
A. TYPICAL PARALLAX READ-IN GATES



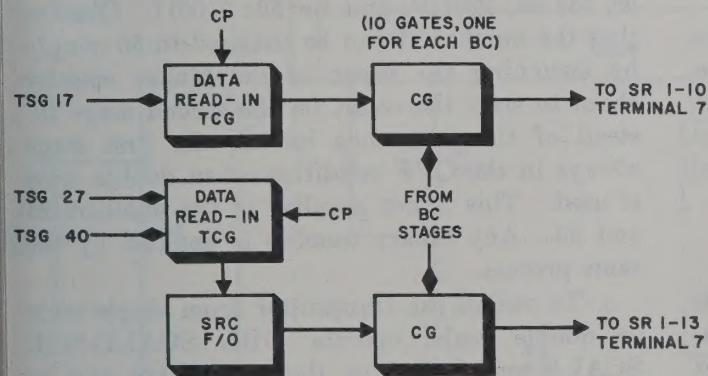
B. BINARY COUNTER RESET GATES



C. AUX DATA READ-IN



D. READY AND SYNC READ-IN GATES



E. DATA READ-IN GATES

- NOTES:
1. INDICATES A BIAS OR GATE CONTROL VOLTAGE.
 2. INDICATES A PULSE.
 3. INDICATES DIRECTION ONLY.

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Figure 70. Data processing section, time control gates, block diagram.

applied to the auxiliary data read-in gates which are enabled by TSG 7. These gates are biased according to the data appearing on the auxiliary data control leads, reading the data into the shift registers (C of fig. 70).

i. At this time, during the interval of time slots 8 to 17, inclusive, the auxiliary word is being

stepped out to the output section by the shift registers, and the encoder sweep generator is advancing to release 100-kc pulses to the binary counters. These counters will complete their count and will convert the number of 100-kc pulses to the corresponding binary number when the encoder is reset. The encoder is reset when

the clock pulse at the end of TS 15 is applied to the ERP F/O of the encoder control (par. 109).

j. The H coordinate relay lockup (HRLU) and the earth curvature relay lockup (ECRLU) are turned OFF at the end of TS 14 through the release gates in the coordinate multiplex section (par. 111). This causes these relays to release about one time slot later because of the mechanical inertia of the relays.

k. The X coordinate relay lockup (XRLU) is turned ON at the end of TS 16. The X coordinate relay closes its contacts about one time slot later to apply the X analog coordinate voltage to the encoder (par. 111).

l. Just as the X coordinate relay operates, or slightly earlier, the 10-digit H coordinate binary number is transferred from the binary counters to the shift registers, and the binary counters are reset. These functions are activated by the clock pulse at the end of TS 17, the transfer taking place through the data read-in gate (E of fig. 70) and the reset through the BC reset TCG (B of fig. 70).

m. The shift register, having cleared the 10 digits of the auxiliary data word at the end of time slot 17, can now accept the H coordinate word from the binary counters and step the H binary word out to the output section while the binary counters are counting the 100-kc pulses of the X coordinate.

n. The remaining sequence of events for the completion of the frame is similar to the above. Note on figures 70, 81, and 163(3) that the clock pulses for the H coordinate data read-in are not reinforced by SRC as are those for the X and Y coordinates.

124. Single Scale-Double Scale Feature

a. The discussion in this chapter up to this point has been concerned with single-scale operation of the data set. The data set is arranged for intercommunication between stations operat-

ing in single or double scale grids. Some local grids are two times as large on a side as other local grids. In each case, however, the maximum analog voltage range is the same. As a result, in double scale operation the least significant digit of the encoded binary number represents twice as many yards as the number representing the single scale grid. It is necessary that the data at any one station have the same meaning as at any other station, whether the station is in a double scale area or a single scale area. The data set meets this requirement by providing a single scale-double scale switch in the data processing section to effect the necessary circuit modifications (fig. 64) to start the count at BC 2 instead of at BC 1.

b. It is helpful to see what is necessary in binary notation to double a number. In paragraph 121 describing the operation of a binary counter, the number 25 was used for illustration. Number 25 in binary notation is written conventionally 11001. The number 50 is represented in binary notation by 110010 (appendix I). The data set displays these numbers in reverse order, with the least significant digit at the left. They appear on the indicator lamps of the binary counters as follows:

	BC 1	BC 2	BC 3	BC 4	BC 5	BC 6
25-----	ON	OFF	OFF	ON	ON	OFF
50-----	OFF	ON	OFF	OFF	ON	ON

or, for 25: 100110; and for 50: 010011. Observe that the number 25 can be changed to 50 simply by switching the input of the binary counter chain to start the count on the second stage instead of the first, thus leaving the first stage always in the OFF condition when double scale is used. This is not peculiar to the numbers 25 and 50. Any binary number is doubled by the same process.

c. To switch the transmitter from single scale to double scale, operate DBL SCALE-SGL SCALE switch S48 on the transmitter unit to DBL SCALE.

Section V. OUTPUT SECTION

125. Output Section

The output section contains two oscillators, one operating at 1,500 cycles, the other at 600 cycles, and their associated amplifiers. The output of each channel is connected through modulator

diodes to the output hybrid coil, through which it passes to the outgoing line. Each of the diode modulators is keyed by a transistor circuit. The block diagram (fig. 27) shows the arrangement of these elements.

126. The 1,500-Cycle Oscillator

(figs. 71 and 168)

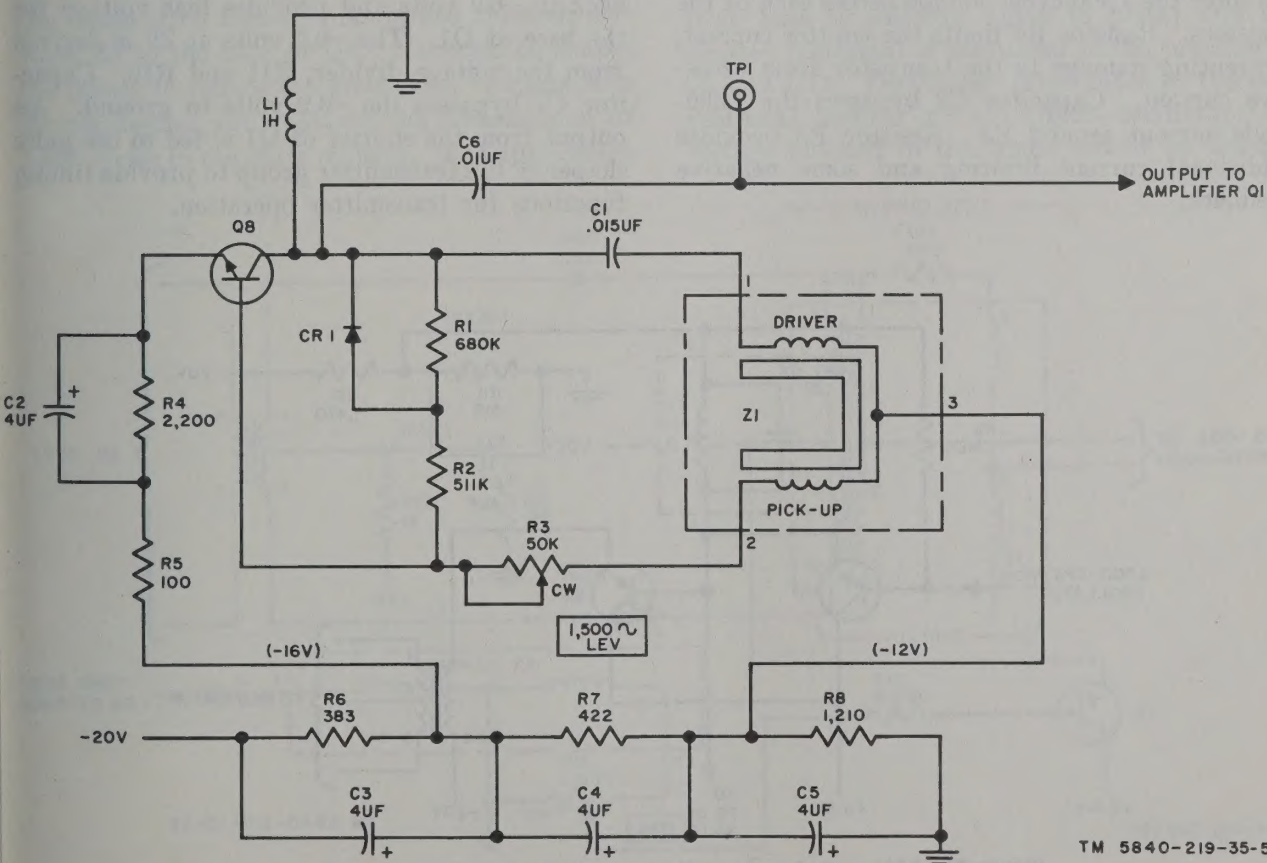
a. The 1,500-cycle oscillator is used to generate the basic timing wave that becomes the carrier for the transmitted data to the line. The timing wave is processed in the transmitter to form clock pulses at the rate of 750 pulses per second.

b. The oscillator is a transistor amplifier used to drive a tuning fork resonator. The resonator, in turn, develops a voltage, proportional to the motion of the fork tines, which is applied to the base of the transistor for amplification. The gain of the transistor amplifier is greater than the losses in the tuning fork resonator, and the result is sustained oscillation in the circuit.

c. Figure 71 is a simplified schematic of the oscillator. Transistor Q8 is a junction type transistor: the input is the base, and the output is the collector. The tuning fork resonator consists of a tuning fork adjusted to vibrate at a rate of 1,500 cycles. Associated with the fork are two coils, each wound on a magnetized yoke,

so arranged that the tines of the fork are in the magnetic fields of the yokes.

d. An initial impulse in the circuit caused by the application of voltage to the transistor causes a current to flow through the driver coil of the resonator, shock exciting the tuning fork and causing it to start vibrating at its natural period. As the tines move through the magnetic field, a voltage due to the motion is developed in the pickup coil and is applied to the transistor base through R3. Since Q8 is connected as a grounded emitter, a positive-going voltage at the base causes the collector voltage to go in the negative direction because of increased current in the collector circuit. The negative voltage swing at the collector is greater in amplitude than the positive voltage swing at the base, and this negative swing causes a current to flow through C1 and through the driver coil, giving further impetus to the motion of the tines. The arrangement of the coils and their connections is such that the amplified pickup coil voltage is always of the



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Figure 71. 1,500-cycle oscillator (modulator), simplified schematic.

right polarity to reinforce the motion of the tuning fork and cause it to continue vibrating. The output of the oscillator is taken from the collector and can be checked at TP1.

e. As shown in figure 71, diode CR1 is connected across a part of the resistor network from collector to base of the transistor. This diode is normally nonconducting because of the -12-volt back bias. When, during a cycle of oscillation, the collector voltage reaches -12 volts, the diode conducts, shorting out R1, and partially limiting the negative part of the wave at that point. This limiting action aids the maintenance of the tuning fork vibration by reducing the damping effect at the maximum excursion of the tines. The oscillator feedback is controlled by resistor R3. It is adjusted so that the waveform, as seen on an oscilloscope which may be connected at TP1 and ground, shows about 25 percent distortion. If this control is not sufficiently advanced, oscillations will not be maintained.

f. Emitter and collector bias voltages are obtained from the voltage divider consisting of resistors R6, R7, and R8. Capacitors C3, C4, and C5 filter the 1,500-cycle voltage across each of the resistors. Resistor R4 limits the emitter current, preventing damage to the transistor from excessive current. Capacitor C2 bypasses the 1,500-cycle current around R4. Resistor R5 provides additional current limiting and some negative feedback.

127. The 1,500-Cycle Tuned Amplifier Q1 and Q2

(fig. 72)

a. The 1,500-cycle amplifier isolates the oscillator from the modulator and also improves the waveform of the signal fed to the 1,500-cycle modulator.

b. Transistors Q1 and Q2 are junction-type and are connected as a low gain, tuned amplifier. The simplified circuit of the amplifier is shown in figure 72. The 1,500-cycle output of the oscillator is applied to the base of Q1, where it appears at approximately the same amplitude but a low impedance at the emitter. The base of Q2 is directly connected to the emitter of Q1, and the junction has a common coupling, part of network Z2, which is resonant at 1,500 cycles. Being resonant, it offers a high impedance to 1,500-cycle current, and also smoothes out irregularities in the oscillator output waveform. Transistor Q2 again lowers the impedance of the signal in the manner of a cathode follower. The output at the emitter causes 1,500-cycle current to flow through the primary of T1. Resistor R9 is connected back to -6.2 volts and provides bias voltage for the base of Q1. The -6.2 volts at Z2 is derived from the voltage divider, R11 and R10. Capacitor C7 bypasses the -6.2 volts to ground. An output from the emitter of Q1 is fed to the pulse shaper in the transmitter group to provide timing functions for transmitter operation.

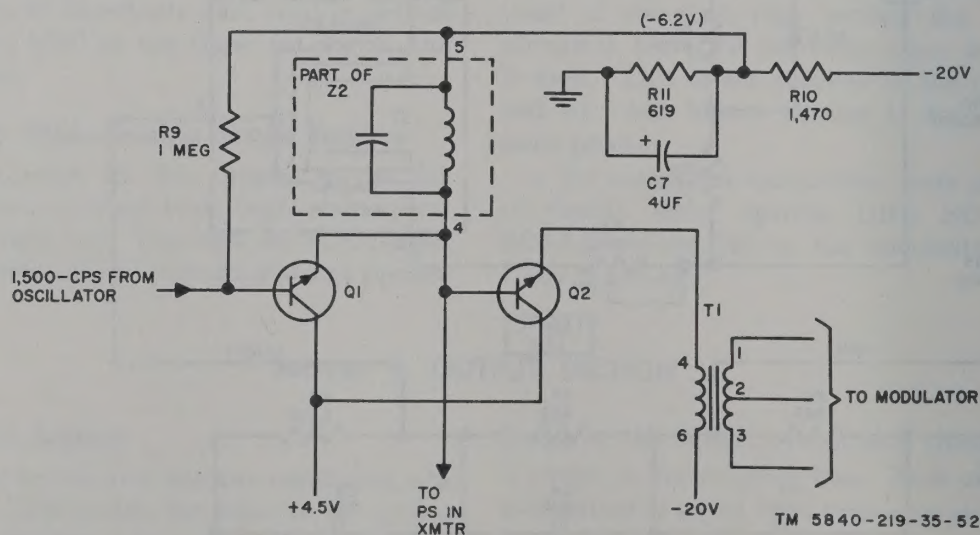


Figure 72. 1,500-cycle tuned amplifier (modulator), simplified schematic.

128. The 1,500-Cycle Modulator

(fig. 73)

a. The 1,500-cycle modulator is a keying circuit which allows two cycles of 1,500-cycle signal to pass through the output hybrid coil to the outgoing lines for each ONE of the transmitted message.

b. The secondary of transformer T1 is push-pull, and is connected to terminals 7 and 10 of the hybrid output coil through two diodes, CR6 and CR7, as shown in figure 73. The secondary winding center tap of T1 is connected to the voltage divider, R13 and R14, which has a potential at this point of about -3 volts. The primary windings of T2 are connected together at terminals 8 and 9, which are also connected to the modulator transistor, Q6. During the OFF condition of Q6, the potential at its emitter is more negative than -12 volts. This negative voltage back-biases diodes CR6 and CR7, preventing transmission of the 1,500-cycle signal from T1 to T2.

c. The output of the shift register, consisting of positive-going pulses, one for each ONE of the transmitted message, is applied through network Z2 to the base of Q6. Network Z2 shapes the pulses to reduce the generation of harmonics during keying and prevents the transmission of 1,500 cycles to the shift register. The application

of this positive pulse causes the emitter impedance to be reduced, and the potential at the emitter to be dropped to about -2.5 volts. This is less negative than the potential of -3 volts at the voltage divider at T1, thus causing the diodes to conduct and transmit two cycles of 1,500-cycle signal for each pulse from the shift register.

129. The 600-Cycle Oscillator Q9

(fig. 74)

a. The 600-cycle oscillator provides a 600-cycle ready signal to the receiver at the beginning of each frame to prepare the receiver for the receipt of the sync pulse. The oscillator output goes through two amplifiers to the modulator, where it is keyed by ready tone control signals applied to transistor Q5.

b. The circuit of figure 74 is readily understood if it is compared with an analogous electron tube Colpitts oscillator. In this analogy the emitter of the transistor corresponds to the cathode of the electron tube, the base to the grid, and the collector to the plate. The tuned tank circuit, consisting of the inductance of transformer T3 and the capacitance of C9 and C11, is connected from base to collector (grid to plate) and the emitter (cathode) is connected to the junction of C9 and C11. Oscillation takes place in the conventional manner of a Colpitts oscillator: the voltage induced in the tuned circuit by the ap-

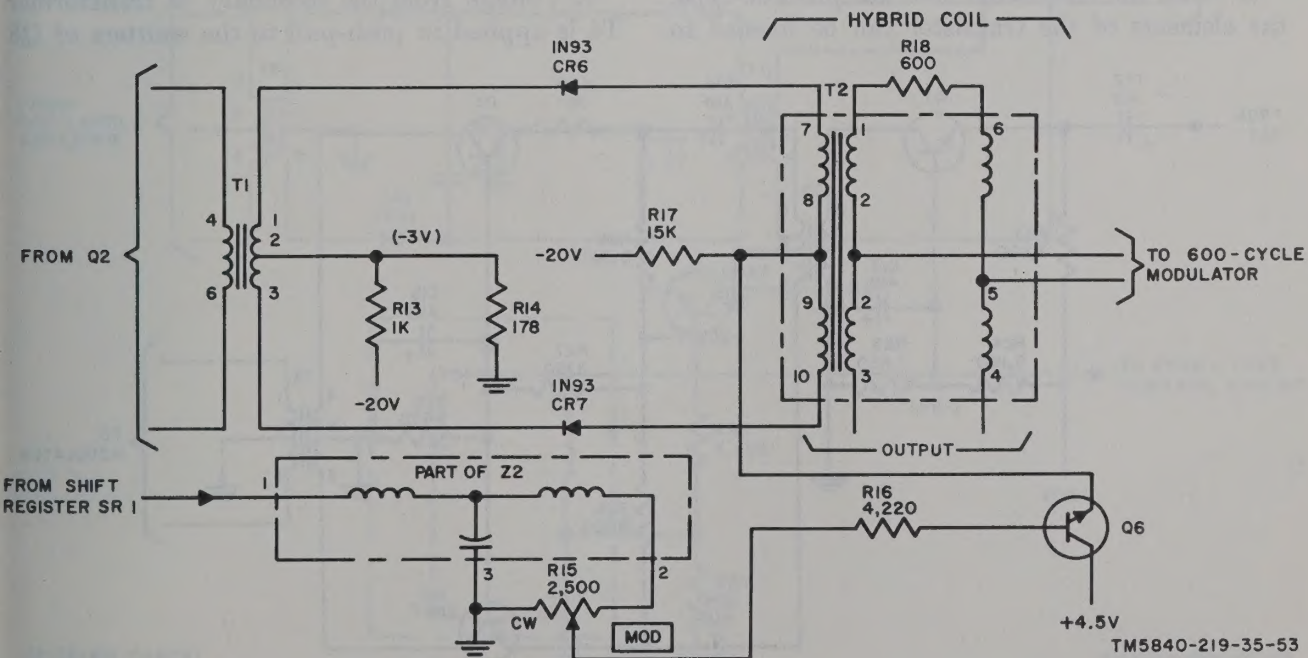


Figure 73. 1,500-cycle modulator, simplified schematic.

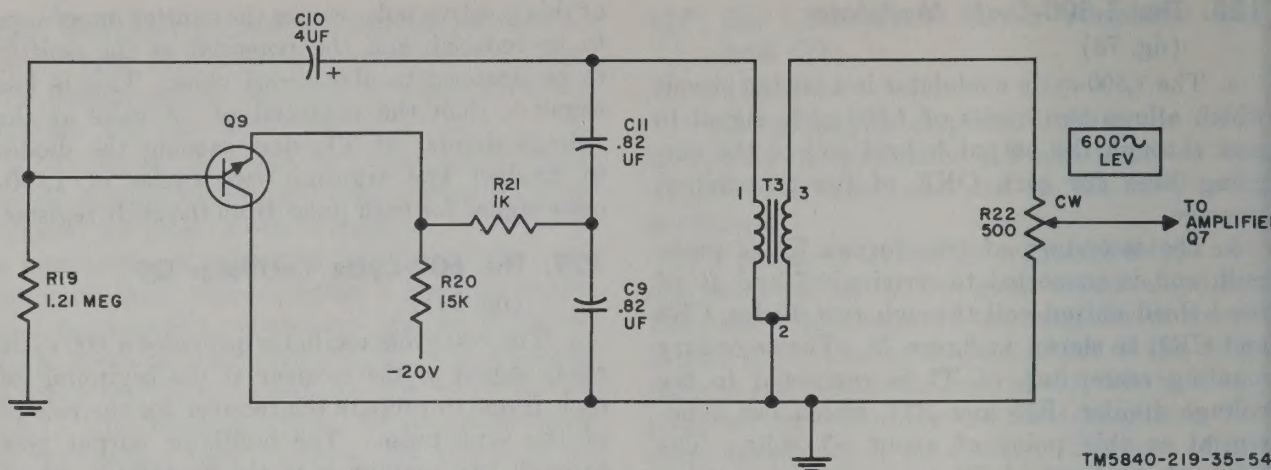


Figure 74. 600-cycle oscillator, simplified schematic.

plication of power to the transistor is applied to the base and is amplified at the collector and then is applied to the tuned circuit in the correct phase to sustain oscillations in the circuit.

130. The 600-Cycle Amplifier (fig. 75)

a. The output of the 600-cycle oscillator is amplified by the 600-cycle amplifier consisting of two transistor stages, the first a single ended driver stage and the second a push-pull stage. The output at transformer T5 is applied to the modulator.

b. Since the transistors used are junction-type, the elements of the transistor can be likened to

those of conventional triode tubes. In this stage the emitters correspond to the cathodes of tubes, the collectors to plates, and the base to grids. The circuit is comparable to a grounded grid amplifier. The 600-cycle output of the oscillator applied to the emitter of Q7 is amplified at the collector and applied to the primary of T4. C13 isolates the -12 volts from ground, but passes the signal to the emitter. Bias for the emitter is supplied from the -20-volt source through R23. Bias for the base is derived from the voltage divider R24 and R25 connected to -20 volts and ground. The base bias is about -8 volts.

c. Voltage from the secondary of transformer T4 is applied in push-pull to the emitters of Q3

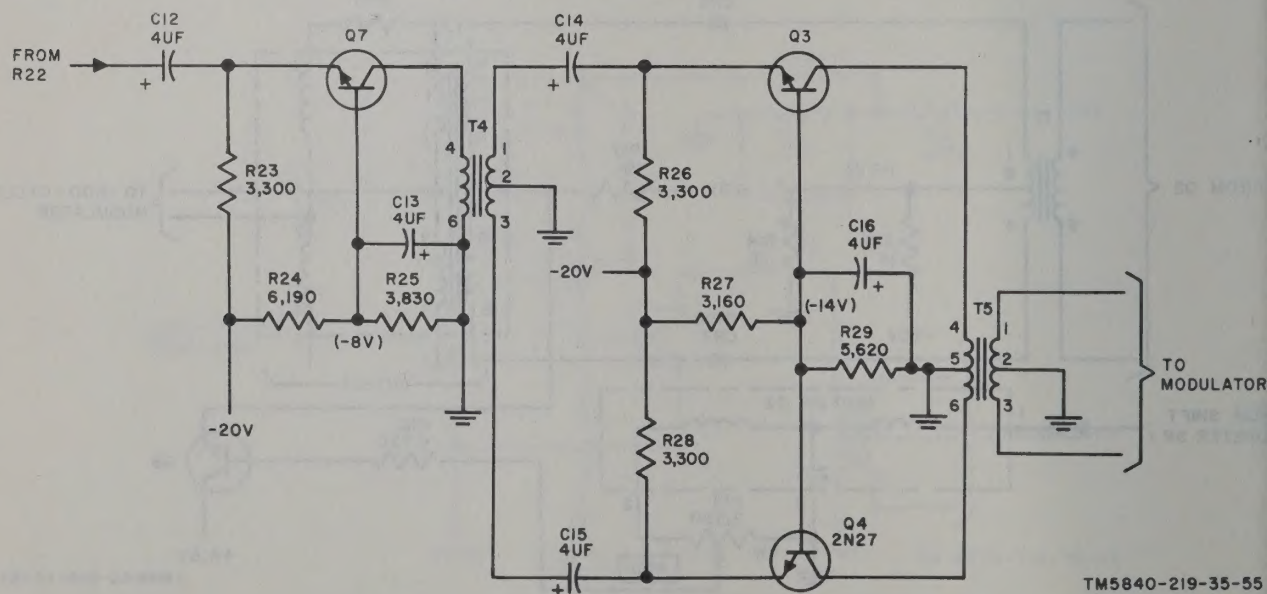


Figure 75. 600-cycle amplifier, simplified schematic.

and Q4 through capacitors C14 and C15. The function of each half of this push-pull amplifier is identical to the function of the preceding stage. The push-pull output is applied to transformer T5, where it is sent to the modulator.

d. Capacitors C14 and C15 isolate the -20 volts from ground. Resistors R27 and R29 form a voltage divider which applies about -14 volts bias to the two base connections. Resistors R26 and R28 return the emitters to -20 volts.

131. The 600-Cycle Modulator

(fig. 76)

a. The 600-cycle modulator is a keying circuit keyed by the signal from the ready-tone control

circuit, which allows a 600-cycle signal to pass through the hybrid output coil to the outgoing line. It functions in the same way as the 1,500-cycle modulator.

b. The center tap of the secondary winding of transformer T5 is connected to ground. The center tap of the primary of T6 is connected to the emitter of Q5. During the OFF conditions of Q5 the potential at the emitter is about -12 volts. Diodes CR8 and CR9 are back-biased by this voltage, are nonconducting, and do not transmit the 600-cycle signal to T6. Upon the application of a positive voltage on the base of Q5, the emitter voltage goes from -12 volts to slightly positive, causing the diodes CR8 and CR9 to con-

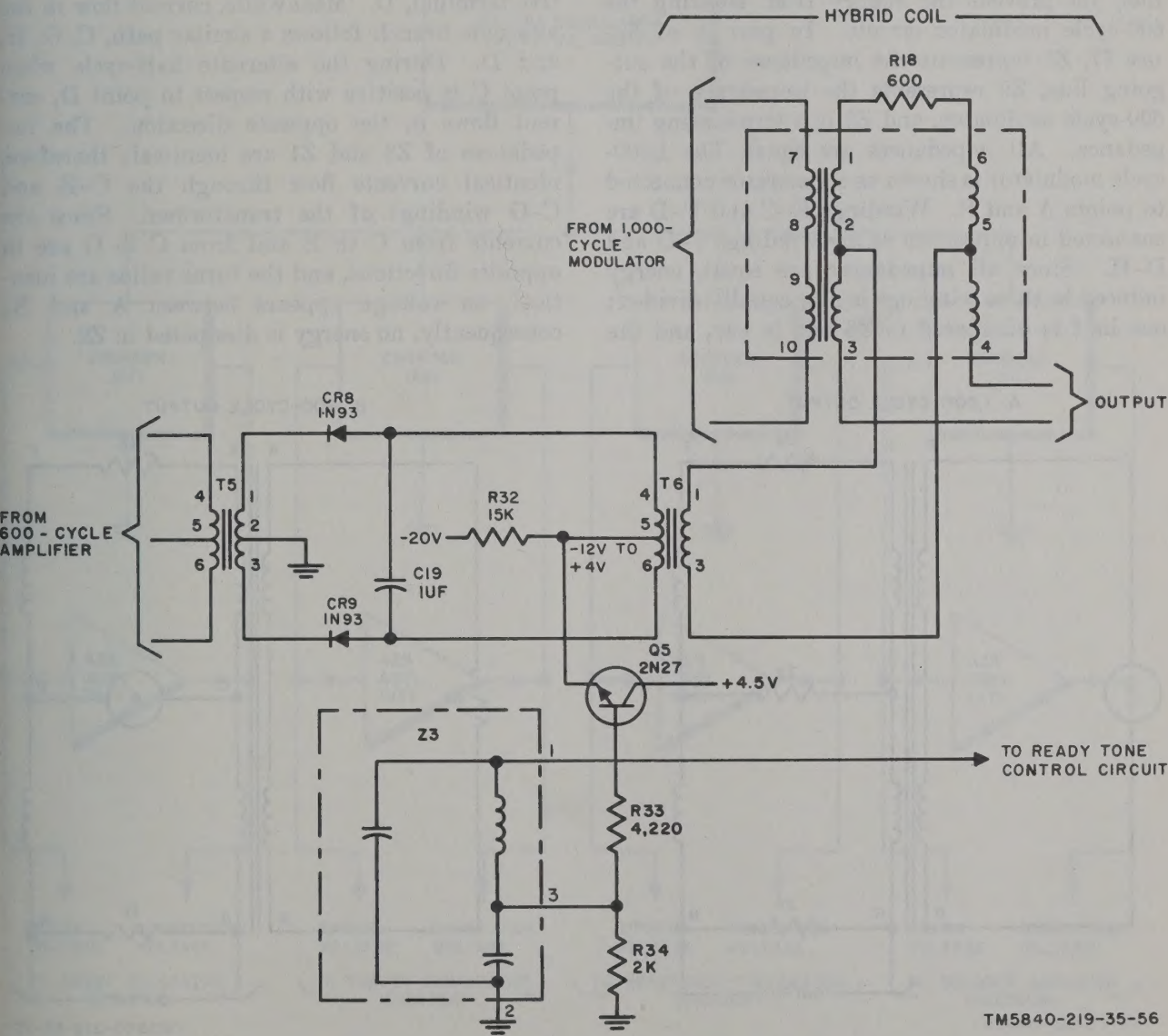


Figure 76. 600-cycle modulator, simplified schematic.

duct. Capacitor C19 is connected across the primary of T6, filtering out any 1,500-cycle component that might be generated in the modulator. Network Z3, in addition to shaping the pulse voltage from the ready tone control, also prevents transmission of 600-cycle energy back into the ready tone control circuit.

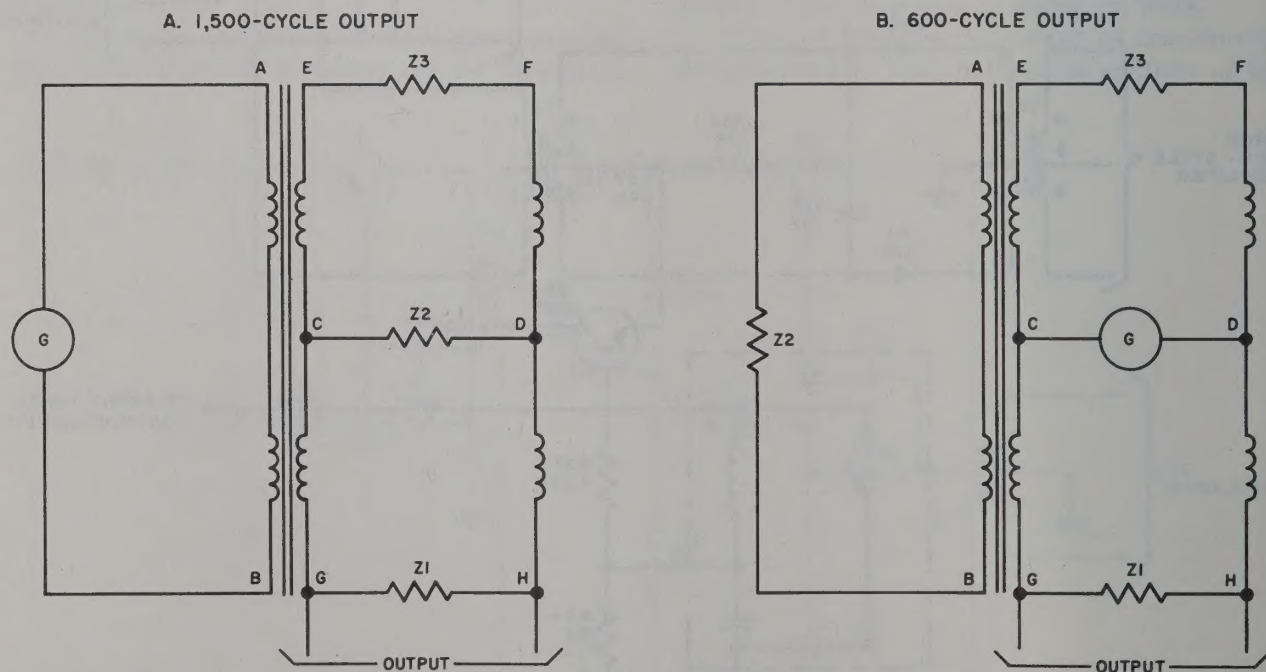
132. Hybrid Coil

(fig. 77)

a. The purpose of the hybrid coil is to connect the outputs of the 1,500-cycle modulator and the 600-cycle modulator to the outgoing line, while isolating the two modulators from each other. First consider the case where it is desired to transmit the 1,500-cycle modulator output to the line, yet prevent the energy from entering the 600-cycle modulator circuit. In part A of figure 77, Z1 represents the impedance of the outgoing line, Z2 represents the impedance of the 600-cycle modulator, and Z3 is a terminating impedance. All impedances are equal. The 1,500-cycle modulator is shown as a generator connected to points A and B. Windings E-C and F-D are connected in opposition as are windings C-G and D-H. Since all impedances are equal, energy induced in these windings is also equally divided; one half is dissipated in Z3 and is lost, and the

other half in Z1, the outgoing line. When all the elements are balanced, no voltage difference exists between C and D; consequently, no energy is dissipated in Z2.

b. In B of figure 77 Z1 represents the outgoing line, Z2 represents the impedance of the 1,500-cycle modulator, and Z3 is the terminating impedance. The 600-cycle modulator is shown as a generator connected to points C and D. With this arrangement the energy from the 600-cycle modulator is divided, one half being dissipated in Z1, and the outgoing line, and the other half being dissipated in Z3. Assume that point C is negative with respect to point D; current will flow from C and E, through impedance Z3, to point F, through F-D windings and to the positive terminal, D. Meanwhile, current flow in the alternate branch follows a similar path, C, G, H, and D. During the alternate half-cycle when point C is positive with respect to point D, current flows in the opposite direction. The impedances of Z3 and Z1 are identical; therefore, identical currents flow through the C-E and C-G windings of the transformer. Since the currents from C to E and from C to G are in opposite directions, and the turns ratios are identical, no voltage appears between A and B; consequently, no energy is dissipated in Z2.



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Figure 77. Hybrid coil, schematic.

Section VI. AUTOMATIC ZERO SET

133. Automatic Zero Set

(fig. 78)

a. As described in paragraph 115g the automatic zero set (AZS) provides a zero set voltage to the sweep amplifier in the encoder to correct for inherent drift within the sweep amplifier. The automatic zero set also generates zero set

voltages to zero set the two comparator amplifiers in the encoder and a similar amplifier in the decoder.

b. The function of the AZS circuitry is to provide a zero set voltage in the sweep amplifier input difference stage to insure that the output of the sweep amplifier is proportional to the sum

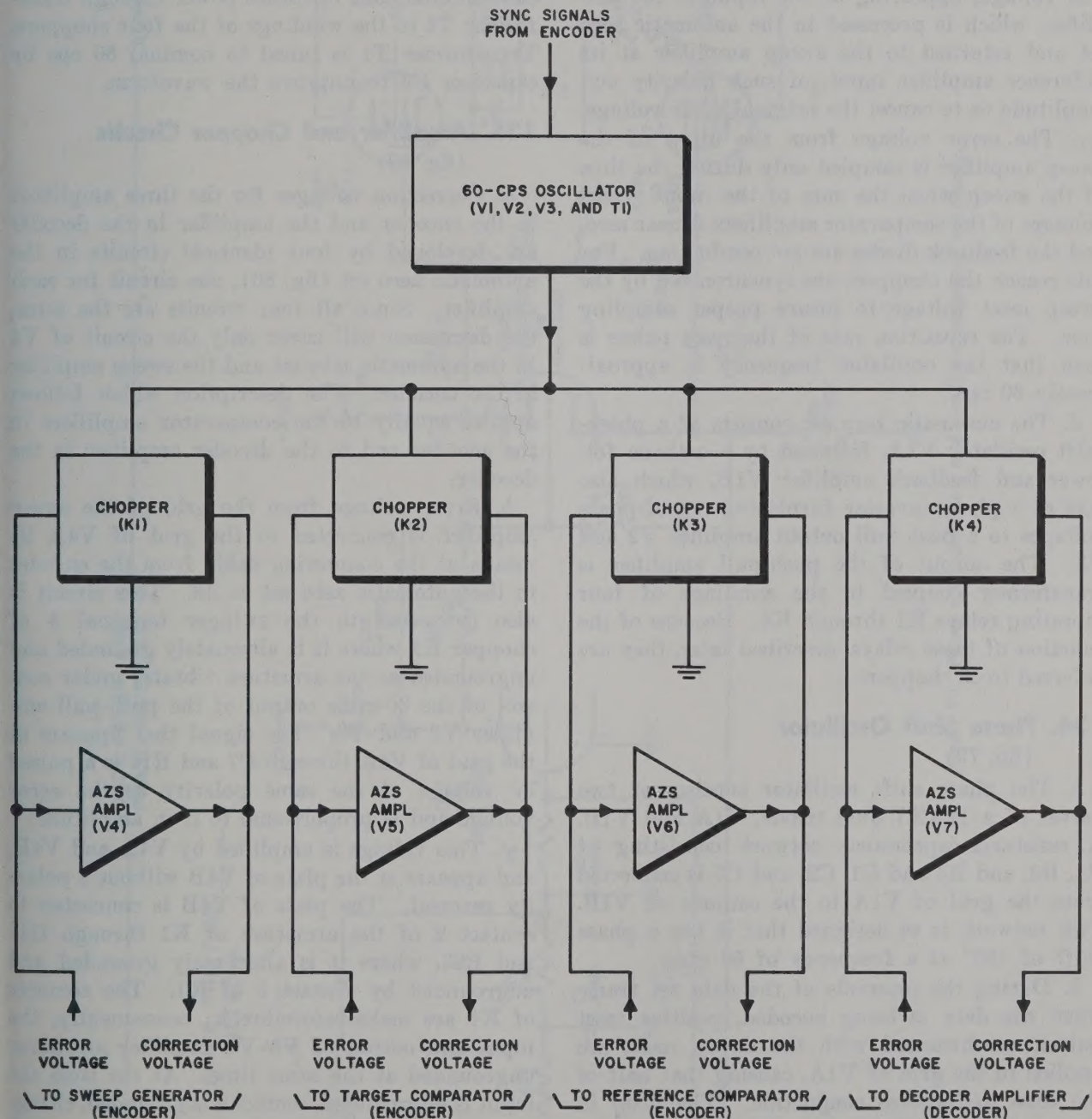


Figure 78. Automatic zero set, block diagram.

of its input signal voltages. During a condition of the operation of the sweep amplifier when the sum of its input signal voltages is zero, the output voltage must be zero. If the output voltage is not zero, the cause is an unbalance within the amplifier. Since the amount of feedback around the sweep amplifier is large, any undesired output voltage also appears at the input connections but with its polarity reversed because of the odd number of stages used in the amplifier. It is this voltage, appearing at the input to the amplifier, which is processed in the automatic zero set and returned to the sweep amplifier at its difference amplifier input, of such polarity and amplitude as to cancel the original error voltage.

c. The error voltage from the input of the sweep amplifier is sampled only during the time of the sweep when the sum of the input signal voltages of the comparator amplifiers is near zero, and the feedback diodes are not conducting. For this reason the choppers are synchronized by the sweep reset voltage to insure proper sampling time. The repetition rate of the reset pulses is such that the oscillator frequency is approximately 60 cps.

d. The automatic zero set consists of a phase-shift oscillator V1A, followed by a cathode follower and feedback amplifier V1B, which also acts as a phase inverter furnishing out-of-phase voltages to a push-pull output amplifier V2 and V3. The output of the push-pull amplifier is transformer coupled to the windings of four vibrating relays K1 through K4. Because of the function of these relays, described later, they are referred to as choppers.

134. Phase Shift Oscillator

(fig. 79)

a. The phase shift oscillator consists of two halves of a 12AX7 dual triode, V1A and V1B. A resistance-capacitance network consisting of R1, R2, and R3 and C1, C2, and C3 is connected from the grid of V1A to the cathode of V1B. This network is so designed that it has a phase shift of 180° at a frequency of 60 cps.

b. During the intervals of the data set frame when the data is being encoded, positive reset pulses, synchronized with the sweep reset, are applied to the grid of V1A, causing that half of the tube to increase conduction. The drop in plate voltage at V1A is coupled to the grid of V1B through R5 and C35. The resulting reduc-

tion in cathode current of V1B causes a negative-going voltage to be fed back to the input to the phase-shifting network. This voltage having been inverted by V1A is now 180° out of phase with the reset pulses and is further shifted 180° by the network so that it arrives back at the grid of V1A in time to reinforce the next pulse, or to maintain oscillation in the circuit in the absence of a reset pulse.

c. The push-pull output stage V2 and V3 is conventional, and furnishes power through transformer T1 to the windings of the four choppers. Transformer T1 is tuned to nominal 60 cps by capacitor C6 to improve the waveform.

135. Amplifier and Chopper Circuits

(fig. 80)

a. Correction voltages for the three amplifiers in the encoder and the amplifier in the decoder are developed by four identical circuits in the automatic zero set (fig. 80), one circuit for each amplifier. Since all four circuits are the same, the discussion will cover only the circuit of V4 in the automatic zero set and the sweep amplifier in the encoder. The description which follows applies equally to the comparator amplifiers in the encoder and to the decoder amplifier in the decoder.

b. Error voltage from the grid of the sweep amplifier is connected to the grid of V4A by means of the connecting cable from the encoder to the automatic zero set at J2. This circuit is also connected to the swinger terminal 4 of chopper K1 where it is alternately grounded and ungrounded as the armature vibrates under control of the 60-cycle output of the push-pull amplifier V2 and V3. The signal that appears at the grid of V4A through C7 and R14 is a pulsed dc voltage of the same polarity as the error voltage and is proportional to it in amplitude.

c. This voltage is amplified by V4A and V4B, and appears at the plate of V4B without a polarity reversal. The plate of V4B is connected to contact 2 of the armature of K1 through C11 and R23, where it is alternately grounded and ungrounded by contact 3 of K1. The contacts of K1 are make-before-break; consequently, the input and output of V3-V4 amplifier are never ungrounded at the same time. At the time the input is ungrounded, contact 2 is grounded, charging capacitor C11 to the voltage to which it had been driven by the amplified input signal. A

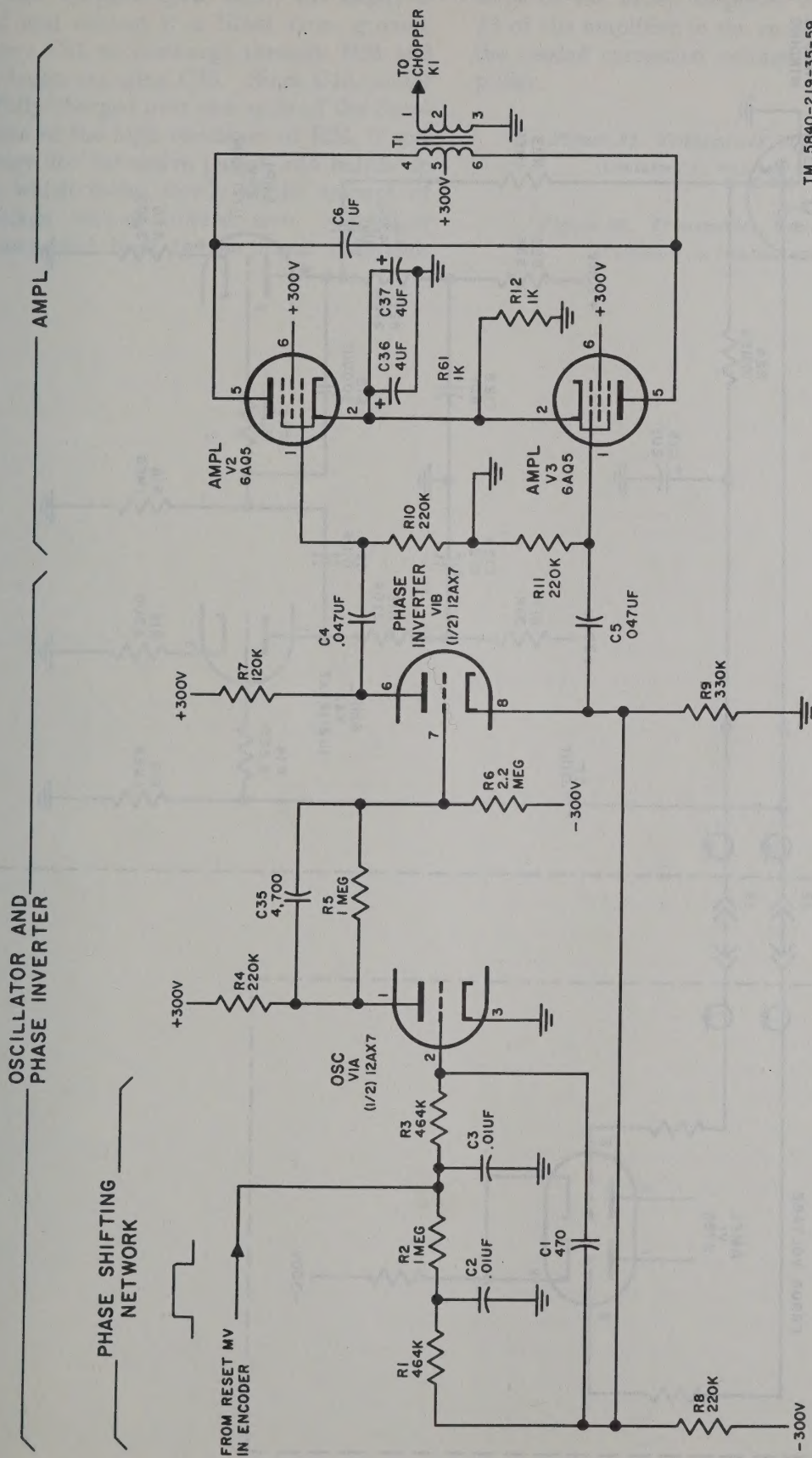


Figure 79. Phase shift oscillator and amplifier, simplified schematic.

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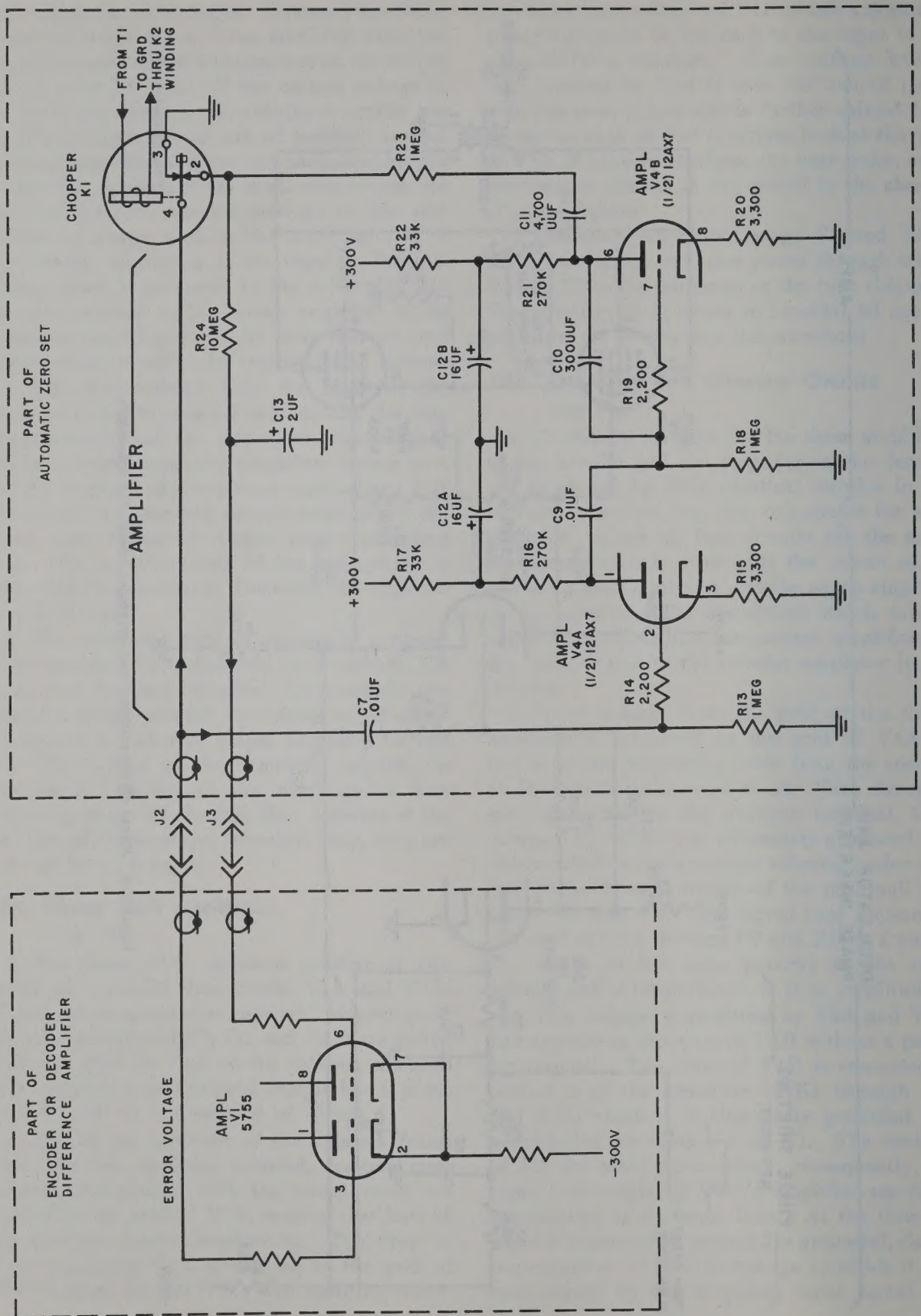


Figure 80. Amplifier and chopper circuit, simplified schematic.

part of the chopper cycle later, the input is grounded and contact 2 is lifted from ground. This allows C11 to discharge through R23 and R24 and begin charging C13. Since C13 cannot become fully charged over one cycle of the chopper because of the high resistance of R24, it acts as a storage for successive pulses, and builds up a charge which varies slowly as the amount of error voltage reduces toward zero. Capacitor C13 is connected back to the input difference

stage of the sweep amplifier by the cable from J3 of the amplifier to the encoder, and furnishes the needed correction voltage to the sweep amplifier.

Figure 81. Transmitter, block diagram.

(Contained in separate envelope)

Figure 82. Transmitter, timing diagram.

(Contained in separate envelope)

CHAPTER 8

THEORY—RECEIVER

Section 1. INPUT SECTION

136. Block Diagram

(fig. 83)

a. The signals received on the line from the transmitter start with a ready signal of 600 cps lasting for three time slots and a signal of 1,500 cps lasting for six time slots, both signals arriving approximately simultaneously. Following the six time slot signal is a no-signal interval of one time slot, followed by a sync signal of 1,500 cps lasting for one time slot. The 1,500-cps auxiliary and data signals follow immediately after the sync signal. These signals are illustrated on the timing chart (fig. 88).

b. The path of the input signal through the amplifying section is selected in accordance with the desired mode of operation, CDG/TAC or OC (par. 37).

- (1) When using the CDG/TAC mode, the signal is switched through part of CDG/TAC-OC switch S1 and the pad and filter to amplifier V1 where it is amplified, and where its level is automatically controlled by the AGC circuits. It then passes through another set of contacts of S1 to amplifier V2A where it is further amplified. The output of V2A is passed through the separation filter, where the 600-cps and 1,500-cps components of the signal are processed separately. Each goes through a detector and a slicer circuit, where it is converted to positive-going pulses. The duration of the pulses is about the same as the duration of the groups of ac pulses received on the line. A portion of the output of the data detector is applied to AGC amplifier V2B. The output of V2B is rectified and filtered and is used to control the gain of V1.

- (2) When using the OC mode, the signal is switched directly into the input of V2A, where it follows the same path as during the CDG/TAC mode. During the OC mode, no AGC is applied to the signal.

c. At the start of the frame, the output of the ready slicer (+) is applied to the gate of F/F No. 1, passing a 6,000-pps pulse and turning F/F No. 1 ON (appendix III). At the same time, the output of the data slicer (+) is applied to CG2. The positive output bias from F/F No. 1 turns ON delay F/F after a time delay of .8 milliseconds. The leading edge of the positive output of the delay F/F is differentiated, and the resulting pulse turns ON F/F No. 6. The positive output of F/F No. 6 is applied to CG1, but CG1 gate will not open unless the input to it from F/F No. 3 is negative. F/F No. 3, however, is ON because CG2 was opened when the data signal was applied at the start of the frame, and the first pulse of the 6,000 pps passed through it to turn F/F No. 3 ON. The positive output of F/F No. 3 opens the count gate CG6 and allows the 6,000-pps pulses to pass through it to the pulse frequency divider. The pulse frequency divider selects every eighth pulse of the 6,000 pps, which is used as a sampling pulse in the programmer section.

d. At the end of the ready signal, the negative bias from the ready slicer and the positive bias from delay F/F open the input gate at F/O No. 1, allowing a 6,000-pps pulse to trigger the F/O. The pulse from the F/O turns F/F No. 1 OFF, and the negative output of F/F No. 1 opens the gate of F/O No. 4 to pass a pulse which triggers F/O No. 4. The output pulse from F/O No. 4 turns OFF delay F/F.

e. With F/F No. 6 ON (*c* above) and the positive data signal present, both biases open

Figure 83. Receiver input section, detailed block diagram.

(Contained in separate envelope)

CG3, which passes a clock pulse (clock pulses are being generated in the programmer section while the pulse frequency divider is generating sampling pulses) to turn ON ready control F/F No. 2. F/F No. 2 then sends a positive ready signal to the programmer section, and also applies positive bias to CG5. At the end of the data signal, the negative data bias and the positive output from F/F No. 2 open CG5 which allows a 6,000-pps pulse to pass through it to trigger F/O No. 3, turning OFF sync control F/F No. 3. The negative output from F/F No. 3 and the positive output from F/F No. 6 open the gate of CG1 passing a 6,000-pps pulse to the frequency divider stages, resetting them to OFF. The same pulse is passed back to F/O No. 6, triggering it and thus turning OFF F/F No. 6. The negative output of F/F No. 6 opens the gate of CG4, allowing a pulse to pass through the trigger F/O No. 2, thus turning OFF F/F No. 2 and terminating the ready signal to the programmer section.

f. The sync pulse, a single time slot data signal which follows next, opens gate CG2 passing a pulse to turn ON F/F No. 3 again. F/F No. 3 remains ON for the duration of the frame and opens the count gate CG6, passing 6,000-pps pulses to the pulse frequency divider where sampling pulses are generated throughout the frame.

g. The TPC switch in the test position disables the pulse frequency divider reset function and maintains a continuous flow of 6,000-pps pulses to generate sampling pulses.

h. The data pulses coming from the data slicer are not sharply defined, being envelopes of the rectified ac signals. The pulses must be reformed into rectangular pulses, and also must be retimed to the clock pulses being generated in the programmer section. These are done by the data sampling control F/F No. 5 and F/O No. 5. A positive data pulse opens the gate within F/F No. 5, allowing a clock pulse to turn it ON. At the end of the data pulse (—) the gate within F/O No. 5 is opened, allowing a clock pulse to trigger the F/O and turn OFF F/F No. 5. The output of F/F No. 5 is a squared version of the incoming data pulse, and is timed by the receiver clock pulses. Since the sampling pulses which trigger the clock pulses occur at the fourth pulse

and every eighth pulse thereafter of the 6,000-pps pulses, the clock pulses and the regenerated data pulses occur one-half time slot later than those of the transmitter.

i. The 6,000-pps generator consists of a 1,500-cps oscillator Q1; amplifier and shaper stages Q2, Q3, Q5, and Q6; a frequency multiplier V3A, which selects the fourth harmonic of the oscillator frequency; and a pulse generator Q4 and V3B, which converts the 6,000-cps signal to short, negative-going pulses.

137. Amplifier AGC Circuits

(fig. 84)

a. *CDG/TAC Operation.* Either of two modes of operation, CDG/TAC or OC, can be selected by S1. In the CDG/TAC mode, the input signal passes through a 600-ohm 20-db terminating pad, filter Z4, and transformer T1 to grid 1 of V1 through current limiting resistor R1. Filter Z4 is a band pass filter which discriminates against electrical noise outside the pass band of 500 to 2,000 cycles. Bias for grid 1 is taken from voltage divider R31–R32 and the –300-volt supply. R3 is the plate load resistor and R2 is the screen resistor bypassed by C1. The output from plate 5 is coupled to grid 2 of V2A by C2 and R4 through S1. Bias voltage for V2A is provided by the IR drop across R5 filtered by C3. R35 limits the low frequency response of the amplifier stage to add stability. The output from pin 1 of V2A is passed to the separation filter (fig. 85). The input of AGC amplifier V2B is the rectified positive 1,500-cycle data signal. The output of V2B is passed through C5 and appears across R7. The positive portion of the signal is clamped to ground by CR13, and the negative portion is passed through CR1 where it charges capacitor C4. This voltage across C4 and R6 is proportional to the signal applied to grid 1 of V2B, and is used to control the voltage at pin 7 of V1, thus controlling the gain of V1.

b. *OC Operation.* In the OC mode of operation, switch S1 is at OC. The input signal level is AGC-controlled by associated equipment to about –4 dbm. This signal appears at the arm of R40 and is applied to grid 2 of V2A. R40 is adjusted to give the same signal level at the grid of V2A for both OC and CDG/TAC operation. The operation of the circuit of V2A through the separation filter is the same as described for a above.

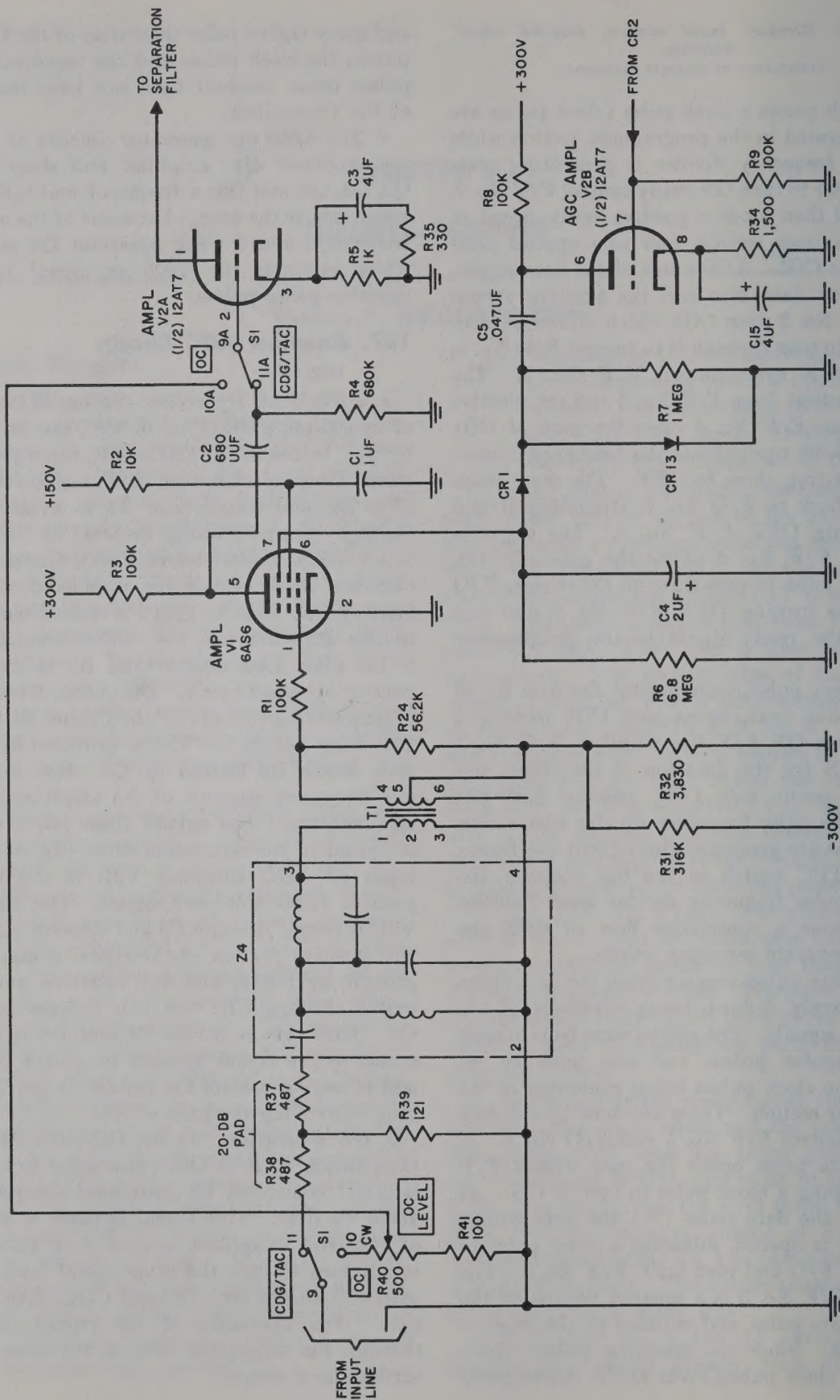


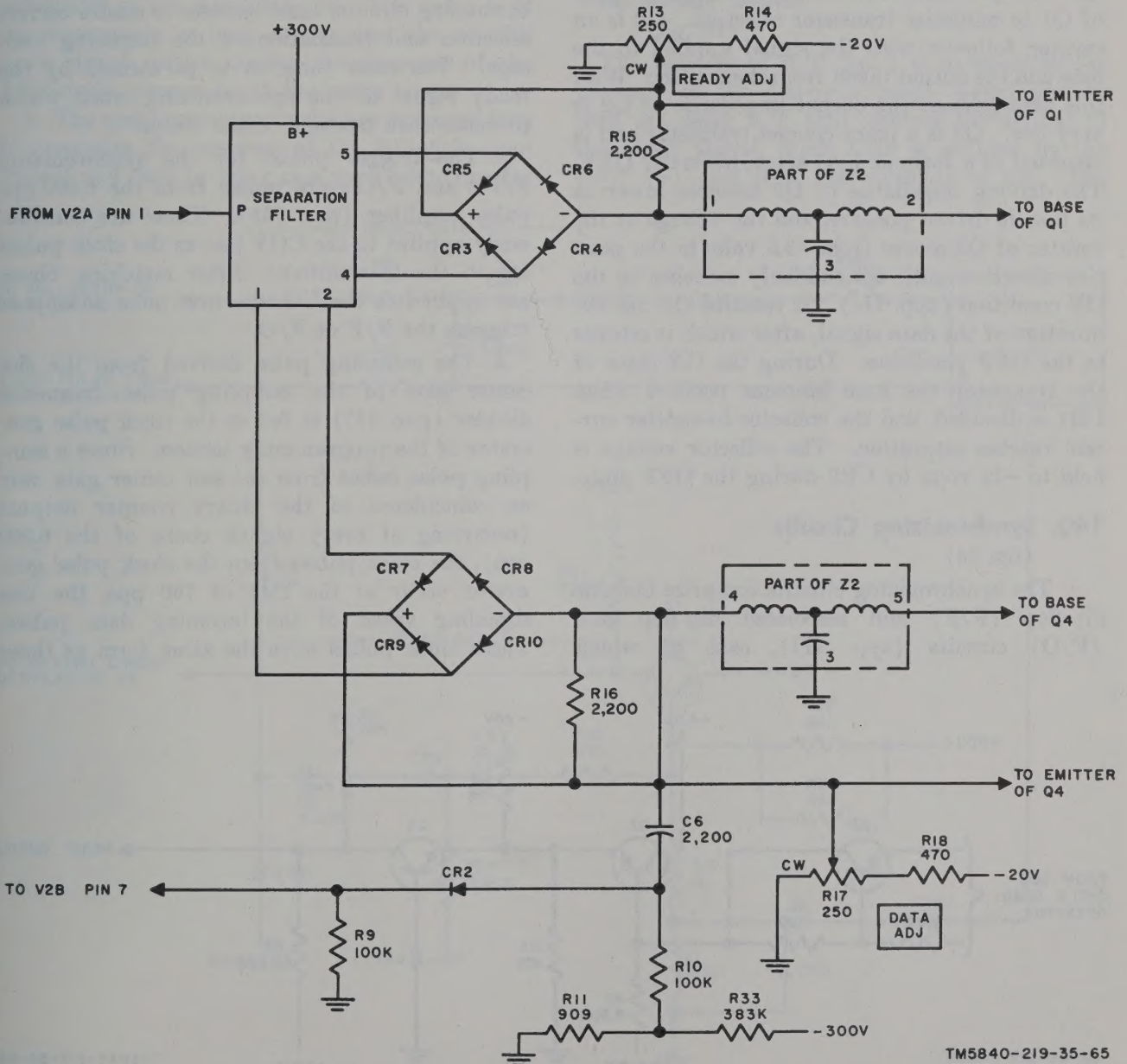
Figure 84. Amplifier circuits, simplified schematic.

138. Separation Filter, Detectors and Filters (fig. 85)

a. These circuits separate the 600- and 1,500-cycle ready and data signals, detect and filter them, and present them as carrier envelopes of ON and OFF pulses.

b. The plate load for V2A (fig. 84) is the separation filter Z1. This filter is a sealed unit. It functions to separate the 600-cycle component of the received signal from the 1,500-cycle component. The 600-cycle output is rectified by full

wave bridge rectifier CR3, 4, 5, and 6, and is filtered by network Z2. The output of filter Z2 is applied to transistor Q1 (fig. 86). Resistance network R14 and potentiometer R13 provide a bias for the emitter of Q1, part of the ready slicer (par. 139). The amount of bias at the arm of R13 determines the length of the rectified and filtered output pulses. The circuits for rectifying, filtering, and adjusting the 1,500-cycle signal component are identical to those for the 600-cycle signal component, except for the circuit designations shown in the figure.



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Figure 85. Amplifier synchronizer, separation filters, detector and filters, simplified schematic.

139. Ready and Data Slicers

(fig. 86)

a. Since the circuits of the ready and data slicers are identical, only the circuits of the ready channel are described.

b. The input signal from the ready detector and filter is applied to the emitter and base of Q1, which acts as a conventional common emitter amplifier (app. III). Negative bias for the emitter comes from the READY ADJ potentiometer (fig 85); positive bias for the collector comes from the +4.5 volts applied to the base of Q2. R2 provides feedback to stabilize the gain of Q1 to minimize transistor selection. Q2 is an emitter follower with the signal applied to the base and the output taken from the emitter. With this arrangement the output impedance of Q2 is very low. Q3 is a point contact transistor and is operated as a form of F/O stage, normally OFF. The driving impedance of Q2 becomes lower as its base is driven positive, and the voltage at the emitter of Q3 moves from -3.5 volts in the positive direction until Q3 suddenly switches to the ON condition (app. III). It remains ON for the duration of the data signal, after which it returns to the OFF condition. During the ON state of the transistor the base becomes positive when CR1 is disabled, and the collector-to-emitter current reaches saturation. The collector voltage is held to -12 volts by CR2 during the OFF state.

140. Synchronizing Circuits

(fig. 83)

a. The synchronizing circuits comprise bistable flip-flop (F/F) and associated flip-flop zero (F/O) circuits (app. III), each of which

is controlled by a combination gate (CG). These combination gates each have two or more enabling bias inputs designated (+), meaning ON, or (-), meaning OFF. These are the basic control elements described in appendix II. In these applications the F/F or F/O is activated when the enabling bias applied to the gates matches the polarities designated on the block diagram (fig. 83); an ON bias matches (+) and an OFF bias matches (-). The CG is enabled only if *all* such inputs match. A mismatch of any one or more of the inputs causes the gates to be disabled.

b. Before the sync signal is accepted, the synchronizing circuits must be reset to assure correct selection and translation of the incoming message. The reset function is performed by the ready signal of the synchronizing word which precedes each message of the frame.

c. The trigger pulses for the synchronizing F/F's and F/O's are pulses from the 6,000-pps pulse amplifier (par. 155). These are continuously applied to the CG's just as the clock pulses are in the transmitter. After matching biases are applied to the CG, the first pulse to appear triggers the F/F or F/O.

d. The sampling pulse derived from the slot center gate of the sampling pulse frequency divider (par. 147) is fed to the clock pulse generator of the programming section. Since a sampling pulse issues from the slot center gate only on coincidence of the binary counter outputs (occurring at every eighth count of the 6,000 pps), the clock pulses from the clock pulse generator occur at the rate of 750 pps, the line signaling speed of the incoming data pulses. These clock pulses have the same form as those

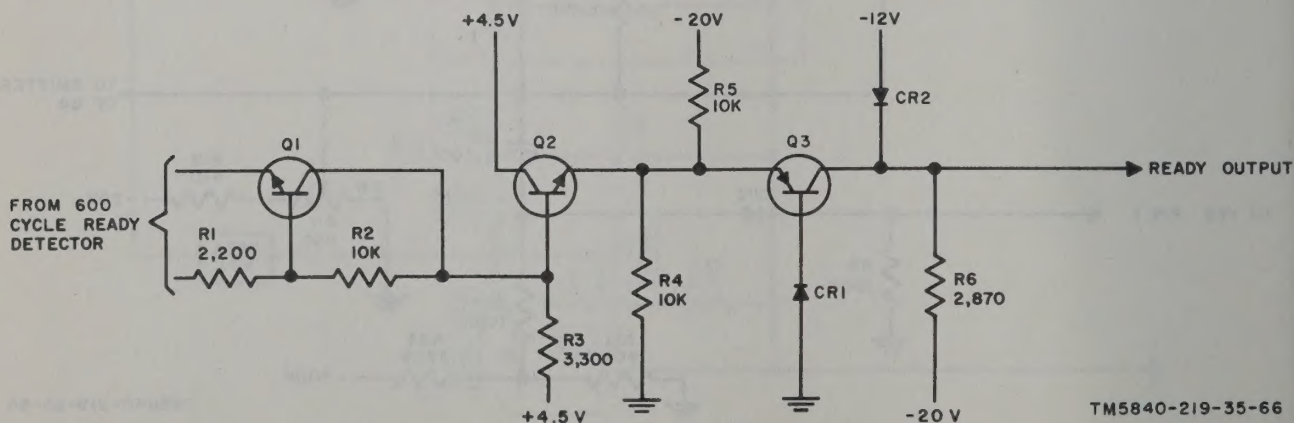


Figure 86. Ready slicer, simplified schematic.

used in the transmitter, and they are used in the data sampling control in the receiver input section and in other sections of the receiver.

141. Ready Signal Recognition

(fig. 83)

a. The distant transmitter sends simultaneously to the line three time slots of 600-cycle signal and six time slots of 1,500-cycle signal. These may appear simultaneously at the receiver as shown in the timing diagram (fig. 88), or the 600-cycle interval may be delayed or advanced from the 1,500-cycle signal, depending on the delay characteristics of the telephone line. The delay is of no consequence as long as one time slot of 600-cycle signal occurs during the presence of the 1,500-cycle component of the ready signal.

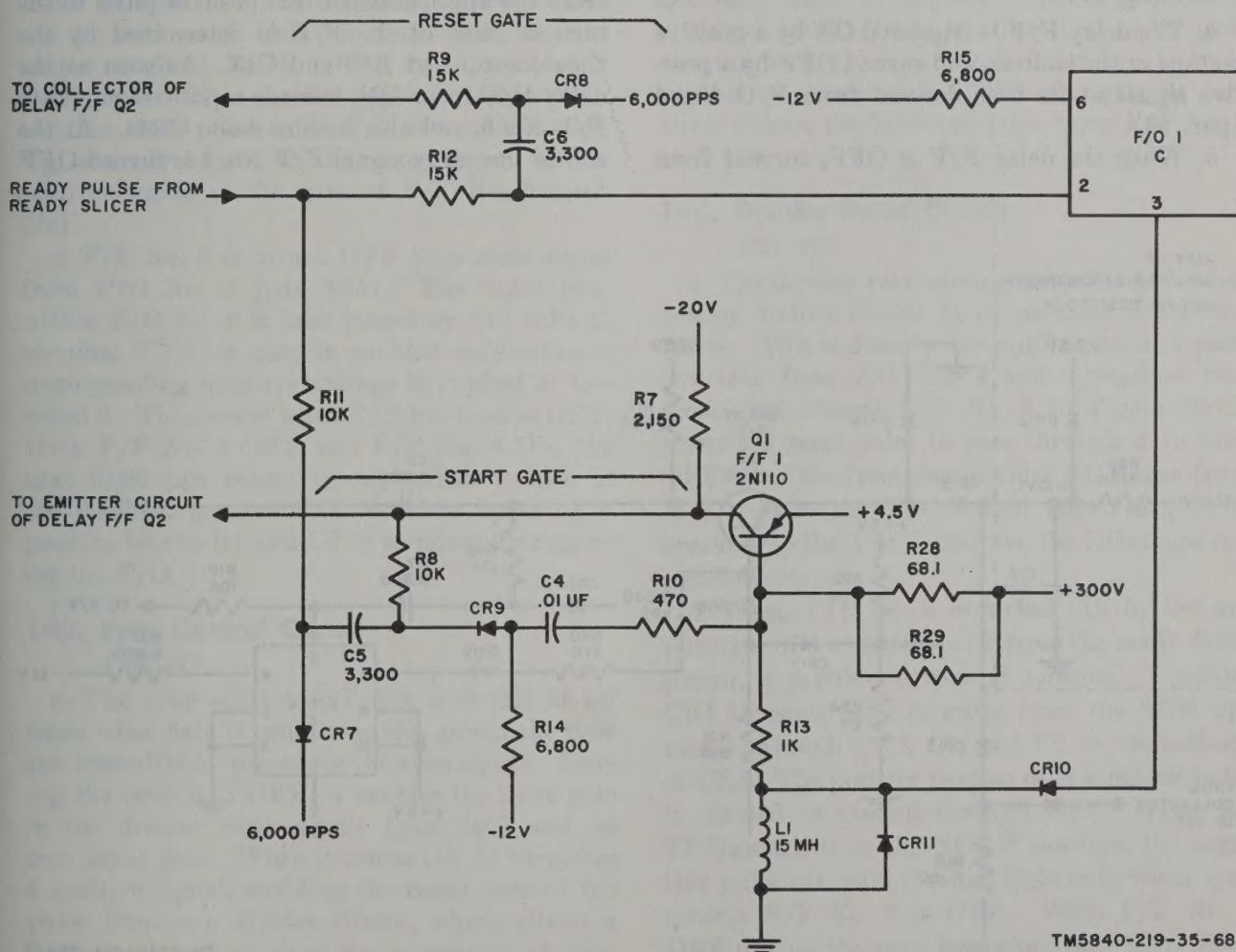
b. The synchronizing circuits are arranged first to recognize the presence of the 600-cycle component and then to check at a particular time for

the presence of the 1,500-cycle component. This allows maximum tolerance in delay differences between the 600-cycle and the 1,500-cycle components such as are introduced by different types of telephone lines. Coincidence of both frequency components of the ready signal activates the ready control to reset the receiver programmer and the sampling pulse frequency divider and thus to prepare the receiver for the sync pulse. Refer to the receiver input timing diagram (fig. 88) and the receiver timing diagram (fig. 132) for the sequence of events.

142. Ready Signal

(fig. 87)

The purpose of F/F No. 1 is to establish the presence of the 600-cycle ready signal and to turn the delay F/F ON. Before the arrival of the ready signal, diode CR9 is enabled by the OFF (-) bias from the collector of Q1. The



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Figure 87. Amplifier synchronizer F/F No. 1 and F/O No. 1, simplified schematic.

arrival of the ready signal applies a positive bias to the anode of CR7, allowing the next 6,000 pps to pass through CR7, C5, CR9, C4, and R10 to the base of Q1, turning the F/F No. 1 ON. The output of F/F No. 1 is about +2 volts and turns ON the delay F/F (par. 143). F/F No. 1 is turned OFF when a positive bias from the delay F/F is applied to the anode of CR8 through R9. CR8 is thus enabled, passing one of the 6,000-pps pulses through C6 to terminal 2 of F/O No. 1. A negative (OFF) bias from the ready slicer output is also necessary because of the -12 volts applied at terminal 2 of F/O No. 1 (par. 96). This pulse triggers F/O No. 1, and F/O No. 1 turns F/F No. 1 OFF.

Figure 88. Receiver input section, timing diagram.
(Contained in separate envelope)

143. Delay F/F Circuit (fig. 89)

a. The delay F/F is triggered ON by a positive voltage at the emitter, and turned OFF by a positive signal at its base derived from F/O No. 4 (par. 96).

b. While the delay F/F is OFF, current from

+300 volts through R30, CR13, and R16 to -12 volts develops a potential of about -10 volts at the junction of CR13 and C13. CR12, being back biased by this voltage, is disabled. CR15 is disabled by reverse bias. The emitter of Q2 is held close to ground potential by CR16. Upon the arrival of the positive-going pulse from F/F No. 1 through CR12, CR13 is disabled, and the voltage at C13 rises in the positive direction through R30 toward +300 volts. Diode CR12, however, is connected directly from C13 to +4.5 volts, preventing C13 from rising more positive than +4.5 volts. The rise in potential at C13 through CR15 to the emitter causes the delay F/F to turn ON (app. III) when the emitter reaches about +1 volt. The base is prevented from rising to more than +.8 volt by CR17 and CR18. CR18 also prevents damage to the transistor from excessively high emitter voltage and current. The time delay (about .8 millisecond) from the application of this positive pulse to the turn on time of the F/F is determined by the time constant of R30 and C13. As soon as the delay F/F turns ON, it sends a positive signal to F/F No. 6, and also enables diode CR14. At the end of the ready signal F/F No. 1 is turned OFF

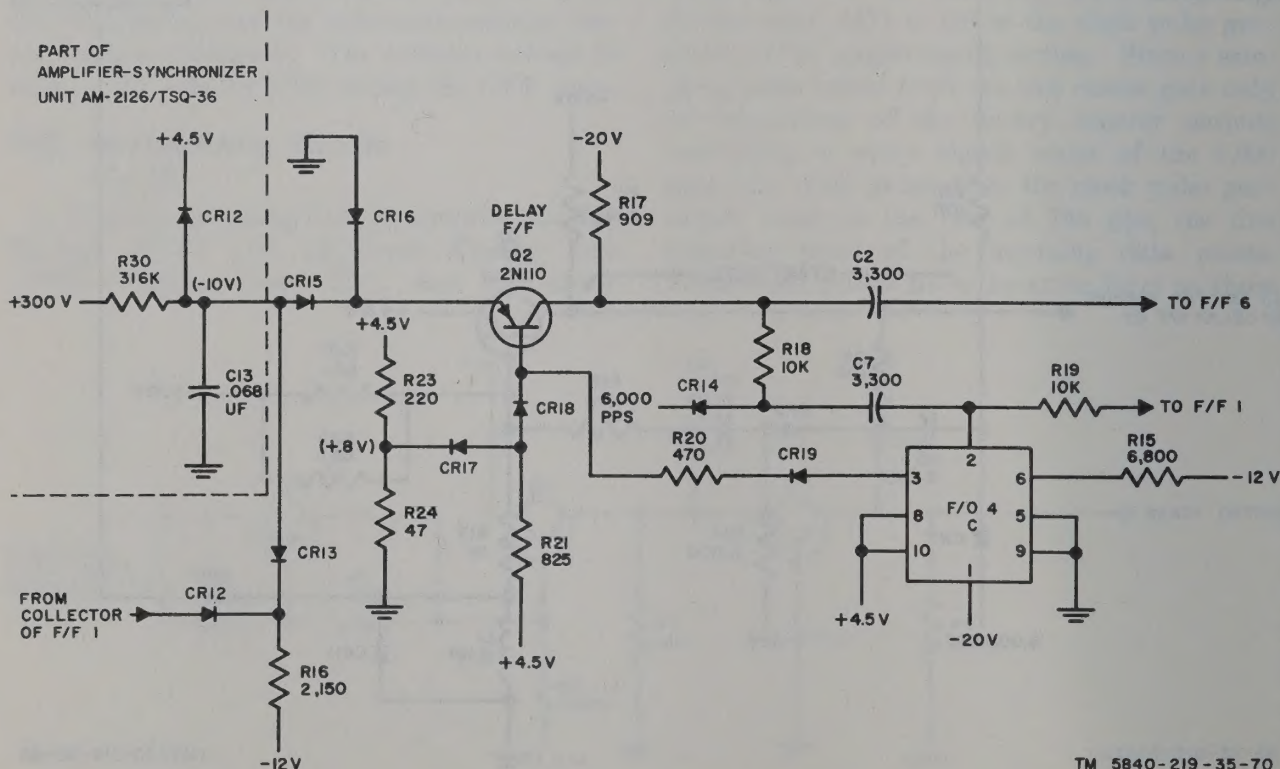


Figure 89. Delay F/F, simplified schematic.

(par. 142). Its negative output enables CR2 within F/O No. 4, allowing the next 6,000-pps pulse to pass through CR14 and C7 to trigger F/O No. 4. When F/O No. 4 fires, it turns OFF the delay F/F by applying a positive pulse through CR19 and R20 to the base of Q2.

144. Ready Control Circuit

(fig. 90)

a. The purpose of this circuit is to send a ready signal to the receiver programmer, described in paragraph 162.

b. When the delay F/F (par. 143) turns ON, the output pulse is differentiated by transformer T2 and diode CR13 and coupled to F/F No. 6 (part of the divider reset circuit (par. 146)). This pulse turns F/F No. 6 ON.

c. F/F No. 2 (par. 94*d*) is triggered ON by a receiver clock pulse through CR7 and C2. However, CR7 is back biased to nonconduction if either of two inputs is negative. These inputs are the data pulse from the data slicer, and the output of F/F No. 6. With both inputs ON (+), diode CR7 is enabled (app. II, A, fig. 211) and the clock pulse turns F/F No. 2 ON, sending a ready signal to the programmer and a positive signal to the gate of F/F No. 3 (par. 94*e*).

d. F/F No. 2 is turned OFF by a reset signal from F/O No. 2 (par. 96*h*). The input gate within F/O No. 2 is back biased by -12 volts at terminal 7. This gate is enabled only when a corresponding negative voltage is applied at terminal 2. This occurs when F/F No. 6 turns OFF. With F/F No. 6 OFF and F/F No. 2 ON, the next 6,000 pps passes through CR8 (which is now enabled because F/F No. 2 is applying a positive bias to it) and C3 to terminal 2, triggering the F/O.

145. Sync Control Circuit

(fig. 91)

a. The sync control F/F No. 3 is ON at all times when data is being received, except the time slot immediately preceding the sync signal. During the time it is OFF, it enables the reset gate in the divider reset circuit (par. 146) and its own input gate. When it comes ON, it furnishes a positive signal, enabling the count gate of the pulse frequency divider circuit, which allows a 6,000-pps signal to start the generation of sampling pulses (par. 147) for the receiver.

b. Sync control F/F No. 3 is turned OFF by F/O No. 3 (par. 96*i*) which in turn is triggered by one of the 6,000 pps applied to terminal 2. When F/F No. 3 is ON, bias from F/F No. 3 disables CR10. The combination gate comprising CR10 and CR13 is enabled by the combination of ON bias from ready control F/F No. 2 and ON bias from F/F No. 3 (appendix II, A of fig. 211). The positive bias from these gates enables CR11, allowing 6,000-pps pulses to pass through it and through C8 to terminal 2 of F/O No. 3, triggering the F/O, which turns F/F No. 3 OFF. The negative data (ZERO) signal through R11 overcomes the -12 volts applied to the input gate of F/O No. 3 at terminal 7.

c. F/F No. 3 is turned back ON again by the leading edge of the sync signal. Positive bias (ONE) of the sync pulse enables CR7, allowing one of the 6,000-pps pulses to pass through CR7 and C5 to terminal 2 of F/F No. 3. F/F No. 3 had been OFF (*a* above). Applying negative bias from terminal 3 to terminal 2 opens the gate at terminal 2 which had been closed by -12 volts applied at terminal 5. With the gate at terminal 2 open, the 6,000-pps pulse turns F/F No. 3 back ON.

146. Divider Reset Circuit

(fig. 92)

a. The divider reset circuit resets the pulse frequency divider circuit in preparation for a new frame. This is done by the application of a positive bias from F/F No. 6 and a negative bias from sync control F/F No. 3 to a gate which permits a reset pulse to pass through it to turn OFF all of the frequency divider BC stages (par. 147). When the TPC switch (fig. 172 (1)) is operated to the TEST position, the BC stages run continuously.

b. When F/F No. 6 is turned ON by the application of a negative pulse from the ready delay circuit, a positive output at terminal 3 enables CR1 through R1. A pulse from the 6,000 pps passes through CR1, C1, and C2 to the cathode of CR3. The positive portion of this output pulse is shorted to ground through CR2. When the TPC switch is in the NORM position, the negative pulse can pass through CR3 only when sync control F/F No. 3 is OFF. With F/F No. 3 OFF during the reset time slot (par. 145), diode CR3 is enabled, allowing the negative pulse to

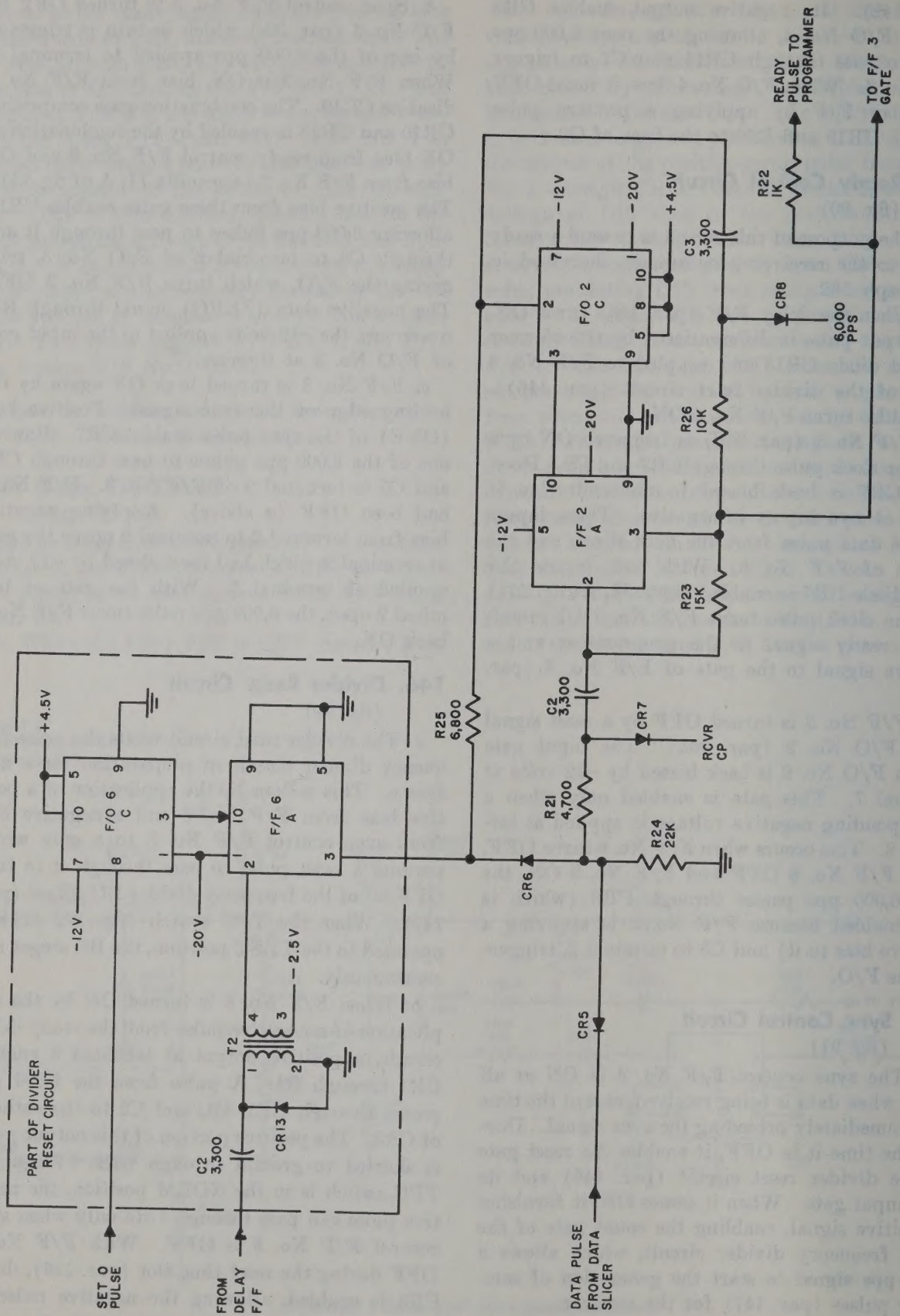


Figure 90. Ready control, simplified schematic.

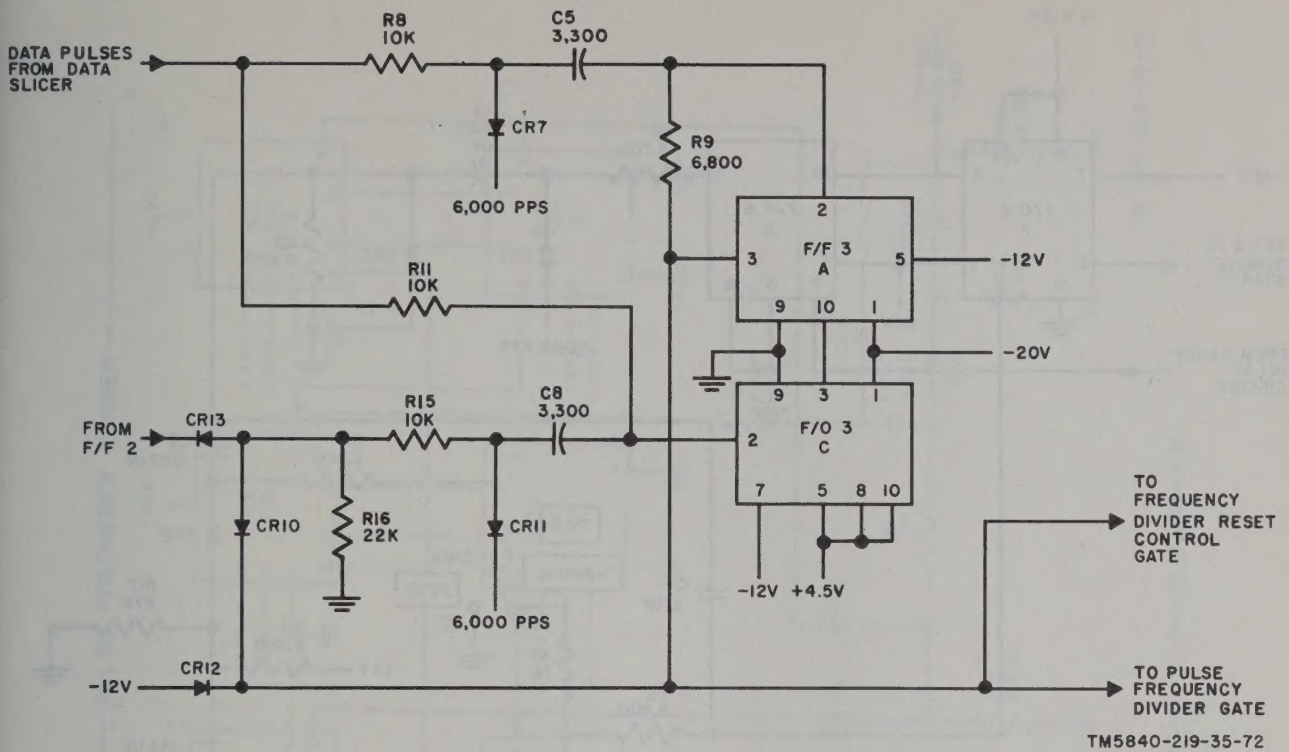


Figure 91. Sync control circuit, simplified schematic.

pass through it and through C3 to reset the BC stages (par. 147).

c. The pulse from the 6,000-pps source which resets the BC's is also routed from C1 through C4 to terminal 2 of F/O No. 6. One side of the input gate of F/O No. 6 is biased at -12 volts at terminal 7. The application of negative bias from F/F No. 3, when it is OFF, enables the input gate at terminal 2 and allows the pulse to trigger F/O No. 6, which then turns F/F No. 6 OFF.

d. When the TPC switch is set to the TEST position, the negative output bias from terminal 3 of F/F No. 3 is removed from the cathode of CR3. CR3 then is disabled and cannot pass a pulse to the frequency dividers to reset them. This switch is used during certain tests when an uninterrupted supply of sampling pulses from the pulse frequency divider circuit is wanted.

147. Pulse Frequency Divider and Slot Center Gate Circuits (fig. 93)

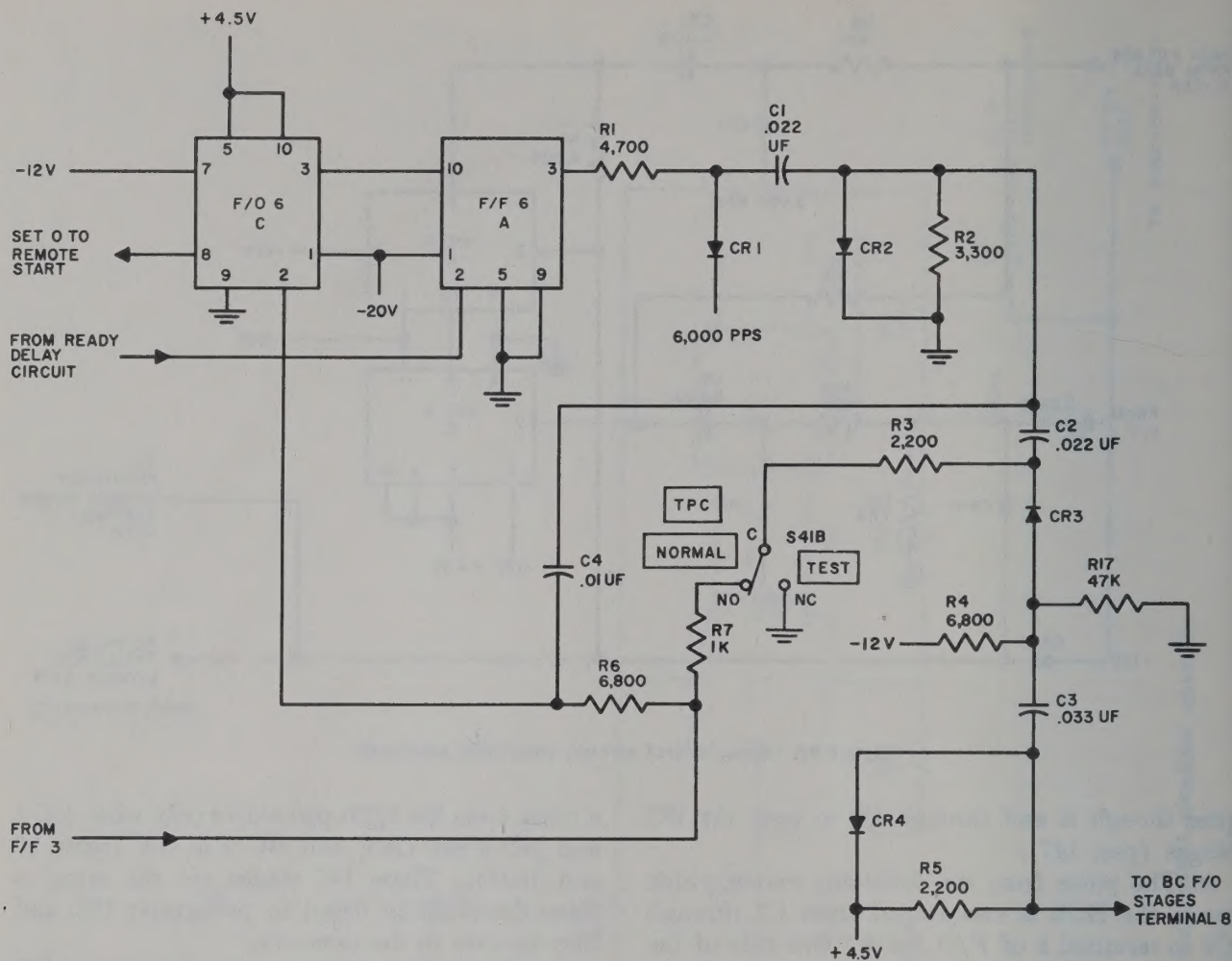
a. While the start of the frame is under control of the leading edge of the sync pulse (par. 145), the sampling (clock pulse) interval is under control of the three-stage binary counter of the pulse frequency divider. The slot center gate passes

a pulse from the 6,000-pps source only when BC 1 and BC 3 are OFF and BC 2 is ON (pars. 96 and 100d). These BC stages are the same as those described in detail in paragraph 121, and they operate in the same way.

b. All three BC stages have been reset to OFF before the count TCG is enabled (par. 146). When F/F No. 3 is turned back ON by the leading edge of the sync pulse (par. 145), its positive bias is applied through CR5 and R10 to remove the negative bias from CR8. This negative bias was obtained from -12 volts through R13 and R10. Since CR8 is now enabled, the 6,000-pps pulses through C7 to BC1 start the BC's counting these pulses. Starting from the first pulse which turns F/F No. 3 ON, the binary counter stages are left in the conditions shown below for each succeeding pulse.

6,000 pps No.	BC 1	BC 2	BC 3
1 F/F No. 3 comes ON.	0	0	0.
2	1	0	0.
3	0	1	0 coincidence with slot center gate.
4	1	1	0 sampling pulse generated.

On the third pulse following the appearance of the leading edge of the sync pulse, the biases from



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Figure 92. Divider reset, simplified schematic.

the three BC stages match the three inputs to the slot center gate.

c. With all three BC stages OFF, diode CR1 (fig. 93) is enabled by -20 volts through R22 and R1. CR6 is disabled by the OFF (-) bias from BC 2. When either BC 1 or BC 2 comes ON, the ON (+) bias disables CR1. When BC 2 is ON, it enables CR6 and allows a pulse to pass through it. Thus, when both BC 1 and BC 3 are OFF and BC 2 is ON, the fourth pulse passes through CR6, C3, CR1, and C1, and appears at the output as a sampling pulse.

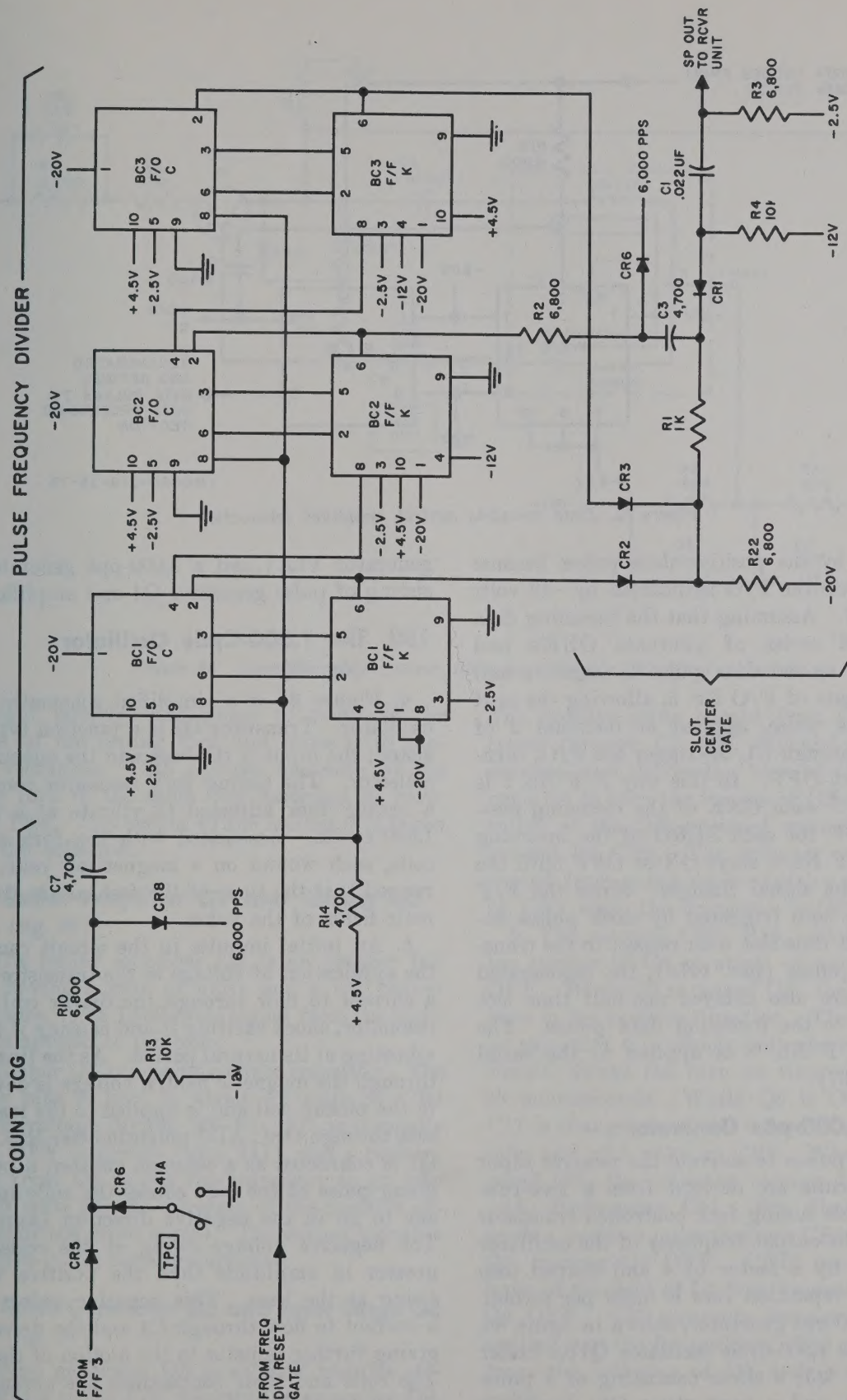
d. As the binary counters continue the count, coincidence occurs every eighth pulse, namely the 11th, 19th, 27th, etc. Since eight successive pulses of the 6,000 pps equal one time slot, and the binary counters are started by F/F No. 3 coming ON, the sampling pulse occurs at the middle of the sync pulse and of succeeding incoming data

pulses. For this reason, the receiver clock pulses are delayed one-half time slot with respect to the transmitter clock pulses.

148. Data Sampling Control Circuit (fig. 94)

a. The incoming signals from the data slicer are regenerated and retimed by the data sampling control circuit. The positive incoming data pulse (ONE) gates a clock pulse to turn an F/F ON, and the incoming negative data pulse (ZERO) shuts the F/F OFF. The F/F produces regenerated and retimed data pulses.

b. Data pulses from the data slicer are applied to terminal 2 of F/F No. 5 (par 94f) and terminal 2 of F/O No. 5 (par. 96k) through R13. The first positive data pulse, however, enables the gate at terminal 5 of F/F No. 5, and the next clock pulse turns F/F No. 5 ON. F/O No. 5 is



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Figure 93. Pulse frequency divider circuit and slot center gate, simplified schematic.

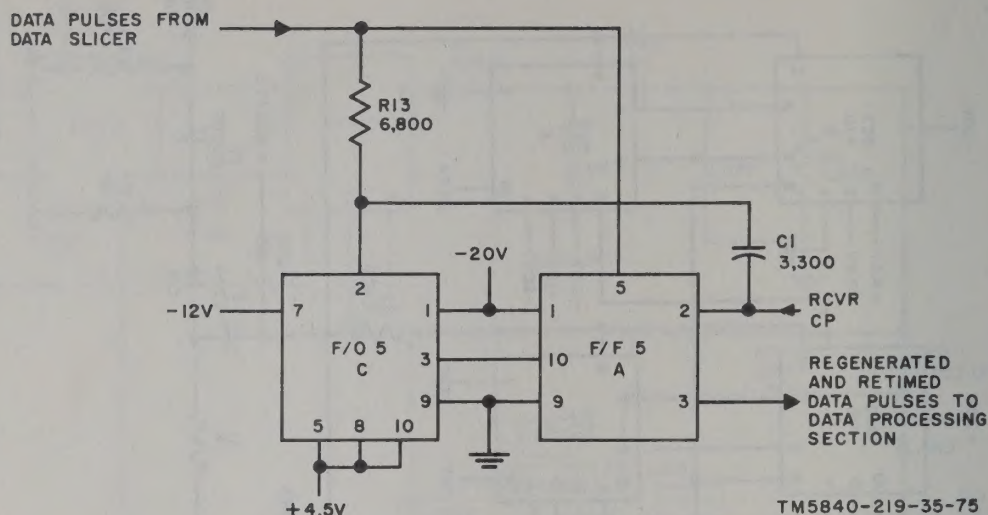


Figure 94. Data sampling control, simplified schematic.

not affected by the positive data pulses because the gate within the F/O is disabled by -12 volts at terminal 7. Assuming that the incoming data pulses are a series of alternate ONE's and ZERO's, the second data pulse is negative and enables the gate of F/O No. 5, allowing the next receiver clock pulse, applied at terminal 2 of F/O No. 5 through C1, to trigger the F/O, turning F/F No. 5 OFF. In this way F/F No. 5 is turned ON for each ONE of the incoming message and OFF for each ZERO of the incoming message. F/F No. 5 stays ON or OFF until the polarity of the signal changes. Since the F/F and F/O are both triggered by clock pulses delayed one-half time slot with respect to the transmitter clock pulses (par. 147d), the regenerated data pulses are also delayed one-half time slot with respect to the incoming data pulses. The output of F/F No. 5 is applied to the serial adder(par. 167).

149. The 6,000-pps Generator

a. Trigger pulses to activate the receiver input transistor circuits are derived from a free-running 1,500-cycle tuning fork controlled transistor oscillator. The output frequency of the oscillator is multiplied by a factor of 4 and shaped into pulses whose repetition rate is 6,000 per second.

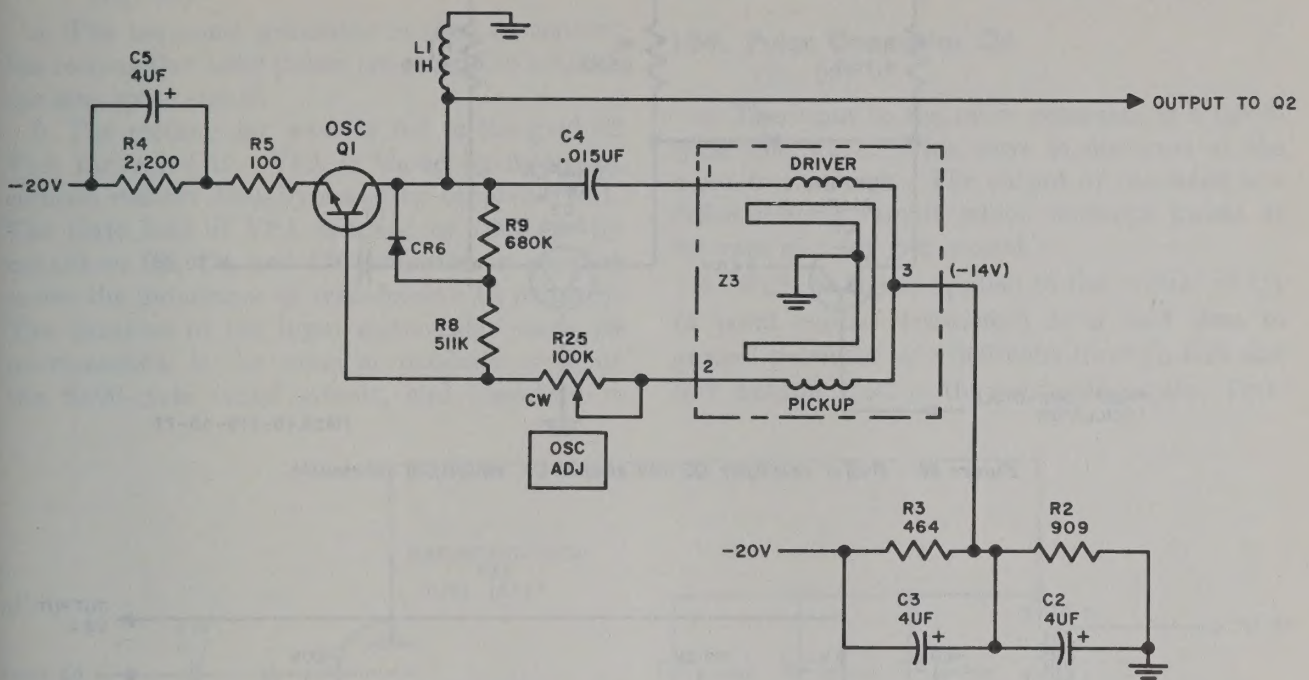
b. The 6,000-pps generator, shown in figure 83, consists of the 1,500-cycle oscillator Q1; a buffer Q2; a shaper Q3; a slicer consisting of a pulse generator Q5, and a reset stage Q6; harmonic

generator V3A; and a 6,000-pps generator consisting of pulse generator Q4 and amplifier V3B.

150. The 1,500-Cycle Oscillator (fig. 95)

a. Figure 95 is a simplified schematic of the oscillator. Transistor Q1 is a junction type transistor; the input is the base and the output is the collector. The tuning fork resonator consists of a tuning fork adjusted to vibrate at a rate of 1,500 cycles. Associated with the fork are two coils, each wound on a magnetized yoke, so arranged that the tines of the fork are in the magnetic fields of the yokes.

b. An initial impulse in the circuit caused by the application of voltage to the transistor causes a current to flow through the driver coil of the resonator, shock exciting it and causing it to start vibrating at its natural period. As the tines move through the magnetic field, a voltage is developed in the pickup coil and is applied to the transistor base through OSC ADJ potentiometer R25. Since Q1 is connected as a common emitter, a positive-going pulse at the base causes the collector voltage to go in the negative direction (app. III). The negative voltage swing at the collector is greater in amplitude than the positive voltage swing at the base. This negative swing causes a current to flow through C4 and the driver coil, giving further impetus to the motion of the tines. The coils and their connections are arranged so that the amplified pickup coil voltage is always of



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Figure 95. Amplifier synchronizer, 1,500-cps oscillator, simplified schematic.

the right polarity and phase to reinforce the motion of the tuning fork and cause it to continue vibrating. CR6 reduces damping of the tuning fork in the same way described in paragraph 126e. The output of the oscillator is taken from the collector.

151. Buffer Amplifier Q2 and Shaper Q3 (fig. 96)

a. The buffer amplifier Q2 is an emitter follower having a gain of unity and a low output impedance. The 1,500-cycle signal from the oscillator is applied to the base.

b. Shaper Q3 is a point contact transistor. The emitter bias is held to about -2 volts by CR1 and the voltage divider R6-R1. Q1 is normally in the OFF condition (app. III), and a positive signal from Q3 causes the transistor to go into the ON state for the duration of the positive excursion of the input signal. The output signal is a positive-going rectangular wave.

152. Pulse Generator Q5 and Reset Stage Q6 (fig. 97)

a. Pulse generator Q5 is an F/F bistable circuit similar to the F/F described in appendix III.

The positive-going output from Q3 is differentiated through C1 (fig. 96) and associated resistance, and drives the base of Q5 far enough negative to turn the transistor ON. The positive spikes of the differentiated wave are shunted to ground by CR9. The collector voltage is prevented from going more negative than -12 volts by CR2 when the transistor is OFF.

b. The network CR2, R16, and R17 maintains the emitter of Q6 at about -4 volts when Q5 is OFF. When Q5 is turned ON, the emitter of Q6 rises in the positive direction. The rise is slowed by capacitor C10 which, with the resistors in the circuit, delays the turn on time of Q6 F/O by 83 microseconds. While Q6 is OFF, capacitor C11 is charged to about -17 volts at the collector side, and -2.5 volts at CR5. When Q6 is triggered ON, the collector voltage drops to about -2.5, discharging C11. The discharge of C11 sends a positive pulse through CR4 to the base of Q5, turning Q5 OFF. CR12 prevents the collapse of the field of L2 from prematurely turning Q6 OFF. CR3 prevents damage to Q6 if the emitter goes too far positive. The output is taken from the collector of Q5 and is a rectangular pulse.

153. Harmonic Generator V3A

(fig. 98)

a. The harmonic generator is used to convert the rectangular 1,500 pulses per second to a 6,000-cps sine wave signal.

b. The rectangular wave is fed to the grid of V3A through C10. V3A is biased by means of cathode resistor R20, bypassed by capacitor C11. The plate load of V3A is tuned to 6,000 cps by capacitors C7, C8, and C9 connected in parallel across the inductance of transformer T2 primary. The duration of the input rectangular wave, 83 microseconds, is the same as one-half cycle of the 6,000-cycle tuned circuit, and therefore is

favorable for the generation of the fourth harmonic of the 1,500-cycle oscillator frequency.

154. Pulse Generator Q4

(fig. 99)

a. The input to the pulse generator is a 6,000-cycle sine wave. This wave is distorted at the input to the stage. The output of the stage is a differentiating circuit which develops pulses at the rate of 6,000 per second.

b. With no signal applied to the emitter of Q4 (a point contact transistor) it is held close to ground potential by +300 volts through R26 and R27, holding CR7 in the conducting state. Dur-

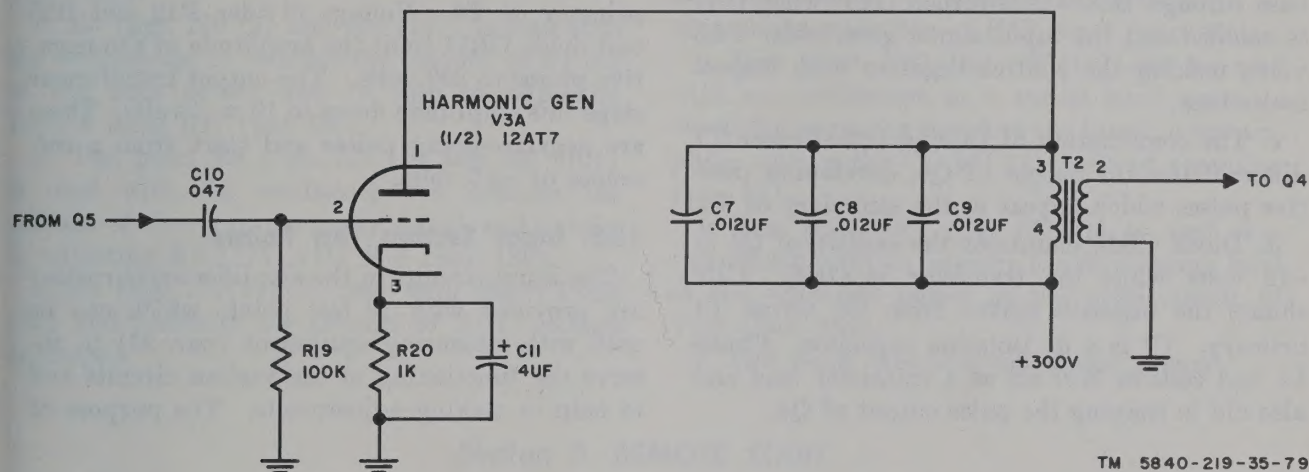


Figure 98. Harmonic generator V3A, simplified schematic.

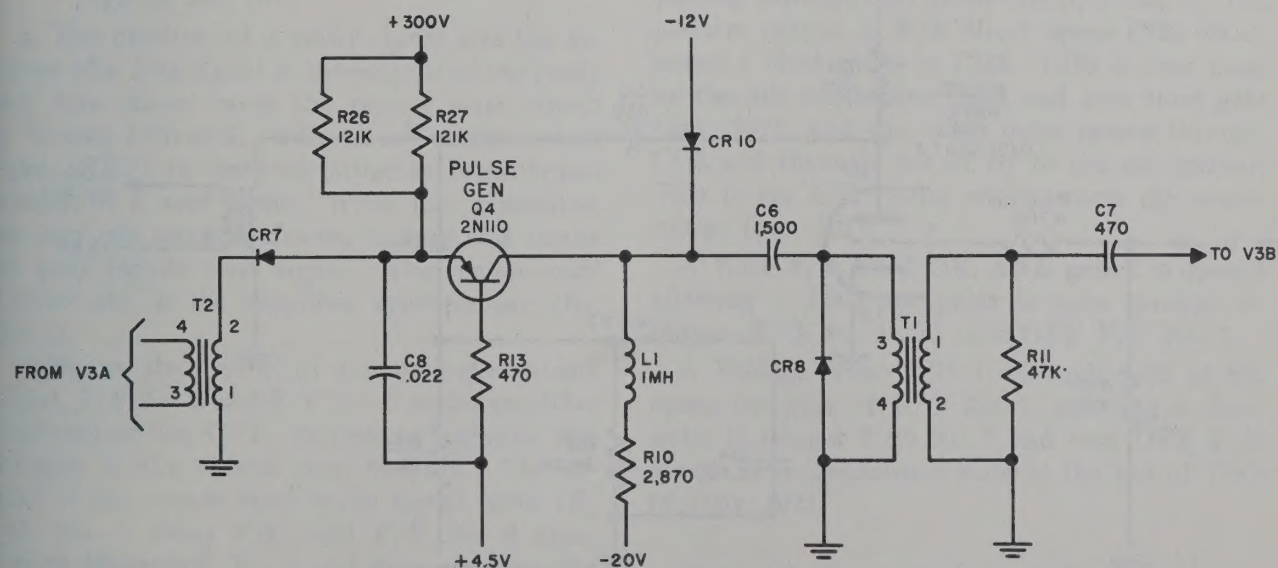


Figure 99. 6,000-pps pulse generator, simplified schematic.

ing the negative part of the input cycle C8 is charged through the low impedance source of T2 secondary and CR7. However, when the input signal goes positive, C8 holds the anode of CR7 at near ground potential for a short time, disabling CR7, and allowing the emitter voltage to rise in the positive direction toward +300 volts at a rate determined by C8 and the resistance of the circuit. When the input signal recedes from the maximum positive value, CR7 again becomes enabled and abruptly returns the emitter to the signal potential. The transistor acts as an F/F and is turned ON when diode CR7 is disabled, and capacitor C8 charges to a positive voltage sufficient to overcome the positive voltage at its base through R13. It is turned OFF when CR7 is enabled and the input signal goes below +4.5 volts, making the emitter negative with respect to its base.

c. The combination of C6 and transformer T1 differentiates the output of Q4, developing positive pulses which appear at the secondary of T1.

d. Diode CR10 maintains the emitter of Q4 at -12 volts while the transistor is OFF. CR8 shunts the negative spikes from C6 across T1 primary. C7 is a dc isolation capacitor. Choke L1 and resistor R10 act as a transistor load and also aid in shaping the pulse output of Q4.

155. Pulse Amplifier V3B

(fig. 100)

a. The input to V3B is a series of positive pulses having a repetition rate of 6,000 per second. The output is a series of negative pulses of the same rate, having a duration of about one microsecond and an amplitude of 10 volts.

b. The grid of V3B is heavily biased by -12 volts through R12; however, the positive pulses applied to it from the preceding stage overcome this bias and cause some grid current to flow, thus clipping the peaks of the pulses by developing a voltage drop across R22. The output pulses developed across plate load resistor R21 are negative and are coupled through C12 to the primary of T3. Voltage divider R12 and R23 and diode CR11 limit the amplitude of the negative pulses to 200 volts. The output transformer steps this amplitude down to $10 \pm .5$ volts. These are negative-going pulses and start from a reference of -2.5 volts.

156. Input Section Test Points

The input circuits in the amplifier synchronizer are provided with 12 test points which can be used with measuring equipment (par. 23) to observe the functioning of the various circuits and to help in making adjustments. The purpose of

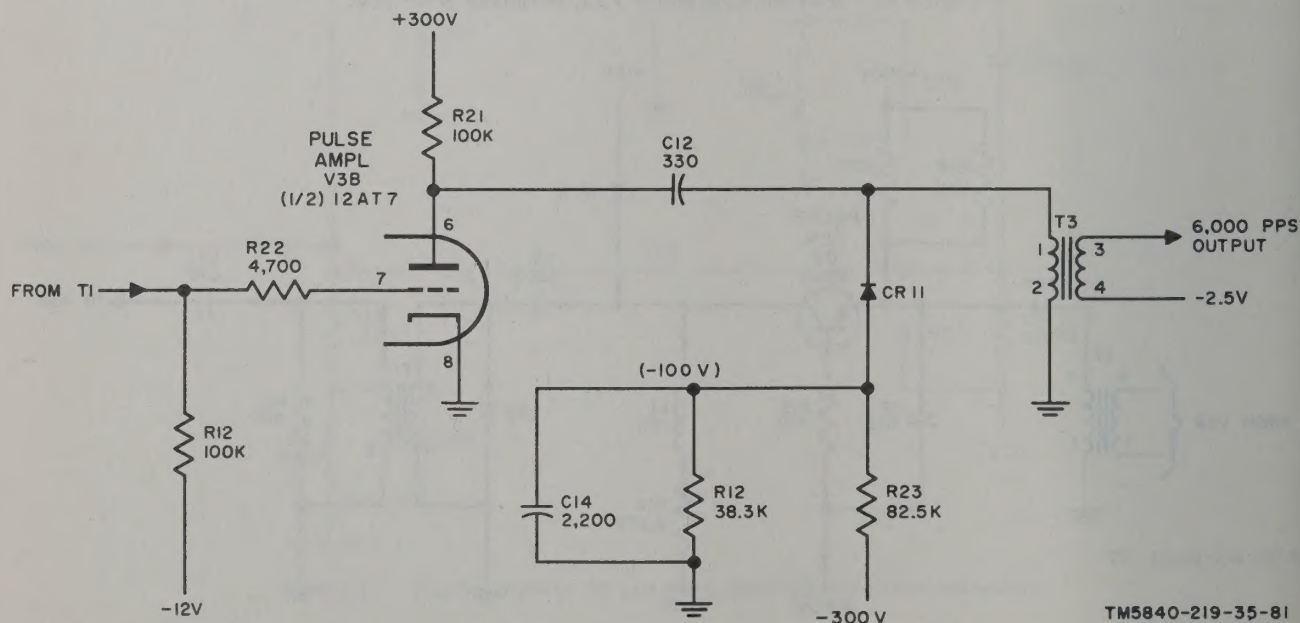


Figure 100. 6,000-pps pulse amplifier, simplified schematic.

these test points is described in *a* through *l* below. All measurements are made from the test point to ground. The methods used for making adjustments and for troubleshooting the circuits associated with the test points are described below.

a. Test point E1 (figs. 170 (1) and 159 (10)) is used with the oscilloscope to observe the waveform of the 1,500-cycle oscillator. It indicates whether or not the circuit is oscillating, and if the required feedback has been applied (par 150).

b. E2 (figs. 170 (2) and 159 (10)) is used with the oscilloscope to observe the time at which the emitter voltage has risen to the value required to turn ON the delay F/F. It also indicates the value of emitter voltage at the turn ON time (par. 143).

c. E3 (figs. 170 (1) and 159 (10)) is used with the oscilloscope to indicate the amount of slicing of the data pulses, and to help in adjusting DATA ADJ R17 (par 139).

d. Test point E4 (figs. 170 (1) and 159 (10)) is used with the oscilloscope to indicate the amount of slicing of the ready signal, and to help in adjusting READY ADJ R13 (par. 139).

e. E5 (fig. 170(1)) is used with the VTVM (dc) and indicates the amount of AGC voltage developed.

f. Test point E6 (fig. 170(1) and 159(2)) is a convenient point to connect an oscilloscope to observe the regenerated data output of F/F No. 5 (par. 94*f*).

g. Test point E7 (fig. 170(1)) is used as a point to connect an oscilloscope to observe the presence of the ready signal from F/F No. 2 (par. 94*d*).

h. Test point E8 (fig. 170(2) and 139) is used as a convenient point to connect an oscilloscope to observe the operating time of F/F No. 6. This test point can be used with test point E2 (*b* above) to time the operation of the delay F/F and F/F No. 6 (fig. 132).

i. Test point E9 (fig. 170(2) and 132) is a convenient point to connect an oscilloscope to observe the operation of F/F No. 3 (par. 94*e*).

j. Test point E10 (fig. 170(1)) can be used with an oscilloscope or a signal level meter to check the incoming signal at the input to the amplifier during the CDG/TAC mode of operation (par. 37).

k. Test point E11 (fig. 170(1)) is used as a convenient point to measure the dc clipping level of the 6,000-pps pulses in the plate circuit of V3B (par. 155).

l. Test point E14 is a convenient ground.

Section II. REMOTE START

157. CDG/TAC Operation, Block Diagram (figs. 83 and 101)

a. The presence of a ready signal and the absence of a data signal at the outputs of the ready and data slicers cause the remote start circuit to become activated. This circuit sends a start pulse (STP) to the transmitter to begin transmission of a new frame. When the transmitter has sent one complete frame, it stops and awaits the next remote start signal. The remote start circuits are in the amplifier synchronizer (fig. 170(1)).

b. Before the arrival of a remote start ready signal, F/F No. 2 and F/F No. 6 in the amplifier synchronizer are OFF, furnishing negative bias voltages to the remote start circuits. The arrival of the remote start ready signal turns ON F/F No. 1, delay F/F, and F/F No. 6 (par. 136*c*). With F/F No. 2 and data negative, the negative output of AND gate 1 and the positive

output of F/F No. 6 open CG1. The clock pulse passing through CG1 turns ON F/F No. 7. The positive output of F/F No. 7 opens CG2 which passes a clock pulse to CG3. CG3 is kept open by the idle transmitter reset and auto start gate (par. 107), and the clock pulse passes through CG3 and through 3-5 of S1 to the transmitter. This is the STP pulse which starts the transmitter (par. 107).

c. With F/F No. 7 ON, AND gate 2 is opened allowing a 6,000-pps pulse to pass through to trigger F/O No. 6 and turn OFF F/F No. 6.

d. Voltage from TSG 1, through 2-12 of S1, opens the gate of F/O No. 7, allowing a clock pulse to trigger F/O No. 7 and turn OFF F/F No. 7. The transmitter stops at the end of TSG 56 (par. 107).

Figure 101. Remote start circuits, block diagram.
(Contained in separate envelope)

158. CDG/TAC Operation, Circuit Analysis (fig. 102)

a. Diode CR1 in the remote start section is disabled by -12 volts applied to it through resistor R2. Diode CR3 is also disabled by a negative bias from F/F No. 7 (par. 94g), which is OFF. In order for a clock pulse (STP) to be sent back to the transmitter, it must pass through both of these diodes. During TS 57 and until the transmitter is reset (par. 107), a negative bias appears at the cathode of CR1 through R1, over-

No. 7 is closed. Also if the bias from F/F No. 6 is negative, CR7 is disabled and the input gate is closed. Conditions (2), (3), and (4) are met by a ready signal (600-cps signal for three time slots) and the absence of data (1,500-cps signal).

c. When both F/F No. 6 and F/F No. 7 are ON, CR5 is enabled through the AND gate consisting of CR2, CR4, and R5, and the first pulse thereafter of the 6,000 pps passes through CR and is used as a trigger for F/O No. 6, which turns OFF F/F No. 6 (par. 146). At TS 1 the

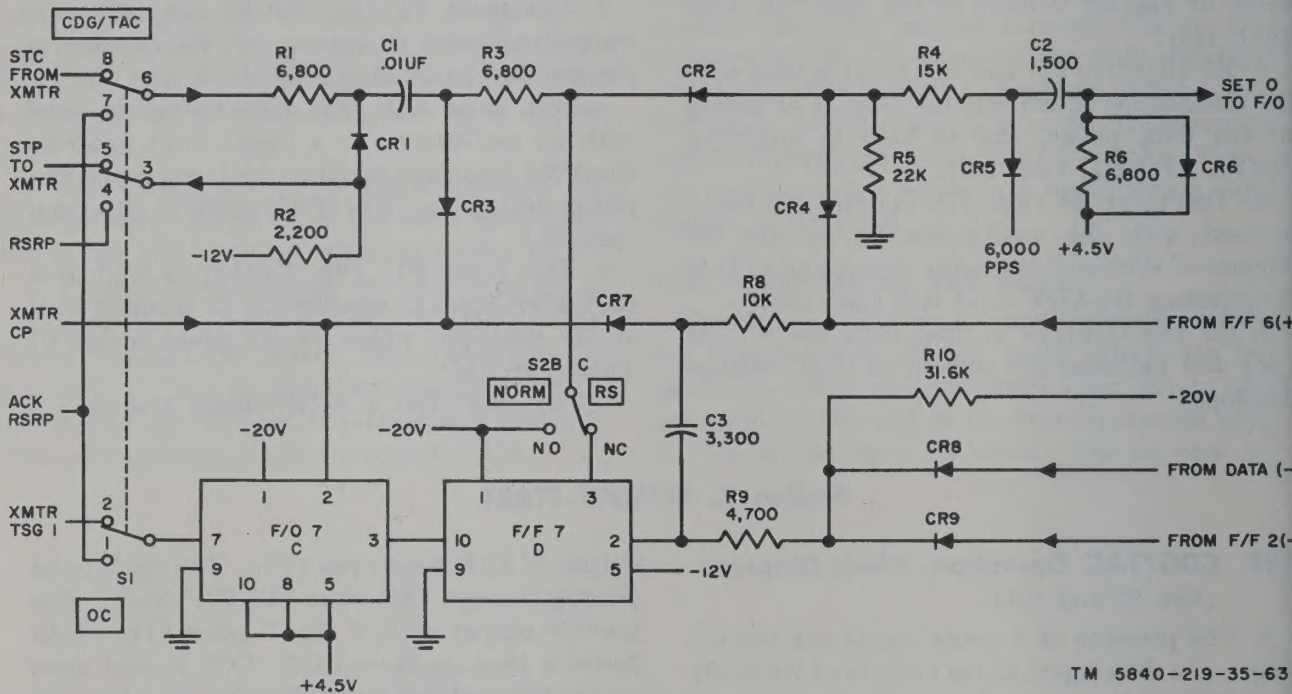


Figure 102. Remote start, simplified schematic.

coming the -12 volts back bias. When F/F No. 7 is turned ON, the anode of CR3 is made positive, and the clock pulse passes through CR3, C1, and CR1, completing the reset of the transmitter programming circuits.

b. F/F No. 7 can only be turned ON by a combination of the following: (1) a clock pulse from the transmitter; (2) a negative (ZERO) data signal; (3) a negative (OFF) bias from F/F No. 2; and (4) a positive (ON) bias from F/F No. 6. If either the F/F No. 2 output or the data signal is positive, the input gate of F/F

gate at terminal 7 of F/O No. 7 is opened and the clock pulse at terminal 2 triggers the F/O turning F/F No. 7 OFF.

159. OC Operation (fig. 101)

The operation of the remote start circuit during OC operation is the same as described in paragraph 158 except that switch S1 is in the OC position. The negative enabling voltage for CG3 and the positive enabling voltage for F/O No. 7 are obtained from associated equipment.

Section III. PROGRAMMER

160. General

(fig. 103)

a. The purpose of the programmer in the receiver is the same as that of the program generator in the transmitter (par. 104). It provides a selection of time slot enabling intervals (TSG) and a source of clock pulses. At the proper times within the message frame, these pulses activate the receiver circuits in the way required to accept the incoming data pulses and translate the digital words of the message into the form originally presented to the transmitter.

b. The principal elements of the programmer are: 1) clock pulse generators, 2) reset control circuits, 3) manual start circuits, 4) ring counter circuits, and 5) time slot gate circuits. These principal elements are shown in the block diagram of the receiver (fig. 131) and in the programmer block diagram (fig. 103) and are discussed in paragraphs 161 through 165. The times of occurrence of the several functions of the programmer circuits are illustrated in the timing chart (fig. 132).

c. Two inputs are applied to the programmer: 1) sampling pulses from the input section, and 2) a ready signal from F/F No. 2 in the input section. The sampling pulses trigger the clock pulse generator. The ready signal starts as a negative bias, goes positive just after the coincidence of the ready and data signals received from the distant transmitter, and goes negative again at the end of the data signal during the guard slot between the data and sync signals.

d. The ready signal prepares the reset control circuits for a new frame and resets the ring counters. When the ready signal goes negative, the ring counters are started, the clock pulse generators are operating, and time slot gate voltages are generated.

161. Clock Pulse Generator Circuits

(fig. 104)

a. The clock pulse generators in the receiver are identical to those in the transmitter and function in the same way to generate a set zero pulse and three clock pulses (par. 105). The input to the clock pulse generators in the receiver is a series of sampling pulses from the slot center gate (par. 147). CP1 and CP2 are distrib-

uted to receiver circuits. CP3 is used only by associated equipment.

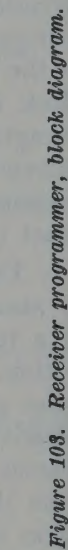
b. Two other circuits, the test control (TC) circuit and the single pulse (SP) generator, are a part of the clock pulse generator circuits and are used for making certain system tests (par. 199, table VII). With the PC switch down, depressing the RECY switch recycles the frame to the desired time slot, as determined by the settings of the units and tens selector switches, and stops the ring counters at that slot. The single pulse generator generates one clock pulse each time the SP switch S49 is depressed, thus advancing the ring counters one time slot. These circuits are the same as the recycle and SP circuits described in paragraphs 105e and 105f.

162. Reset Control Circuits

(fig. 105)

a. Assume that the receiver reset control circuits are idle, awaiting a ready signal (+) from the input section. RC 1 F/F (par. 94i) is OFF disabling CR6, and thereby preventing clock pulses from starting the ring counters. Since RC 2 F/F (par. 94j) is also OFF, both CR8 and CR9 are enabled, and the input to RC 2 F/F is enabled by the OFF bias from its terminal 6 through R12 to its terminal 2.

b. Upon the arrival of the ready signal (+) from ready control F/F No. 2, the gate at terminal 5 of RC 1 F/F is enabled allowing the next clock pulse to turn RC 1 F/F ON. With RC 1 F/F ON, the positive output from its terminal 6 enables CR6. At the end of the ready signal (-), CR7 is enabled allowing a clock pulse through CR6 and C4 to pass through CR7 and C6. From this point the clock pulse goes four ways: through CR8, C5, and S54 to turn ON TR 00; through CR9, C7, and S54 to turn ON UR 0; to terminal 2 of RC 2 F/F, turning it ON; and to terminal 2 of RC 1 F/O (par. 96o), triggering it and turning RC 1 F/F OFF. The circuits remain in this condition until receiver time slot (TS) 51. At TS 51 RC 2 F/F is ON, holding the gates open at 5 of URR and TRR. A clock pulse passes through CR3 and C2 to trigger both URR and TRR. The reset pulses from these two F/O's reset the ring counters, and the reset pulse from TRR turns OFF RC 2 F/F. This is the end of the frame.



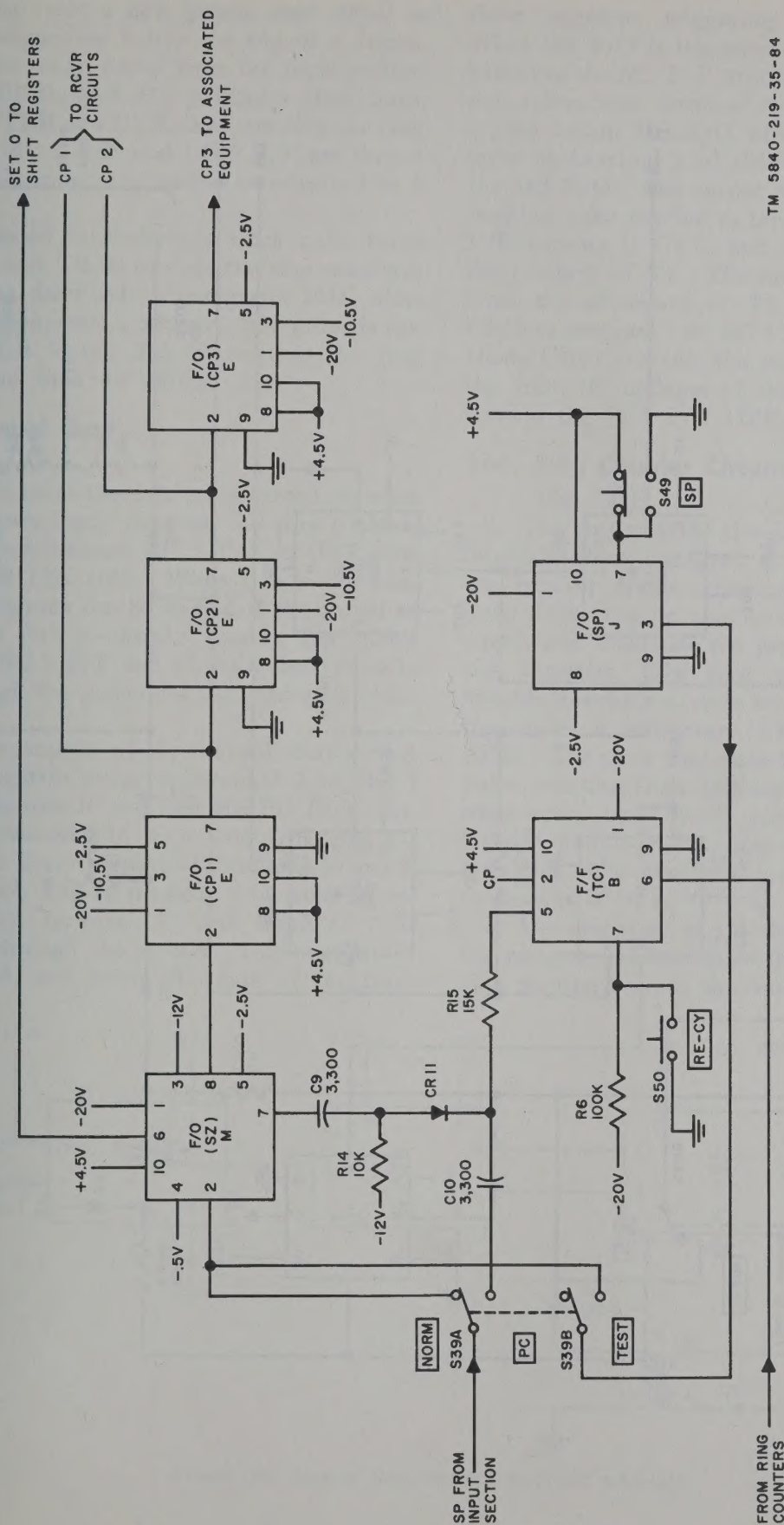


Figure 104. Receiver clock pulse generator circuits, simplified schematic.

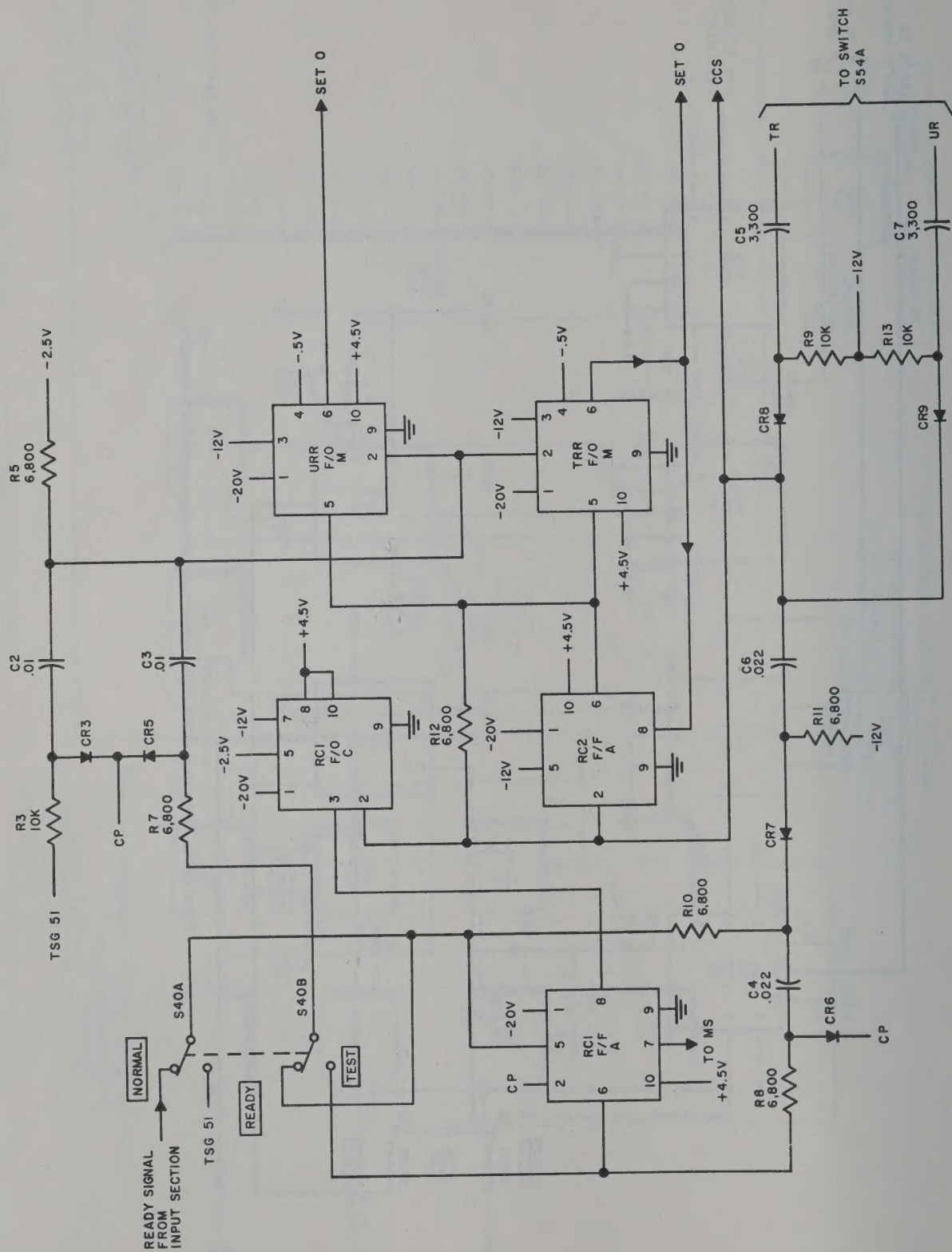


Figure 105 Receiver reset control circuits, simplified schematic.

c. In the event a new remote start signal is sent to the receiver before the end of a frame, the positive ready signal from the input section enables CR5 through R7, passing a clock pulse to trigger TRR and URR, thus resetting the ring counters. RC 1 F/F and RC 2 F/F are turned ON, and the rings are started as described in *b* above.

d. As stated in *b* above, a clock pulse turns ON UR 0 and TR 00 to start the ring counters; however, as described in paragraph 164e, when double scale operation is used, this pulse is applied to UR 9 and TR 50 starting the ring counters one time slot earlier.

163. Manual Start

(fig. 106)

a. In the event the data set is turned on when no signals are being received, the ring counters will not start because RC 1 F/F is OFF, disabling CR6 (fig. 105). When this is the case, the ring counters can be started if the circuit of MS switch S48 is closed. Closing the circuit turns ON RC 1 F/F and allows a clock pulse to pass through the gates and start the ring counters.

b. The operation of the manual start circuit sends a negative pulse to terminal 7 of RC 1 F/F. Terminals 10 and 7 of MS PG F/O (par. 99c) are connected to +4.5 volts, charging C1 (within the F/O) positive at terminals 10 and 7. When switch S48 is pressed, +4.5 volts is removed from terminal 7, and terminal 7 is grounded through the switch. This charges C1 through R5, and drives the base of the tran-

sistor negative, triggering the MSPG F/O. When the F/O is triggered, the output pulse is passed to the MS F/F, turning it ON. The output, taken from terminal 6 of the F/F enables a gate within MS F/O which allows the clock pulse at terminal 2 of the MS F/O to trigger the MS F/O. The output of the MS F/O is a positive pulse applied to terminal 10 of the MS F/F turning it OFF, and also through C8 to the primary of T1. The negative output pulse from the secondary of T1 is passed through CR10 to terminal 7 of RC 1 F/F turning it ON. Diode CR10 prevents the positive pulse, resulting from the collapse of the field of T1, from turning the RC1 F/F OFF prematurely.

164. Ring Counter Circuits

(fig. 107)

a. The ring counter circuits provide enabling intervals (bias voltages) at selected points in the receiver frame. During these intervals a clock pulse may be used to trigger a transistor circuit and thus time the performance of a circuit function. The ring counter circuits are bistable transistor circuits arranged in two counting chains, a units ring (UR) and a tens ring (TR). The units ring steps ONE for each clock pulse, counting from 0 through 9. The tens ring steps every tenth clock pulse. There are ten bistable circuits in the units ring and six in the tens ring. The two form a decade counter able to count to 60.

b. The operation of the ring counters used in the receiver is identical to the operation of the ring counters used in the transmitter (par. 106),

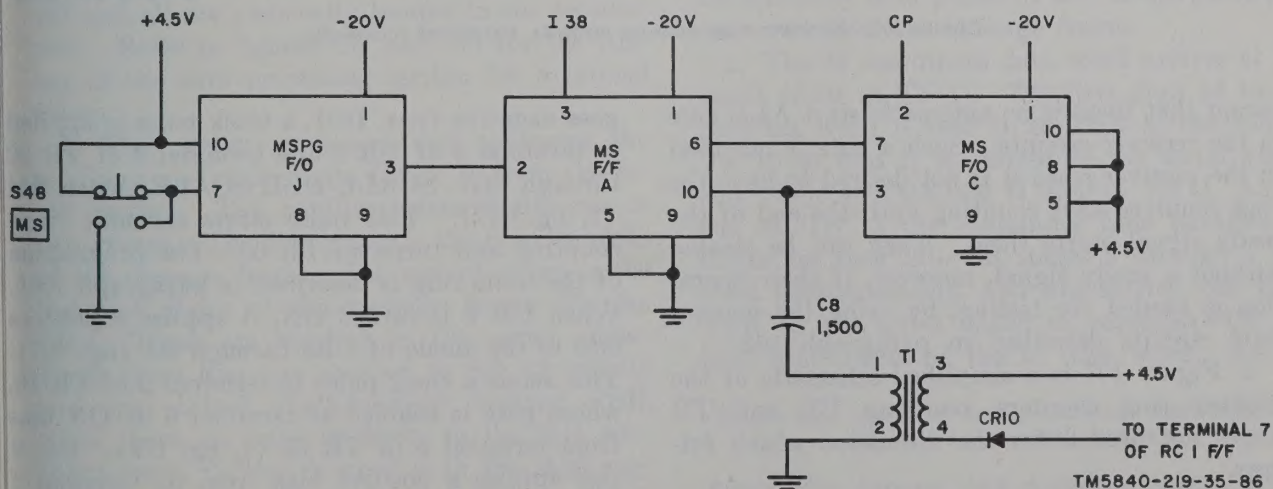


Figure 106. Manual start circuits, simplified schematic.

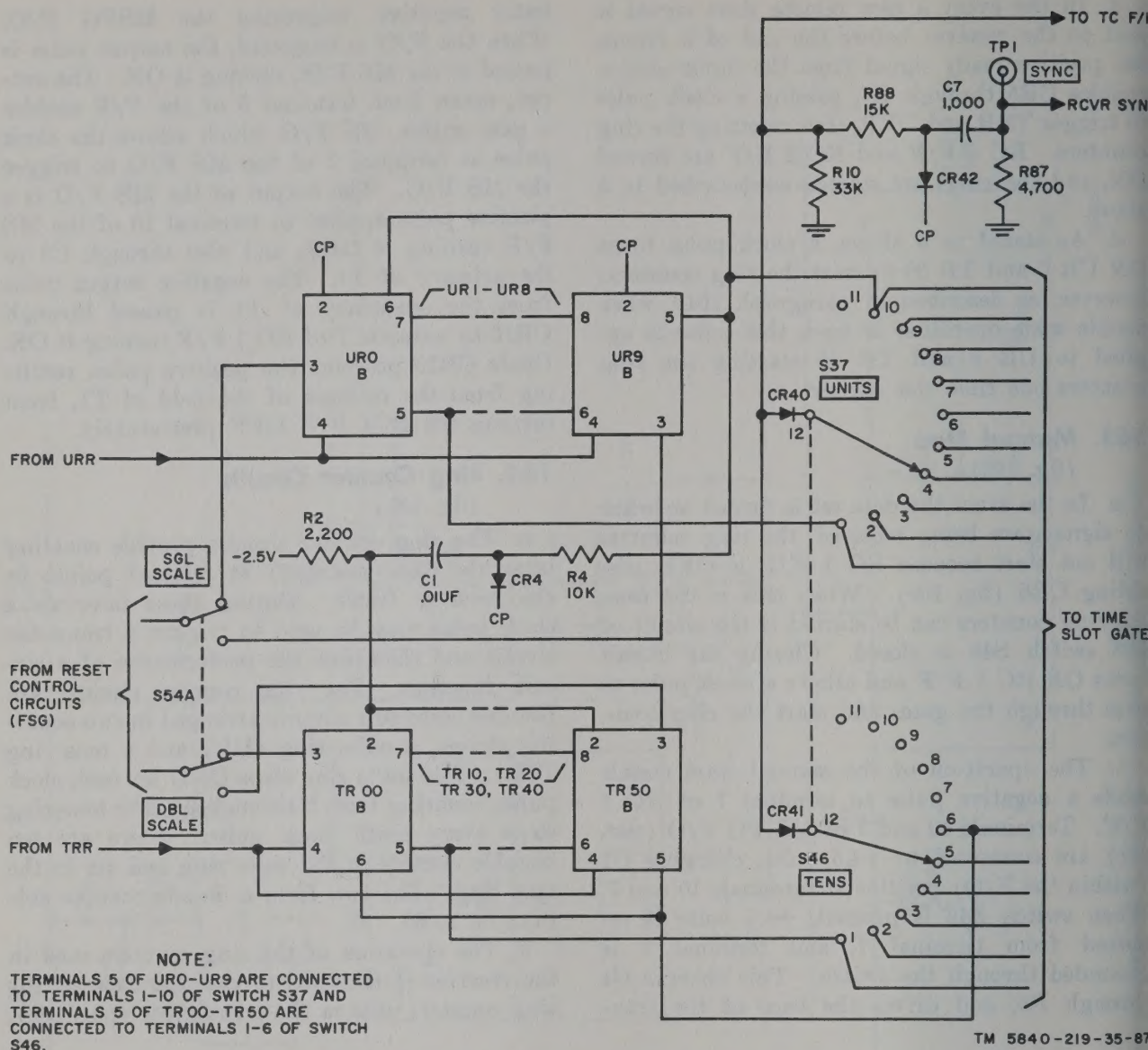


Figure 107. Receiver ring counter circuits, simplified schematic.

except that there is no automatic start ALL gate in the receiver circuits. Such a gate is not used in the receiver since it is not desired to have the ring counters start counting until the end of the ready signal starts them. They can be started without a ready signal, however, if their operation is needed for testing, by using the manual start circuits described in paragraph 163.

c. Figure 107 is a simplified schematic of the receiver ring counters, omitting UR and TR stages not needed for the discussion which follows.

d. At the end of the ready signal all ring counter stages are reset. When the ready signal

goes negative (par. 162), a clock pulse is applied to terminal 3 of UR 0 and terminal 3 of TR 00 through SGL SCALE-DBL SCALE switch S54 (1, fig. 172). This pulse starts the unit rings counting and turns on TR 00. The progression of the units ring is described in paragraph 106b. When UR 9 is turned ON, it applies a positive bias to the anode of CR4 through R4 (fig. 107). This sends a clock pulse to terminal 2 of TR 10 whose gate is enabled at terminal 6 by ON bias from terminal 5 of TR 00 (1, fig. 172). UR 9 also applies a positive bias from its terminal 5 to terminal 6 of UR 0 (fig. 107), allowing a clock pulse at terminal 2 to turn ON UR 0, thus

keeping the ring counters in operation. Each time UR 9 is turned ON, diode CR4 is enabled, and a clock pulse is applied through C1 to turn ON the tens ring stage whose gate is enabled by the ON bias of the preceding tens ring stage. This progresses until the rings are stopped by a reset pulse applied to terminal 4 of each ring counter stage from the reset control circuits.

e. During double scale operation, SGL SCALE-DBL SCALE switch S54 is in the DBL SCALE position. The operation of the ring counters is identical to the operation described above, except that the rings are started one time slot earlier (par. 178) when the start pulse from the reset control circuits is applied to UR 9 and TR 50. The reason for this earlier start is to compensate for the earlier start of the binary counters in the transmitter (par. 121).

f. The output (terminal 5) of each of the units ring stages is connected to a contact of UNITS switch S37, and the corresponding outputs of the tens ring stages are connected to contacts of TENS switch S46. The contact arms of the two

switches are connected together through diodes CR40 and CR41 as shown in figure 107. The ON bias of the UR or the TR stages, which are connected together by these two switches, develops a positive bias across resistor R10. This bias voltage enables CR42, allowing a clock pulse to be sent through R88 to the TC F/F for use with the recycle circuit (par. 161b). The same clock pulse is passed through C7 to the SYNC jack TP1, where it can be used to synchronize an oscilloscope for certain tests (table VII), and is also sent to the cabinet terminal connectors where it is available for use by associated equipment.

165. Time Slot Gate Circuits

a. The time slot gate circuits operate in the same way as described in paragraph 106.

b. A connection is brought out from TSG 14 of the time slot gates which appears at the cabinet terminal connectors (3, fig. 162). This may be used by associated equipment as a signal indicating that auxiliary data pulses 1-10 have been received.

Section IV. DATA PROCESSING SECTION

166. General

(fig. 108)

a. The data processing section consists of seven sets of functional circuits: serial adder circuits, shift register circuits, shift pulse control circuits, parallax read-in circuits, auxiliary read-in and release circuits, height unknown pulse circuits, and off-scale detection circuits. All of these circuits are shown in block form in figure 131 and all are physically located in the receiver unit. Refer to figures 109 and 110 for the timing of the data processing section for a typical frame.

b. This section processes and separates the auxiliary and data digits fed to it from the input section. The auxiliary data digits are in two groups. The first group is the first 10 digits of the message frame. The second group is the last two digits of the message frame (B, fig. 132). These are applied to the serial adder. From there they are applied to SR 13 serially and are shifted, digit-by-digit, toward PSR. Since there are only 10 digits to the first auxiliary word, the entire word is in the shift registers by the time the first digit arrives at SR 4. The digits are then read in to the auxiliary

lockups (ALU) at TS 11 (for single scale operation). Each of the ALU stages assumes the condition of the SR stage associated with it, and operates its auxiliary relay (AR) to send the auxiliary word to associated equipment. The auxiliary 11, 12 digit word is not processed in the data set receiver. Instead, time slot gate voltages, clock pulses, and data pulses from the receiver are sent to associated equipment where the auxiliary data pulses 11 and 12 are gated and extracted from the message frame.

c. The H coordinate data word arrives at the serial adder at TS 11. The first digit of the H parallax word is read in to PSR at the end of TS 10 so that it is shifted to the serial adder coincident with the first H digit at TS 11. At the end of TS 11 the remaining nine parallax H digits are read into SR stages 8 through 1 and PSR simultaneously, and are shifted out from PSR to the serial adder to coincide with the next nine digits of the H data word. As the

Figure 108. Receiver data processing, block diagram.
(Contained in separate envelope)

Figure 109. Receiver data processing section, general timing diagrams.
(Contained in separate envelope)

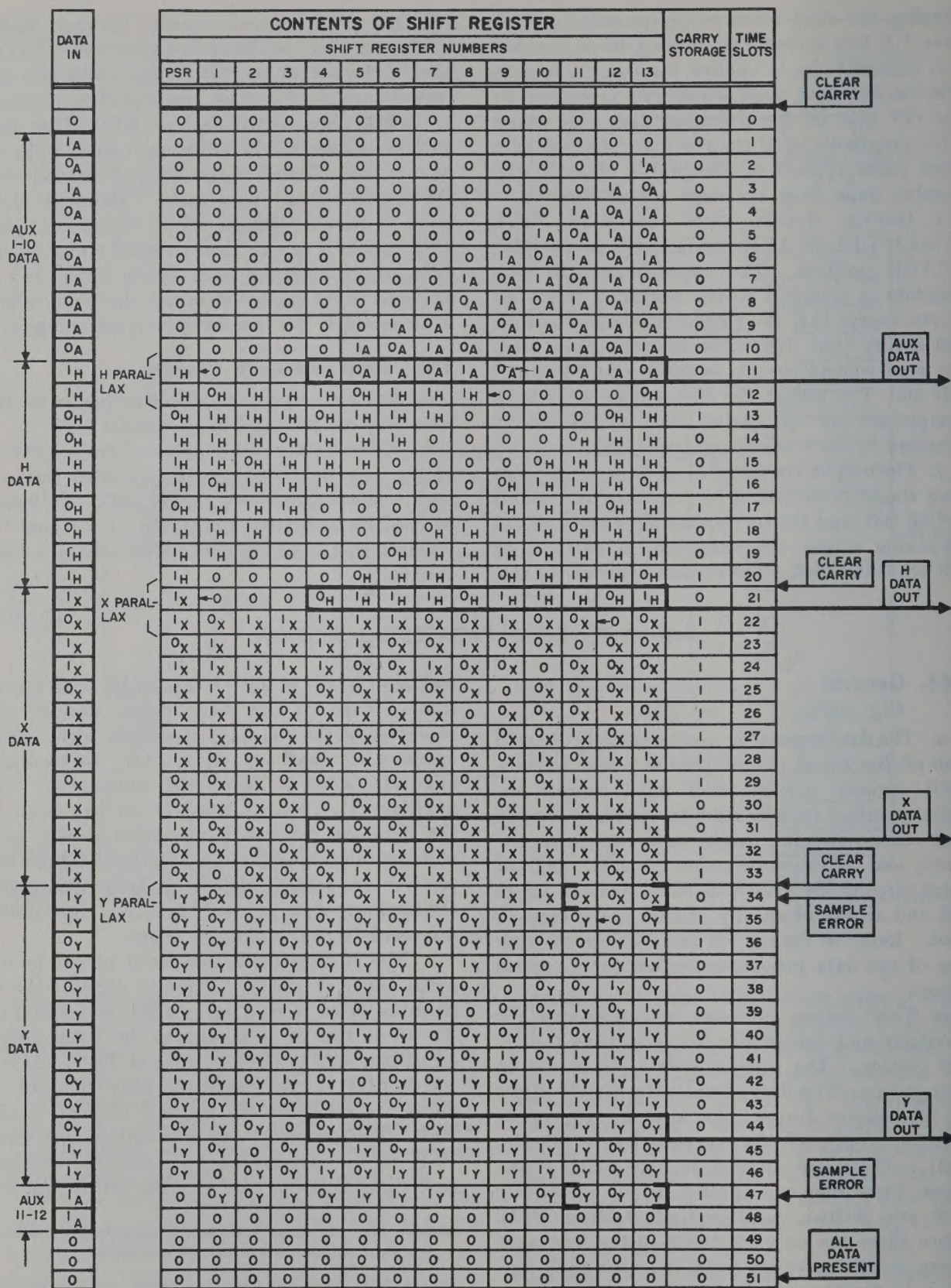


Figure 110. Receiver data processing section, typical timing diagrams.

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first data digit and the first parallax digit are added in the serial adder, the sum digit is applied to SR 13. All succeeding parallax and data digits are similarly added in the serial adder and are applied to SR 13 serially. When the 10-digit sum word is in SR stages 13 through 4, it is read out at the end of TS 21 by the data read-in gate in the decoding network and amplifier section (par. 179).

d. The X coordinate data word is handled in the same way as the H data word. At the end of TS 20, the first X parallax digit is read in to the PSR, and coincides with the first X data digit in the serial adder. The remaining X parallax digits are read in to the shift register stages at the end of TS 21 and are shifted out to the serial adder coincident with the arrival of the remaining digits of that X data word. The sum word is fed into SR 13, shifted down to SR 4, and at the end of TS 31 is read in to the data lockups.

e. The Y coordinate data word is handled in the same way as the X data word. At the end of TS 33, the first Y parallax digit is read in to PSR and coincides with the first Y data digit in the serial adder. The remaining Y parallax digits are read in to the shift register stages at the end of TS 34, and are shifted out to the serial adder coincident with the arrival of the remaining digits of the Y data word. The sum word is fed into SR 13 and shifted down to SR 4, and at the end of TS 44, is read in to the data lockups.

f. During normal operation the sum digits of parallax and data are modified by the associated equipment to provide target slant ranges instead of ground ranges. When this is done, the digits from the serial adder are routed to associated equipment, and data, modified for slant range, is returned to the shift register at SR 13. From there it is read out into the data lockups.

g. All the information of the X and Y data words can be expressed with 10 digits after parallax has been added; consequently, SR stages 11, 12, and 13 should all be OFF by TS 34 (fig. 110). If they are not OFF, it is an indication that data received will place the target off scale. The off scale detection circuits provide a signal to associated equipment in the event any one of the SR stages 11, 12, or 13 is on at this time (par. 177).

167. Serial Adder

(fig. 111)

a. The serial adder is an assemblage of logic circuits which function in accordance with the convention for addition of binary numbers (app. I). The circuits are gate circuits, all of which are used in some form in other parts of the data set. When reference is made in the following discussion to positive pulses, it is meant that the pulse is a positive-going pulse, and has a value near enough to ground potential to enable a gate to pass a negative clock pulse. The positive pulses derived from F/F circuits are never actually positive with respect to ground unless they have been biased by a fixed positive voltage.

b. As indicated in paragraph 166c, the serial adder performs the summation of parallax and incoming data words. There are three incoming signals to this unit: data, parallax, and a carry digit. As each digit of the parallax and data appears in coincidence at the data and parallax inputs, the sum of the two must appear at the output in the form of a clock pulse if the sum is ONE or no clock pulse if the sum is ZERO. If the data and parallax are both ONE's, a zero must appear at the output (par. 5 of appendix I), and the carry ONE must be stored and applied to the following data digit and its corresponding parallax digit. If these two succeeding digits are both ONE's to which a carry ONE is to be added, the output must be ONE and the carry ONE must be continued for application to the next coincident digits of data and parallax.

c. The logic circuits of the serial adder provide four conditional paths between input and output to produce a clock pulse if any of the following conditions exist:

- (1) All (data, parallax, and carry) present.
- (2) Data only.
- (3) Parallax only.
- (4) Carry only.

d. The summing process is performed by six logic gates associated with positive or negative time control gates as required. These gates are analyzed in paragraph 169. The ALL gate of figure 111 is the same as the AND gate of part A of figure 211, except that three F/F circuits must be ON simultaneously to develop a pulse sufficiently positive to enable the associated CG. The negative AND gates (2, 3, 4, and 5, fig. 111)

produce a negative output only when two negatives (ZERO's) appear at the input. If either or both inputs are ONE's, the bias at the output is positive.

e. The carry storage generates a ONE (gate 6) if both data and parallax are ONE, and turns off a ONE (gate 5) in carry (or generates a ZERO) if both data and parallax are ZERO.

f. The auxiliary digits are passed through the data only path, gate No. 2, since these digits do not require summation.

Figure 111. Serial adder, block diagram.
(Contained in separate envelope)

168. Operation of Serial Adder (fig. 111)

a. An example of how the serial adder functions is given below. Assume that there is a data word of 10011 and a parallax of 01011 to be added to it. The numbers are arranged with the least significant digit at the left.

Carry	-----	01100
Data	-----	11001
Parallax	-----	11010
Sum	-----	01111

b. During the first time slot both the data and parallax digits on the left are ONE (+) and their sum is ZERO (-). Gate 6 is the only gate which will pass a clock pulse with this combi-

nation; therefore, the output is ZERO, and the CS F/F (par. 94o) is turned ON to carry a ONE.

c. During the second time slot there is a ONE (+) from the carry F/F and both data and parallax are ONE (+). The only gate which accepts all ONE's is gate 1. The output is ONE, and the carry remains ONE because the F/F has not been turned OFF.

d. During the third time slot there is still ONE to carry, and both data and parallax are ZERO. The carry only gate in this case is the only gate to pass a clock pulse, and the output is ONE. Now that data and parallax are both ZERO (-), gate 5 with its two negative inputs permits a clock pulse to trigger CCS F/O (par. 96r). When the F/O is triggered, it turns the F/F OFF, removing the carry ONE for the next digit.

e. During the fourth time slot there is no carry. Data is ZERO (-) and parallax is ONE (+). The parallax only gate now allows a clock pulse through it, presenting a ONE at the output.

f. For the last digit there still is no carry. Data is ONE (+) and parallax is ZERO (-). The data only gate in this case is the one to pass the clock pulse to produce a ONE at the output.

g. At the end of each coordinate data and parallax sum word the carry F/F must be turned OFF in order that a ONE which may be left

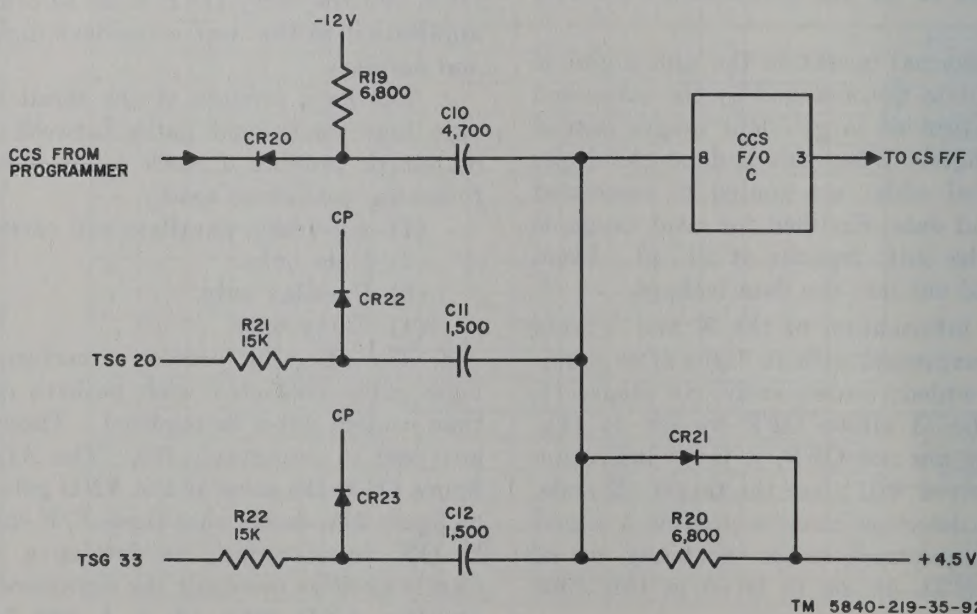


Figure 112. CCS gate circuits, simplified schematic.

from the summation of the preceding word will not be carried over. The reset is done through the gate circuits shown in figure 112, and the reset pulses trigger the F/O which resets the F/F.

h. At the beginning of the frame when RC 1 F/O in the programer is triggered (par. 162b), the same reset signal is sent to the reset gate (fig. 112). The negative bias is applied to the cathode of CR20, enabling it by overcoming the -12 volts applied through R19. The accompanying negative clock pulse triggers the F/O, clearing the Y data of the preceding frame.

i. At TS 20 (end of H data) and TS 33 (end of X data) a positive bias is applied to diodes CR22 and CR23, respectively, enabling them and allowing clock pulses to pass through to trigger the F/O.

j. Diode CR21 and resistor R20 prevent the positive gate voltages from exceeding +4.5 volts at terminal 8 of the F/O.

169. Serial Adder Gate Circuits

(fig. 113)

a. All Present Gate Circuit. With this circuit, a clock pulse appears at the output terminal if all three inputs are positive (ONE). With all inputs positive, CR2 is conducting, and a clock pulse passes through CR2 and C1 to shift register 13. However, if any one of the three inputs is negative, the negative bias disables CR2 through R1, and a clock pulse cannot pass through CR2 to the output.

b. Data Only Circuit. This circuit sends a clock pulse to the output if the data bias is present (+) and both parallax and carry are not present (-). With carry and parallax negative, CR10 and CR11 are disabled, and CR12 is enabled by -20 volts through R10 and R11. With data present (+) CR13 is enabled, allowing a clock pulse to pass through CR13, C7, CR12, and C6 to the output. If either carry or parallax is present, the positive bias through the associated diode applies a positive bias to the cathode of CR12, disabling it, and preventing the passage of a clock pulse to the output.

c. Parallax Only Circuit. This circuit is identical to the circuit in *b* above, except for the input connections. In this circuit CR8 is enabled by a positive parallax bias, and CR7 is disabled if either carry or data is positive.

d. Carry Only Circuit. This circuit is identical to the circuit in *b* above, except for the input connections. In this circuit CR19 is enabled by a positive carry bias, and CR18 is disabled if either data or parallax is positive.

e. Carry Storage Circuit. Whenever the data and parallax are both present (+), a carry ONE is required. In this case the gate within the F/F at terminal 5 is enabled, and a clock pulse at terminal 2 triggers the F/F ON. If, however, either data or parallax is negative, the gate within the F/F is disabled, and the clock pulse cannot pass through the gate to turn the F/F ON.

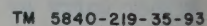
f. Clear Carry Storage Circuit. This circuit removes the carry bias from the serial adder circuits if no carry is required for the summation. The positive carry bias is provided when the carry storage F/F is ON (*e* above). If either parallax or data is present, carry may be required, and the carry storage F/F, if already ON, will be left ON. If neither parallax nor data is present, no carry for the next time slot is required. In this case the negative data bias enables the gate within the F/O at terminal 2, and the negative parallax bias enables CR 9 to let a clock pulse through to terminal 2 to trigger the F/O and turn OFF the F/F.

170. Serial Adder Carry Storage Gate

(fig. 112)

a. The carry storage F/F is turned ON by pulses from the serial adder and turned OFF by the clear carry storage F/O (par. 169).

b. The clear carry storage F/O is triggered by clock pulses from gate circuits enabled by the CCS signal from RC 1 F/O and by TSG 20 and TSG 33. The gate voltage for CCS is accompanied by a clock pulse. The gate voltage enables CR20 and allows the clock pulse to pass through C10 to trigger the F/O. At TSG 20, CR22 is enabled by the gate voltage applied to its diode through R21, enabling CR22 and allowing the clock pulse to pass through it and C11 to trigger the F/O. At TSG 33, CR23 is similarly enabled and the clock pulse passes through CR23 and C12 to trigger the F/O. Diode CR21 and resistor R20 keep CCS F/O terminal 8 at +4.5 volts between pulses. Each time the F/O is triggered it turns OFF CS F/F, clearing the carry ONE at the end of each coordinate sum word.



172

171. Height Unknown Pulse

(2, fig. 172)

During time slot 20 for single scale operation and time slot 19 for double scale operation, a height unknown pulse (HUP) is sent from the receiver to associated equipment. Diodes CR27, CR28, and resistor R27 form an AND gate. If a data ONE is present during the selected time slot, a positive pulse of one time slot duration is generated and appears at J2-19 of the transmitter unit. This pulse represents the tenth digit of the H coordinate.

172. Use of TDC and DATA Switches

(fig. 114)

a. During certain tests (table VII) it is necessary to set single data pulses into the serial adder. This is done by the DATA and TDC switches. When the DATA switch is in the TEST position, the serial adder data input is disconnected from the amplifier synchronizer and connected to the TDC switch.

b. With the DATA and TDC switches in the positions shown in figure 114, the serial adder data input is grounded, which is equivalent to a data ONE. If the ring counters are operating, there is a continuous series of ONE's being generated. If the ring counters are stopped by setting the PC switch at TEST, single ONE's of data are applied to the serial adder each time the ring counters are stepped with the SP switch (par. 164).

c. If it is desired to set in a data word consisting of ONE's and ZERO's, TDC switch S47 is set to 1 (up) for ONE's and 0 (down) for ZERO's, a ONE or a ZERO being generated each time the ring counters are stepped.

173. Shift Pulse Control Circuits

(fig. 115)

a. The shift pulse control circuits control the timing of the clock pulses sent to the shift register to stop the shift registers for one time slot four times each frame. This is done to clear the shift register at the end of TS 10, the H coordinate data during TS 21, the X coordinate data during TS 34, and the Y coordinate data at the end of the frame at TS 46.

b. There are two sets of gates: one, the enable gate, for permitting the shift pulses to pass to the shift registers, and the second, a disable gate, for preventing the shift pulses from passing to the shift registers. This is done by turning ON and OFF SPD F/F (par. 94m) whose output controls a shift pulse generator (SPG). The F/F, in turn, is turned ON by clock pulses passing through selected gates, and is turned OFF by clock pulses passing through other selected gates.

c. The SPD F/F is first turned ON at the end of TS 0. The gate within the F/F is enabled by positive gate voltage at terminal 5, and the clock pulse at the end of TS 0 turns the F/F ON. At the end of TS 10 the gate within SPD

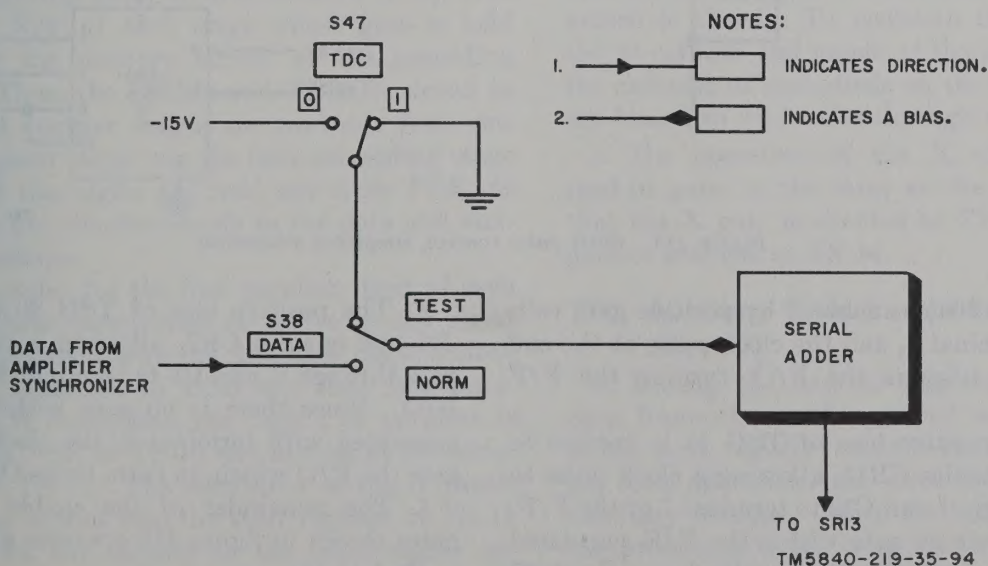


Figure 114. TDC and DATA switches, simplified schematic.

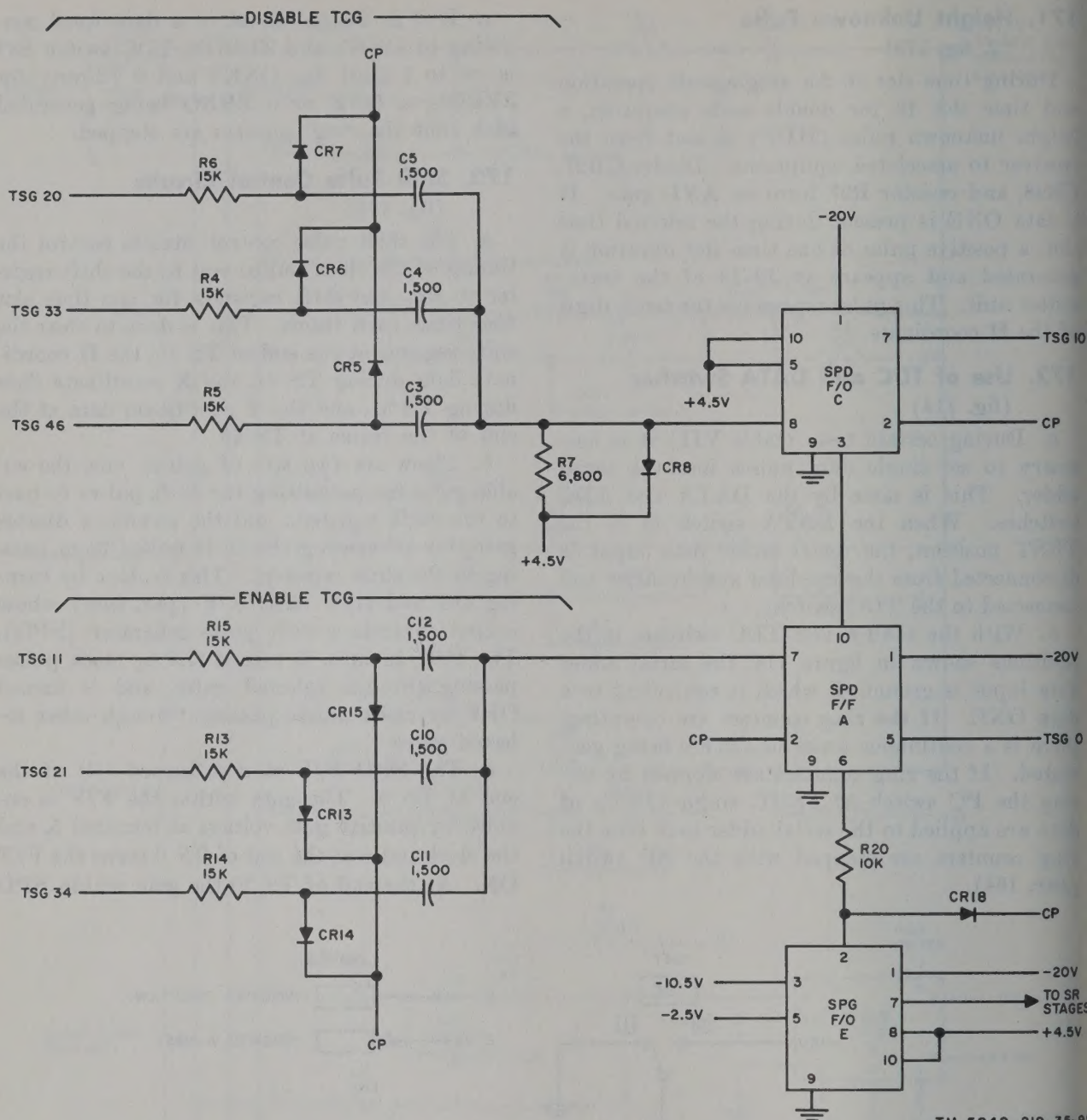


Figure 115. Shift pulse control, simplified schematic.

F/O (par. 96u) is enabled by positive gate voltage at terminal 7, and the clock pulse at the end of TS 10 triggers the F/O, turning the F/F OFF.

d. The positive bias of TSG 11 is applied to R15 and enables CR15, allowing a clock pulse to pass through it and C12 to terminal 7 of the F/F. Since there is no gate within the F/F associated with terminal 7, the clock pulse turns the F/F ON at the end of TS 11.

e. The positive bias of TSG 20 is applied to R6 and enables CR7, allowing a clock pulse to pass through it and C5 to terminal 8 of the SPD F/O. Since there is no gate within SPD F/O associated with terminal 8, the clock pulse triggers the F/O which, in turn, turns OFF the F/F.

f. The remainder of the enable and disable gates shown in figure 115 operates exactly as described above.

g. Since the shift register is reset at TS 46

and not started until TS 0 of the next frame, the data in the shift registers is lost because the memory circuits of the SR stages have died out.

h. Each time the F/F is turned ON, diode CR18 is enabled, permitting clock pulses to pass through to SPG F/O. SPG F/O is triggered once for each clock pulse applied to its terminal 2. The output of SPG F/O is a shift pulse similar to a clock pulse, which is used to advance the shift registers (par. 174).

174. Shift Register

(fig. 116)

a. The parallax digits are read in to SR stages 11 to 1 (par. 94*p*) and PSR (par. 94*l*) for the X and Y coordinates, and SR stages 8 to 1 and PSR for the H coordinate (fig. 108). The sum data digits are applied to the gate input circuit of SR 13 and are shifted along stage-by-stage toward PSR. The basic elements of the shift register are shown in figure 116.

b. Shift clock pulses are applied over a common bus to all 13 shift register stages and PSR. Likewise, the set zero (SZ) pulses are applied to all 13 stages and PSR. The timing of these pulses is such that the SZ arrives to turn OFF all F/F's just before the shift pulse is applied to the gates. The time constant of the memory circuits is such as to remember the ON condition of its own F/F (if it had been ON) until the shift pulse arrives at the gate of the succeeding stage. With this arrangement the SZ turns the F/F of all stages OFF simultaneously, and the shift pulse, arriving about 40 microseconds later, turns ON the F/F of each stage whose gate is held open by the memory circuit of the preceding stage. Thus, the ONE's and ZERO's stored in the shift register stages are read out from one shift register stage into the next succeeding stage until all the digits are read out from PSR, or are read out simultaneously to the data and auxiliary lockups.

c. In order for the first parallax digit of each of the three coordinates to arrive at the serial adder coincident with the first data digit, a clock pulse is admitted to PSR one time slot early. For the H coordinate, the digit 1 of parallax is read into PSR at TS 10 and arrives at the serial adder at TS 11. The remainder of the H parallax word is read into the shift register at TS 11 and shifts out serially to the serial adder coincident with the remaining nine digits of the H

data word. In the same way, digit 1 of X parallax and digit 1 of Y parallax are read in one time slot early at TS 20 and TS 33, respectively.

d. The operation of a shift register stage is described in detail in paragraph 122. The sequence of operation is described in paragraph 166.

175. Parallax Read-in

(fig. 117)

a. Parallax correction is read in to the shift register by allowing a clock pulse to turn ON an SR stage if the parallax correction for that digit of the coordinate word is a ONE, and to leave the SR stage OFF if the parallax correction for that digit of the coordinate word is a ZERO.

b. A clock pulse is applied to a common bus for the H coordinate at TS 11; a clock pulse is applied to a second bus for the X coordinate at TS 21, and a clock pulse is applied to a third bus for the Y coordinate at TS 34.

c. Switches and isolation diodes connect the individual SR stages to the parallax read-in busses so the parallax word can be applied by the operator as required.

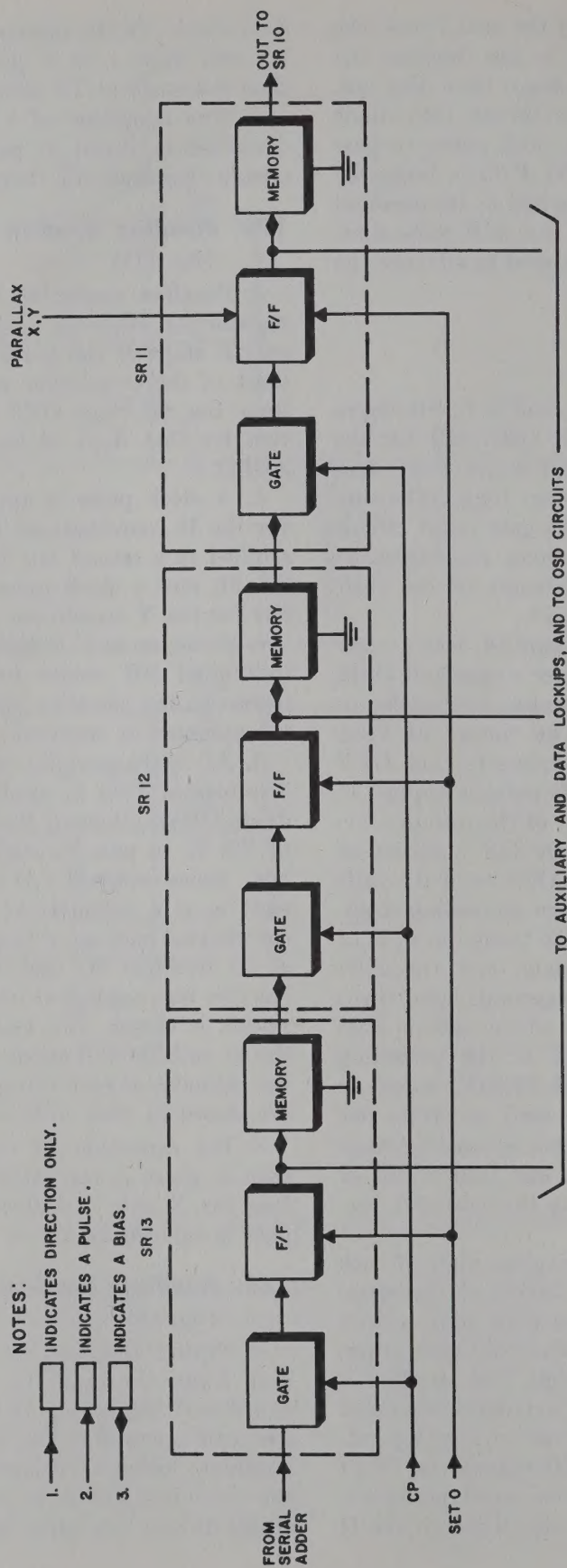
d. All three parallax read-in gates are alike. The bias of TSG 11 applied through R8 enables diode CR39, allowing the clock pulse at the end of TS 11 to pass through CR39 and C6 to the bus. Since terminal 7 of each SR stage (A package) is at a potential of +4.5 volts, because of the internal package wiring and the +4.5-volt bias at its terminal 10, each of the isolation diodes has this bias applied at its anode when a parallax switch is closed. To maintain the same potential at cathode and anode of the isolation diodes, the cathodes of each diode on the H parallax bus are biased to +4.5 volts through resistor R9.

e. The operation of the X and Y parallax read-in gates is the same as the H gate except that the X gate is enabled at TS 21, and the Y gate is enabled at TS 34.

176. Auxiliary Read-in and Release Circuits

(fig. 118)

a. During the first 10 receiver time slots of each frame the auxiliary word is being built up in the shift register. At the end of TS 11 (single scale operation) the word is read out to the auxiliary lockups. Since the auxiliary word of the preceding frame is in the ALU (par. 97*d*) stages during this build up time, the ALU's must



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Figure 116. Basic elements of shift register in receiver, block diagram.

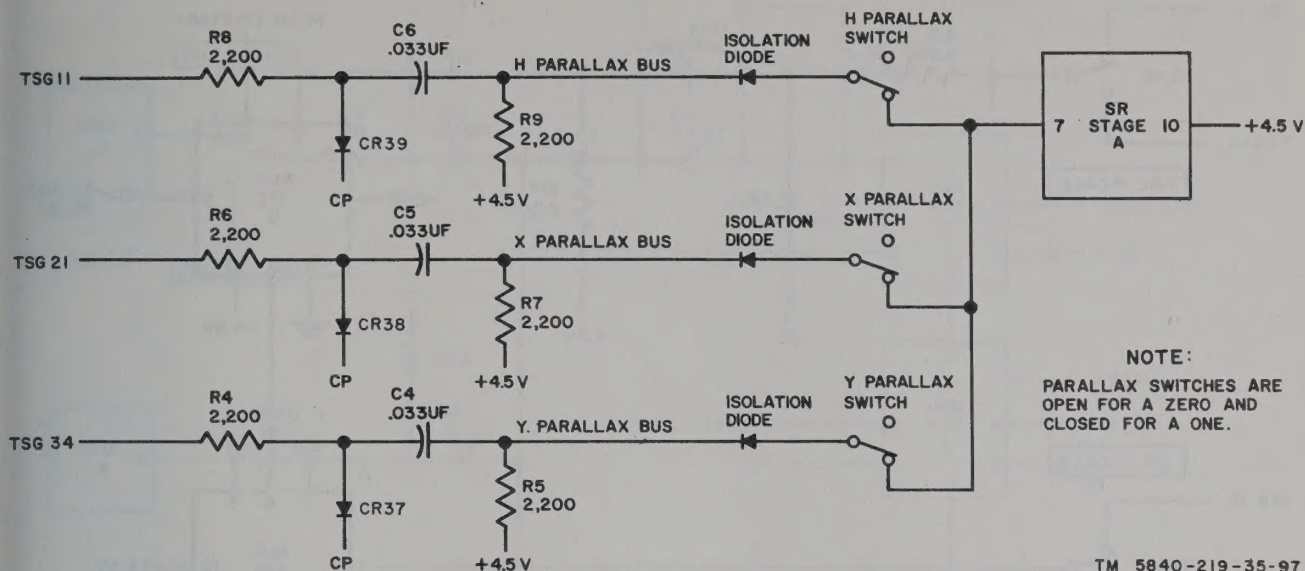


Figure 117. Receiver parallax read-in gates, simplified schematic.

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be reset prior to TS 11. This is done at the end of TS 10 for single scale operation (par. 178).

b. At TS 10, the gate bias is applied to terminal 5 of ALR F/O (par. 102i), which allows the clock pulse at the end of TS 10 to trigger ALR F/O. The positive output pulse from ALR F/O is applied to all ALU F/F's simultaneously at terminal 8 of each, thus turning them all OFF.

c. At TS 11, diode CR16 is enabled by the gate voltage applied through R16. This allows the clock pulse at the end of TS 11 to pass through CR16 and C13 to trigger ON all ALU's which have their gates at terminal 5 enabled by the associated SR stage.

177. Off Scale Detection Circuits

(fig. 119)

a. The AND gate which furnishes the all data present signal at time slot 51 is disabled by the off scale detection feature of the data processing section. If a coordinate is off scale, one or more of the last three of the 13 digits received for the X or Y coordinate is a ONE. At the end of TS 33, when the shift pulse control is disabled, the last 3 of the 13 digits of coordinate X are in SR stages 13, 12, and 11. Each of these SR stages is connected to one of three TCG's in the off scale detection circuit (fig. 119). These in turn are connected to the input of OSD F/O (par. 96s) through two gates: one, an external gate for the Y coordinate, and the other a gate within the

F/O for the X coordinate. If any one of the three SR stages is ON, a clock pulse is admitted to the F/O to trigger it at TS 34 for the X coordinate and at TS 47 for the Y coordinate. When the F/O is triggered, it turns OFF OSD F/F (par. 94n).

b. The OSD F/F is turned ON at TS 34 and remains ON at all times except when there is an off scale condition (if SR 13, SR 12, or SR 11 is ON). With the OSD F/F ON, the combination of its ON output and TSG 51 generates a gate voltage at the AND gate and transmits it to associated equipment for use as an all data present signal. However, if the OSD F/F is OFF, TSG 51 will not appear at the output of the AND gate, and no all data present signal will be transmitted.

c. Assume that SR 11 is ON due to a digit ONE being present in the eleventh place of the X coordinate. This is an off scale condition. The positive bias from SR 11 enables CR14 through R18, allowing clock pulses to pass through CR14 and C12 to terminal 2 of OSD F/O. During TS 34, the gate within the F/O is enabled and the F/O is triggered by the clock pulse at the end of TS 34. This turns OFF OSD F/F and prevents the generation of an all data present signal.

d. Assume that SR 13 is ON due to a digit ONE being present in the thirteenth place of the Y coordinate. This is also an off scale condition.

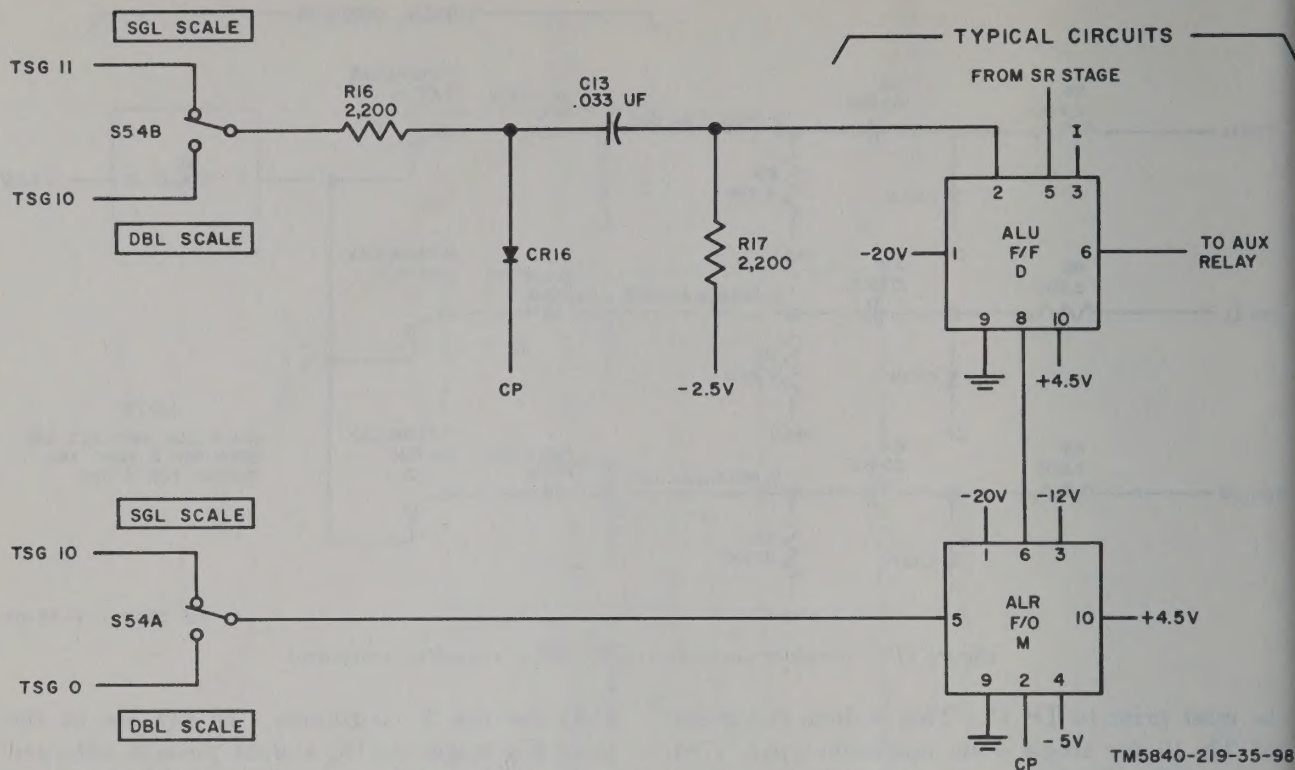


Figure 118. Auxiliary read-in and release gates, simplified schematic.

The positive bias from SR 13 (single scale operation, par. 178) enables CR15 through R19, allowing clock pulses to pass through CR15 and C13. At TS 47 CR13 is enabled, allowing the clock pulse at the end of TS 47 to pass through CR13 and C11 to trigger OSD F/O, and thus turn OFF OSD F/F.

e. Since the positive-going TSG 47 never exceeds about -2.5 volts in the positive direction, -2.5 volts is applied to the cathode of CR13 through R16 to make the potentials at both anode and cathode of CR13 the same during TSG 47.

f. Terminal 10 of OSD F/O is held at +4.5 volts; consequently, diode CR1, within the F/O, is held enabled by +4.5 volts applied to terminal 8 through R21. CR12 prevents the base of the transistor within the F/O from going more positive than +4.5 volts when the field of L1 within the F/O collapses.

178. Single Scale-Double Scale

a. This feature permits all stations to operate together on the same master grid whether the several stations are serving single or double scale local grid areas. All transmitters (par. 124) are arranged to send the same line code for a given

target within the same master grid area. The receivers, accepting coordinate data on the same target, must automatically interpret the target position identically, whether the transmitter or the receiver, or both, are using the single scale or double scale.

b. Since the *line* code transmitted is the same whether the transmitter is operating single scale or double scale, it is necessary at the receiver only to make such changes as are required to decode the line signals on a single or double scale basis. The required circuit changes are made by setting manually operated switches to either SGL SCALE or DBL SCALE in accordance with the size of the local grid being served at the local site, and by setting in parallax by means of the parallax switches.

c. Switching from single scale to double scale at the transmitter bypasses binary counter stage BC 1, starting the count of encoder pulses in BC 2 (par. 124); changing the parallax from single scale to double scale at the transmitter subtracts a ONE in the tenth digit from the single scale parallax. With these changes the code for each coordinate sent to the line is the same

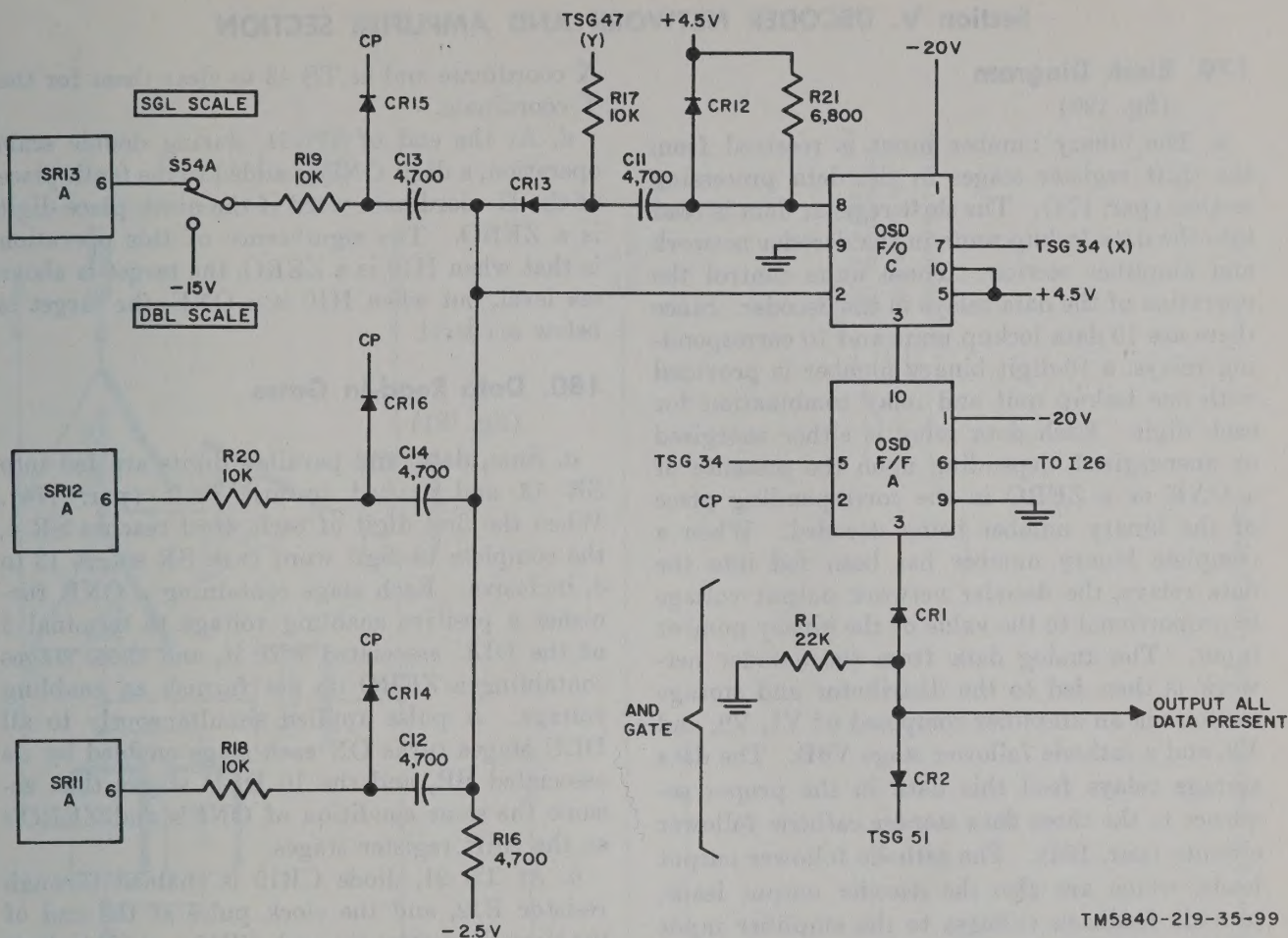


Figure 119. Off-scale detection circuits, simplified schematic.

whether the transmitter is operating single scale or double scale.

d. At the receiver the ring counters are started at TR 50 and UR 9 instead of TR 00 and UR 0, thus shifting the receiver digit selections one time slot *later* with respect to the time slots of the incoming frame, and triggers read-in of the auxiliary word one time slot *earlier* to compensate and leave the word unchanged. Figure 118 shows that the auxiliary lockup is released at TS 0 instead of TS 10 (since no time slots between TS 0 and TS 10 are generated), and the ALU F/F is turned ON at TSG 10 instead of TSG 11 when operating on double scale.

e. Since the digit ONE in the eleventh place of the H coordinate word was not transmitted,

it is replaced at the receiver as a ONE set in DLU 10 at TS 21.

f. Because the ring counters are started one time slot earlier during double scale operation, the first Y coordinate digit is in SR 13 at TS 34. Consequently, the off scale detection features for SR 13 is disabled by switch S54A (fig. 119) during double scale operation to avoid a false indication.

g. In addition to the preceding changes at the receiver, the height unknown pulse gate voltage is switched from TS 20 to TS 19 during double scale operation. Also, contacts on switch S54B are used for switching leads from the associated equipment ((1) fig. 172) to indicate that the receiver is operating in the double scale mode.

Section V. DECODER NETWORK AND AMPLIFIER SECTION

179. Block Diagram

(fig. 120)

a. The binary number input is received from the shift register stages in the data processing section (par. 174). The shift register data is read into the data lockup units in the decoder network and amplifier section. These units control the operation of the data relays in the decoder. Since there are 10 data lockup units and 10 corresponding relays, a 10-digit binary number is provided with one lockup unit and relay combination for each digit. Each data relay is either energized or unenergized, depending upon the presence of a ONE or a ZERO in the corresponding place of the binary number being decoded. When a complete binary number has been fed into the data relays, the decoder network output voltage is proportional to the value of the binary number input. The analog data from the decoder network is then fed to the distributor and storage section via an amplifier composed of V1, V2, and V3, and a cathode follower stage V6B. The data storage relays feed this data in the proper sequence to the three data storage cathode follower circuits (par. 192). The cathode follower output leads, which are also the decoder output leads, provide feedback voltages to the amplifier input circuit. These voltages are first combined in the proper sequence by the data storage relays in the distributor and storage section, and are then fed back to the amplifier input circuit through the feedback circuit included in the decoder network. Thus, variations in the multiplexing and storage circuits are compensated for by including these circuits in the amplifier feedback loop.

b. Feedback relay FR is controlled by lockups in the distributor and storage section, and connects the feedback voltage to the feedback network at appropriate times (par. 192).

c. The data lockups are controlled by two sets of TCG's and a reset F/O. At TS 21, TS 31, and TS 44 the DLU's are turned ON for the H, X, and Y coordinate data, respectively, by clock pulses transmitted through the data read-in gates. The DLU's are reset by the DLR F/O by a clock pulse admitted to it and at the end of TS 20 to clear them for the H coordinate, and by clock pulses transmitted through DLR control TCG's, triggering DLR to clear them at TS 30 for the

X coordinate and at TS 43 to clear them for the Y coordinate.

d. At the end of TS 21, during double scale operation, a digit ONE is added to the tenth place of the H coordinate word if the ninth place digit is a ZERO. The significance of this operation is that when H10 is a ZERO, the target is above sea level, but when H10 is a ONE, the target is below sea level.

180. Data Read-in Gates

(fig. 121)

a. Sum, data, and parallax digits are fed into SR 13 and shifted toward PSR (par. 174). When the first digit of each word reaches SR 4, the complete 10-digit word is in SR stages 13 to 4, inclusive. Each stage containing a ONE furnishes a positive enabling voltage to terminal 5 of the DLU associated with it, and those stages containing a ZERO do not furnish an enabling voltage. A pulse applied simultaneously to all DLU stages turns ON each stage enabled by its associated SR, and the 10 DLU stages then assume the same condition of ONE's and ZERO's as the shift register stages.

b. At TS 21, diode CR12 is enabled through resistor R12, and the clock pulse at the end of the time slot passes through CR12 and C9 to turn ON all DLU stages that were enabled by bias from the H coordinate word in SR stages 13 through 4. Each DLU stage thus turned ON energizes the relay connected to its output terminal 6, through -20 volts, and the combination of all the relay actions develops the analog voltage for the H coordinate as described in paragraph 183b.

c. At TS 31, diode CR10 is enabled through resistor R9, and the clock pulse at the end of the time slot passes through CR10 and C7 to trigger ON all the DLU's that were enabled by bias from the X coordinate word in the shift register.

d. At TS 44, diode CR9 is enabled through resistor R8, and the clock pulse at the end of the time slot passes through CR9 and C6 to trigger ON all the DLU's that were enabled by bias from the Y coordinate word in the shift register.

181. DLR Control Gates

(fig. 121)

a. The DLR control gates are used as a part of the reset function for data lockup release, and

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consist of two external gates and one gate within the DLR F/O (par. 102*h*). These gates reset the data lockups at the end of the Y, H, and X coordinate words in preparation for the new words.

b. At the end of TS 20, the gate within DLR F/O is enabled at terminal 5. This allows a clock pulse at terminal 2 to trigger the F/O to reset all DLU's, thus dropping out the Y coordinate word from the preceding frame in preparation for the new H coordinate word.

c. At the end of TS 30, diode CR4 is enabled through R3. This allows CR4 to pass a clock pulse through C2 to trigger DLR F/O and thus turn OFF all DLU's, dropping out the H word in preparation for the X coordinate word. CR1 is an isolation diode.

d. At the end of TS 43, diode CR3 is enabled and the clock pulse passes through C1, triggering DLR F/O, turning OFF all DLU's, and dropping out the X word in preparation for the Y coordinate word.

182. H Digit 10 Gate

(fig. 122)

During double scale operation a ONE is added to the tenth data digit of the H coordinate word if the ninth digit is a ZERO. With switch S54B in the DBL SCALE position, diode CR17 is enabled by TSG 21 allowing a clock pulse to pass through it and C14. If, at the same time DLU 9 input bias is negative, CR22 is enabled allowing the clock pulse to pass through it and C15 to turn ON DLU 10 at its terminal 7. With DLU 9 bias positive, the clock pulse cannot pass through CR22 to turn ON DLU 10.

183. Decoder Network

(fig. 123)

a. Although the voltage divider network, shown in figure 123 connected to terminals 8 through 19, is used to perform the actual decoding operation, the feedback resistance and the scale modification resistance are also included in the decoder network Z1, because all of these resistors are accurately matched to each other.

b. Terminal 8 is the output terminal of the voltage divider network and terminals 9 through 19 are the input terminals. When energized, the data relays apply the negative reference voltage to their associated network terminals; when unoperated, they apply the positive reference voltage.

age. When all data relays are unoperated, the open circuit output voltage of the network equals the positive reference voltage. When one of the relays is energized, the output voltage is more negative than the positive reference voltage by an amount dependent upon the particular relay involved. The amount of change in the output voltage produced by each relay is inversely proportional to 2^n , where n equals 1 for DR (data relay) 10, 2 for DR 9, 3 for DR 8, and so on. When all relays are energized, the open circuit output voltage is very nearly equal to the negative reference voltage. Since the binary number being decoded is fed to the data relays, the voltage divider output voltage is dependent upon the value of the binary number, and the voltage divider is called relay operated voltage divider (ROVD).

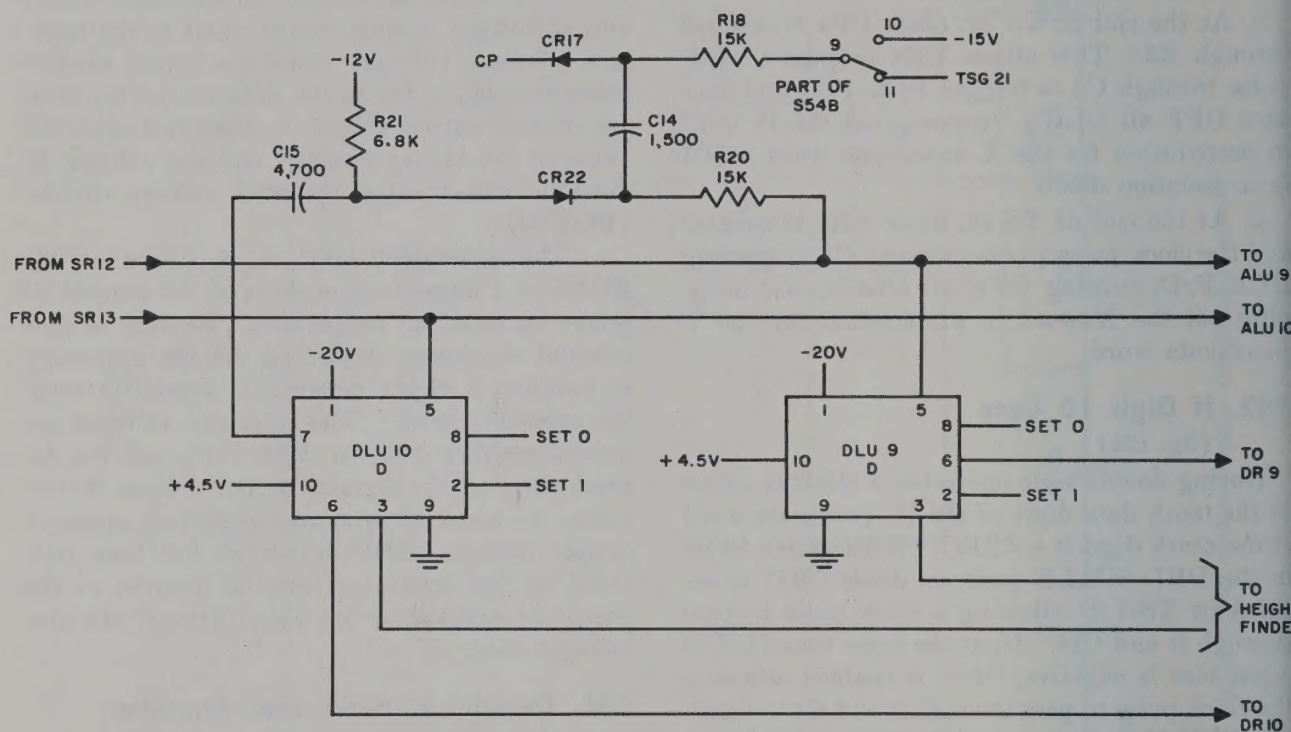
c. The equivalent internal resistance of the ROVD is 1 megohm regardless of the number of relays operated or unoperated. Because of this internal resistance, the actual voltage appearing at terminal 8 of the network is dependent upon the external circuit. The reference voltages are normally either ± 250 or ± 300 volts, and the desired range of the decoder output voltage is ± 50 volts. In order to produce the desired range of output voltages, REF switch S1 has been provided so that resistance may be inserted in the circuit to compensate for the different reference voltages used.

184. Decoder Network and Amplifier

(fig. 124)

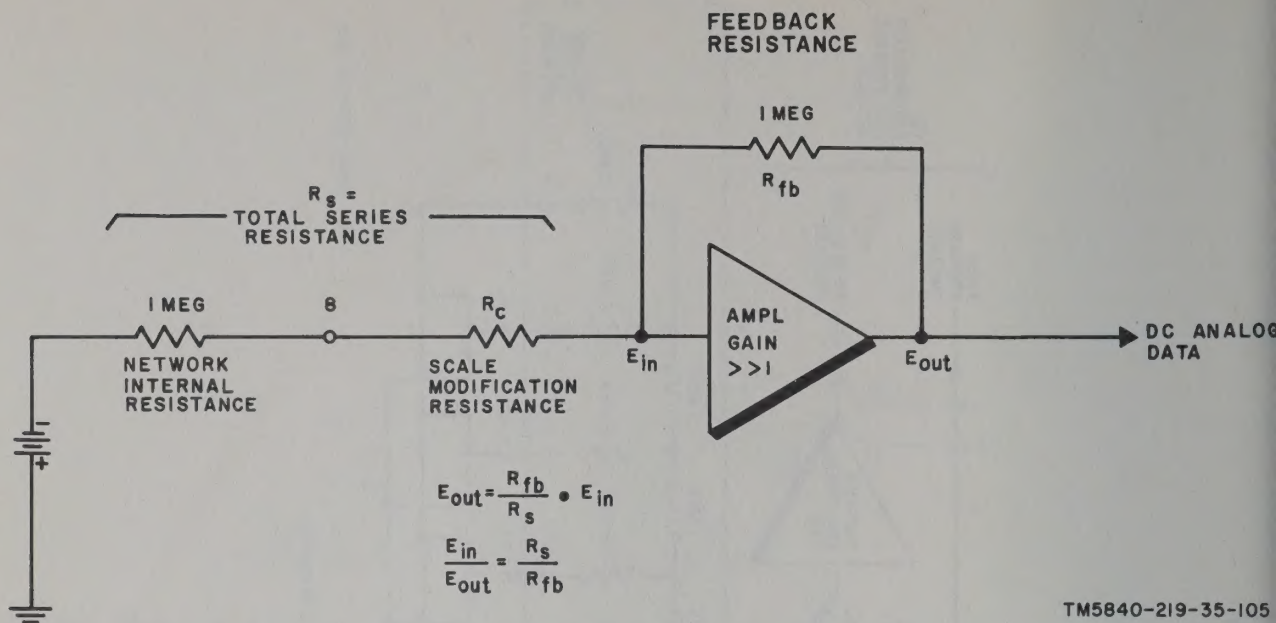
a. In the equivalent circuit of the decoder network and amplifier shown in figure 124, the amplifier output voltage, E_{out} , is equal to the open circuit output voltage of the ROVD, E_{in} , multiplied by the ratio of the feedback resistance, R_{fb} , to the total series resistance, R_s . The REF switch at the 250 position inserts a 4-megohm resistor in the circuit, causing R_s to be 5 megohms. Since R_{fb} is 1 megohm, the ratio of E_{in} to E_{out} is 5 to 1 under these conditions, and the range of decoder output voltages is ± 50 volts when the network open circuit voltage varies over a range of ± 250 volts.

b. The REF switch in the 300 position inserts a 5-megohm resistor in the circuit, causing R_s to be 6 megohms. Since R_{fb} is 1 megohm, the ratio of E_{in} to E_{out} is 6 to 1 under these conditions, and the range of decoder output voltages is ± 50



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Figure 122. H digit 10 gate, simplified schematic.



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Figure 124. Decoder network and amplifier, equivalent circuit.

volts when the network open circuit voltage varies over a range of ± 300 volts.

c. The earth curvature potentiometer R47 (fig. 123) is substituted for a fixed resistor in series with the feedback voltage when the contacts of the earth curvature relay K14 are closed. This potentiometer modifies the feedback voltage slightly to correct errors that would otherwise result from the curvature of the earth. Since the potentiometer is in series with the feedback resistance, its effect upon the decoder depends upon which REF switch position is used.

185. Decoder Amplifier

(fig. 125)

a. The amplifier used in the decoder is a three-stage dc amplifier with a gain of approximately 10,000. The first stage is a type 5755 dual triode connected as a difference amplifier. The signal input to this stage is to the grid of the left-hand section, and the signal output is taken from the plate of the left-hand section. The two cathodes are connected together and to a source of -300 volts through the 1-megohm cathode resistor. The resistor serves as a common coupling element between the two halves of the tube. The right-hand half of the tube is used to zero set the amplifier and thus compensate for unavoidable drifts in the output voltage. This section of the tube also compensates for random emission effects

in the left half of the tube, because such effects tend to be common to both cathodes and cancel out. The normal signal input to the left-hand section is amplified in the usual manner. Since a change in the plate current through the right half of the tube causes a change in the total current through the common cathode resistor, which in turn, varies the grid-to-cathode potential of the left half, ZERO SET control R6 may be used to adjust the zero set of the amplifier.

b. Provisions have been made to use an external automatic zero set (AZS) circuit (par. 133) with this amplifier. The operation of the AZS circuit is based upon the fact that when the amplifier output level changes because of amplifier drift, the input voltage also changes as a result of the feedback circuit. Thus, the average value of the input voltage may be used as a measure of the amount of amplifier drift or error. The AZS circuit receives its input from the grid of the left-hand half of the first stage of the amplifier through isolating resistor R46. The output of the AZS circuit is fed to the grid of the right section of the same tube in such a manner as to reduce the error voltage to zero.

c. When no AZS circuit is provided, the correction input voltage lead to the difference amplifier must be grounded. Under these circumstances, the error signal lead is left floating.

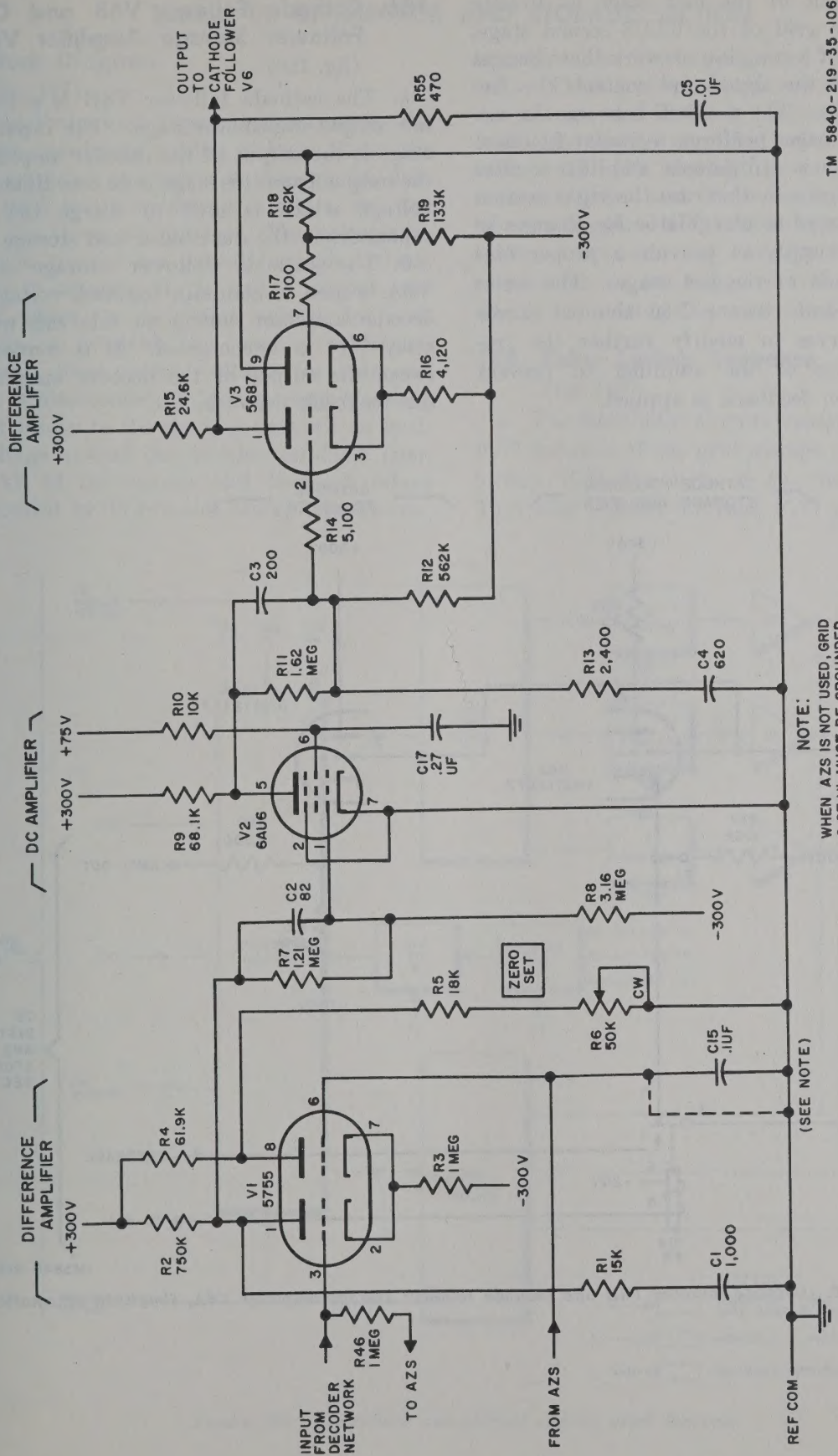


Figure 125. Decoder amplifier, schematic.

d. The output of the first stage is directly coupled to the grid of the 6AU6 second stage, V2, by means of a coupling network that changes the dc level of the signal and controls the frequency response. The network between the second and third stages performs a similar function. The third stage is a difference amplifier similar to the first stage. In this case the right section of the tube is used as a regulator for changes in the -300-volt supply to provide a proper bias for the left side of the last stage. The series capacitor C5 and resistor R55 shunted across the output serves to modify further the frequency response of the amplifier to prevent instability when feedback is applied.

186. Cathode Follower V6B and Cathode Follower Storage Amplifier V6A

(fig. 126)

a. The cathode follower V6B is a low gain, low output-impedance stage. The input to this stage is the output of the decoder amplifier, and the output from this stage is dc coordinate analog voltage which is used to charge the storage capacitors in the distributor and storage section.

b. The cathode follower storage amplifier V6A is used to maintain feedback voltage to the decoder amplifier during the intervals when FR relay K19 is de-energized. It is connected between the output of the decoder amplifier and the feedback network.

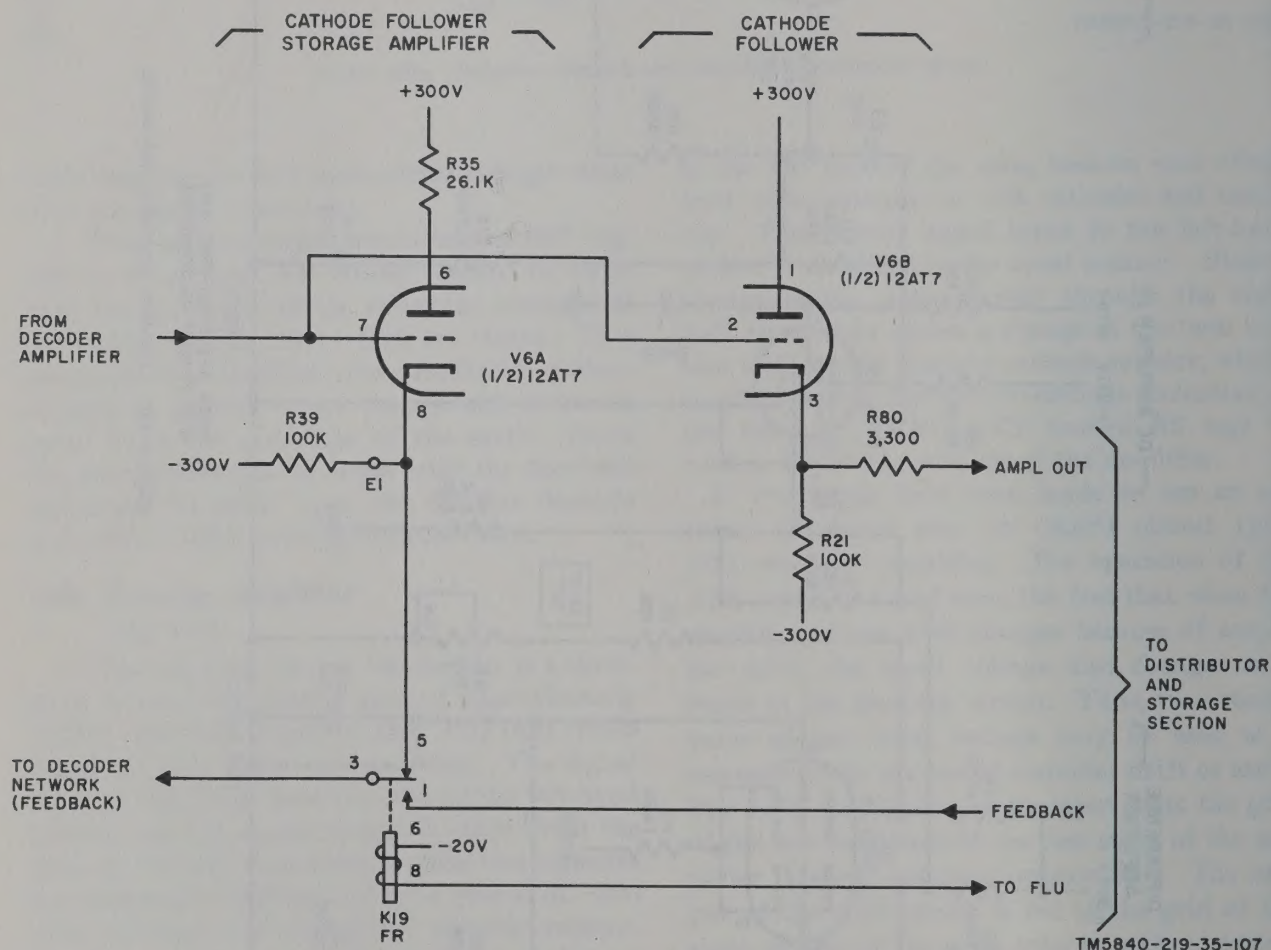


Figure 126. Cathode follower V6B and cathode follower storage amplifier V6A, simplified schematic.

Section VI. DISTRIBUTOR AND STORAGE SECTION

187. Block Diagram

(fig. 127)

The distributor and storage sections accept the sequential coordinate analog voltage from the decoder amplifier and pass it through the data storage grid relays to storage circuits, one for each of the three coordinates. The voltages in the storage circuits are passed through cathode followers to separate H, X, and Y output connections, where the dc analog voltage for each coordinate is available for use by associated equipment. The output voltage for each coordinate is also connected back through the data feedback relays to the decoder network as feedback voltage around the decoder amplifier (par. 183). All of the storage and feedback relays are controlled by TCG's and lockup circuits con-

tained in the block designated distributor circuits. These lockup circuits are timed to release the storage and feedback connections to the decoder data storage amplifier before the data relay lockups (DLU), storing the preceding coordinates, are reset, and the reference protection relays are triggered ON. All storage relay lockups remain reset, and the two for the succeeding coordinates are not triggered ON until after the DLU's are storing the next coordinate.

188. Relay Lockup Sequence

(fig. 128)

a. The distributor circuits consist of one lockup F/F for each of the grid storage relays, and one lockup F/F for each of the feedback relays. They also contain the reset F/O (SLR) and its

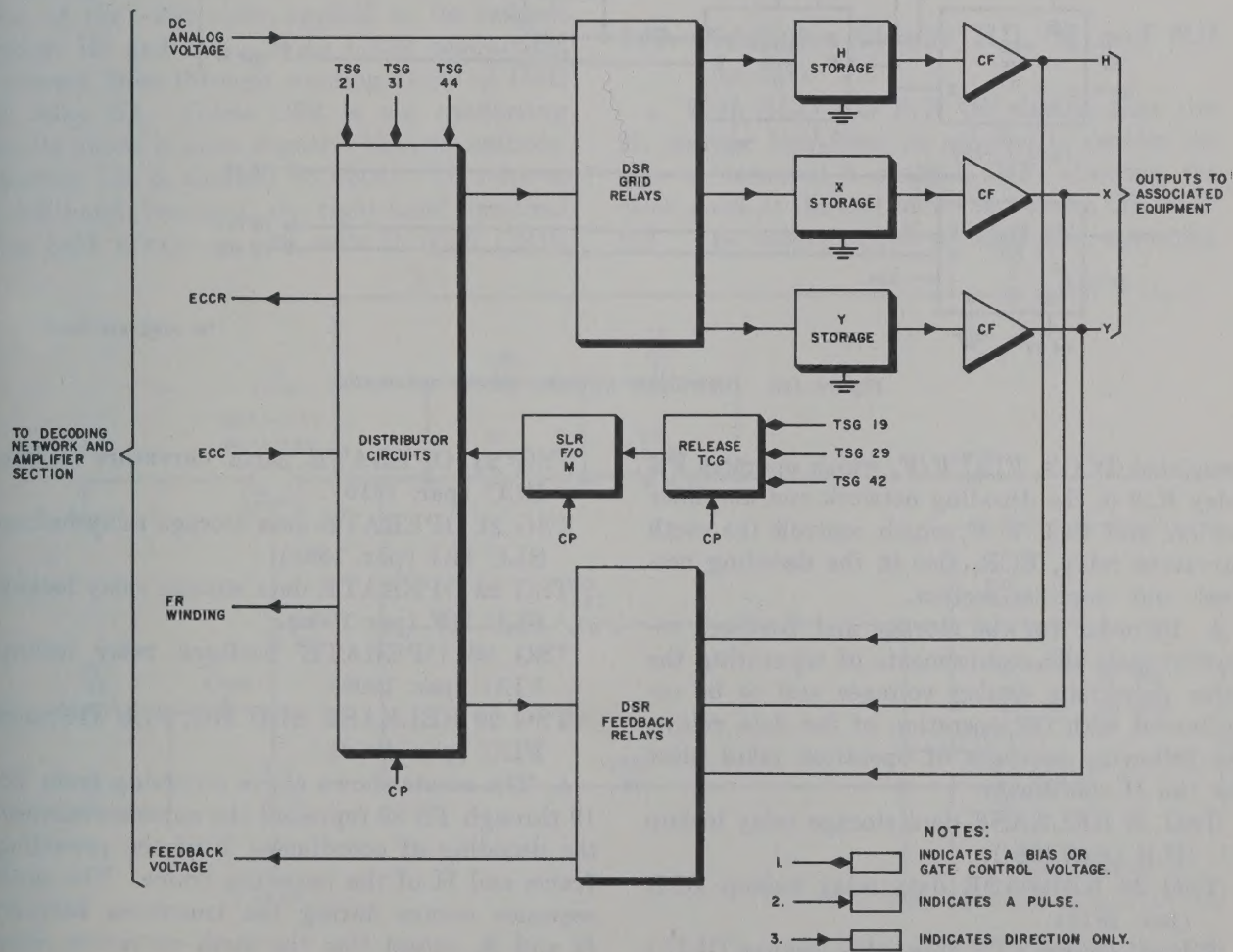


Figure 127. Distributor and storage section, block diagram.

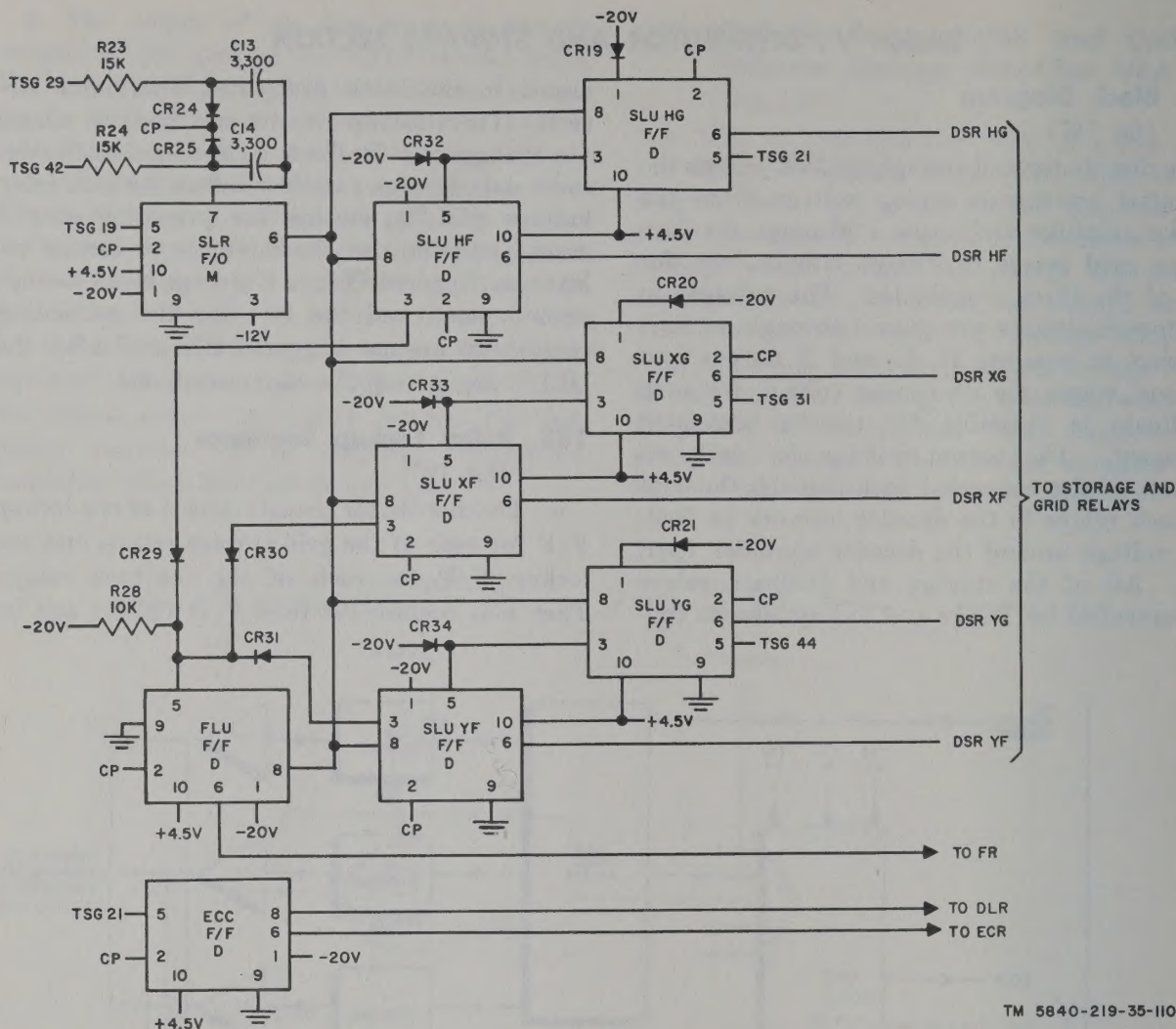


Figure 128. Distributor circuits, partial schematic.

associated TCG's, FLU F/F, which operates FR relay K19 in the decoding network and amplifier section, and ECC F/F, which controls the earth curvature relay, ECR, also in the decoding network and amplifier section.

b. In order for the storage and feedback relays to meet the requirements of separating the three coordinate analog voltages and to be coordinated with the operation of the data relays, the following sequence of operation takes place for the H coordinate:

TSG 19 RELEASE data storage relay lockup SLR (par. 192c).

TSG 20 RELEASE data relay lockup DLR (par. 181b).

TSG 21 OPERATE data relay lockups DLU 1 to 10 (par. 180b).

TSG 21 OPERATE earth curvature lockup ECC (par. 191b).

TSG 21 OPERATE data storage relay lockup SLU HG (par. 189b).

TSG 22 OPERATE data storage relay lockup SLU HF (par. 190a).

TSG 23 OPERATE feedback relay lockup FLU (par. 190b).

TSG 29 RELEASE SLU HG, SLU HF, and FLU (par. 191d).

c. The events shown above occurring from TS 19 through TS 29 represent the sequence between the decoding of coordinates Y of the preceding frame and H of the incoming frame. The same sequence occurs during the transition between H and X, except that the earth curvature relay lockup is released at time slot 30 (on completion

of decoding coordinate H) and is not operated again until the succeeding frame.

189. Distributor Circuits, SLU HG (fig. 129)

a. At time slot 19 the gate at terminal 5 of SLR F/O (par. 102j) is opened and the clock pulse at the end of TS 19 triggers SLR F/O. The positive output pulse at its terminal 6 is applied to all SLU's (par. 97h) and FLU (par. 97i), turning OFF SLU YG, SLU YF, and FLU, and releasing FR and the grid and feedback relays of the Y coordinate of the preceding frame.

b. At TS 21 the gate at terminal 5 of SLU HG is enabled, and the clock pulse at the end of the time slot passes through the gate to the base of the transistor. While the SLU HG F/F is OFF, the potential at the collector is approximately -17 volts (fig. 129). Diode CR19 is conducting, and diode CR32 is conducting because of the -300 volts applied to its cathode through R3 and R41. With CR32 conducting, no current flows through winding 11-13 of DSR HG relay K1. Diode CR3 is not conducting since its anode is more negative than its cathode. Capacitor C2 is charged to about -17 volts at its left-hand terminal, its right-hand terminal being held always at -20 volts through CR19.

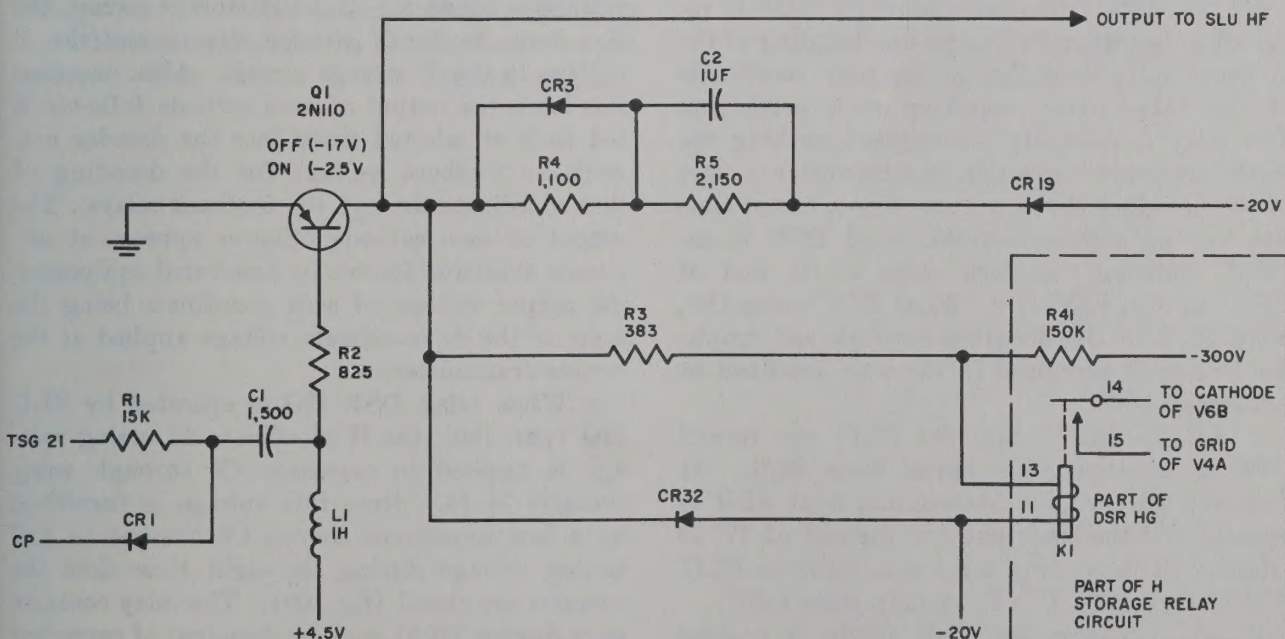
Upon the application of the clock pulse to the base of Q1, the transistor is turned ON, dropping the collector voltage to about -2.5 volts in the time it takes to charge C2 through the combined resistance of the associated circuits.

c. When the collector voltage drops to the point where the potential at the cathode of CR32 is less than -20 volts (about $\frac{1}{5}$ of a time slot), diode CR32 no longer conducts, and current flows through the winding of DSR HG to -20 volts, energizing the relay and closing contacts 14-15.

d. When SLU HG is turned OFF (par. 191d), the voltage at the collector rises toward -20 volts and CR3 is enabled, shorting out R4 until C2 has charged to about -17 volts at its left-hand terminal. The charging time of C2 is shortened by the action of CR3. Diode CR19 is in the circuit to prevent transients from getting back into the -20-volt supply when the circuit is turned OFF.

190. Distributor Circuits SLU HF and FLU (fig. 128)

a. With SLU HG F/F ON during time slot 22, positive bias from its terminal 3 enables the gate at terminal 5 of SLU HF, allowing the clock pulse at the end of TS 22 to turn ON SLU HF. The output circuit of SLU HF, operating



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Figure 129. Storage lockup SLU HG, partial schematic.

the feedback relay, functions in exactly the same way as that of SLU HG described in paragraph 189*b*. The output of SLU HF terminal 3 is a positive-going pulse and is applied to diode CR29 during time slot 23.

b. Diode CR29 is held in its nonconducting state when SLU HF is OFF. With SLU HF ON, CR29 is enabled, and the positive output from SLU HG enables the gate of FLU at its terminal 5 and allows the next clock pulse to pass through to turn FLU ON. With FLU ON, relay FR (K19) is operated in exactly the same way as described in paragraph 189*b*.

191. Distributor Circuits SLU XG, SLU XF, SLU YG, SLU YF, ECC, and SLR (fig. 128)

a. The circuits of the remaining storage lock-ups function exactly as do those described in paragraphs 189 and 190, except that SLU XG is turned ON at the end of TS 31, SLU XF is turned ON at the end of TS 32, SLU YF is turned ON at the end of TS 44, and SLU YG is turned ON at the end of TS 45. FLU, likewise, is turned ON by the clock pulse passing through the gate enabled by the output of SLU XF at the end of TS 33, and again by the clock pulse passing through the gate enabled by the output of SLU YF at the end of TS 46.

b. The earth curvature correction relay is required to operate only during the decoding of the H coordinate, since this is the only coordinate of the three never requiring such correction. The relay is normally unenergized, making the earth curvature correction potentiometer a part of the decoding network (par. 184*c*), but at time slot 21, the gate at terminal 5 of ECC is enabled, allowing the clock pulse at the end of TS 21 to turn ECC ON. When ECC comes ON, relay ECR in the decoding network and amplifier section is energized in the way described in paragraph 189*b*.

c. All the SLU's and the FLU, are turned OFF by positive-going pulses from SLR. At time slot 19 the gate at terminal 5 of SLR is enabled and the clock pulse at the end of TS 19 triggers SLR, sending a set zero pulse to FLU, SLU YG, and SLU YF, turning them OFF.

d. At time slot 29, diode CR24 is enabled through R23, allowing the clock pulse at the end of TS 29 to pass through CR24 and C13 to

trigger SLR at its terminal 7. This sends a set zero pulse to FLU, SLU HG, and SLU HF, turning them OFF.

e. At time slot 42, diode CR25 is enabled through R24, allowing the clock pulse at the end of TS 42 to pass through CR25 and C14 to trigger SLR at its terminal 7. This sends a set zero pulse to FLU, SLU XG, and SLU XF, turning them OFF.

192. Storage Circuits and Cathode Follower Outputs (fig. 130)

a. The storage circuit and cathode follower for the H coordinate is shown in figure 145. The equivalent circuits for the X and Y coordinates are not shown, but their operation is identical to that of the H coordinate. The purpose of this circuit is to store the H coordinate dc analog voltage while the receiver is decoding the X and Y coordinates, thus providing a constant dc voltage for the H coordinate during the entire frame.

b. The output from the decoder is fed to the grid relays of the storage circuit at all times so that the H, X, and Y dc analog voltage appears sequentially on all three grid relays. These relays are operated at selected times (par. 190 and 191) so that only the H coordinate dc analog voltage is connected to the H storage circuit, the X voltage to the X storage circuit, and the Y voltage to the Y storage circuit. Also, one time slot later, the output of each cathode follower is fed back at selected times into the decoder network as feedback voltage for the decoding of that coordinate through the feedback relays. The output of each cathode follower appears at terminals available for use by associated equipment, the output voltage of each coordinate being the same as the dc coordinate voltage applied at the remote transmitter.

c. When relay DSR HG is operated by SLU HG (par. 189), the H coordinate dc analog voltage is applied to capacitor C6 through relay contacts 14-15. Since this voltage is furnished by a low impedance source, C6 charges to full analog voltage during the eight time slots the contacts are closed (fig. 109). The relay contacts open during TS 31, and one terminal of capacitor C6 is connected only to the grid of V4A. Since the grid is an extremely high impedance circuit,

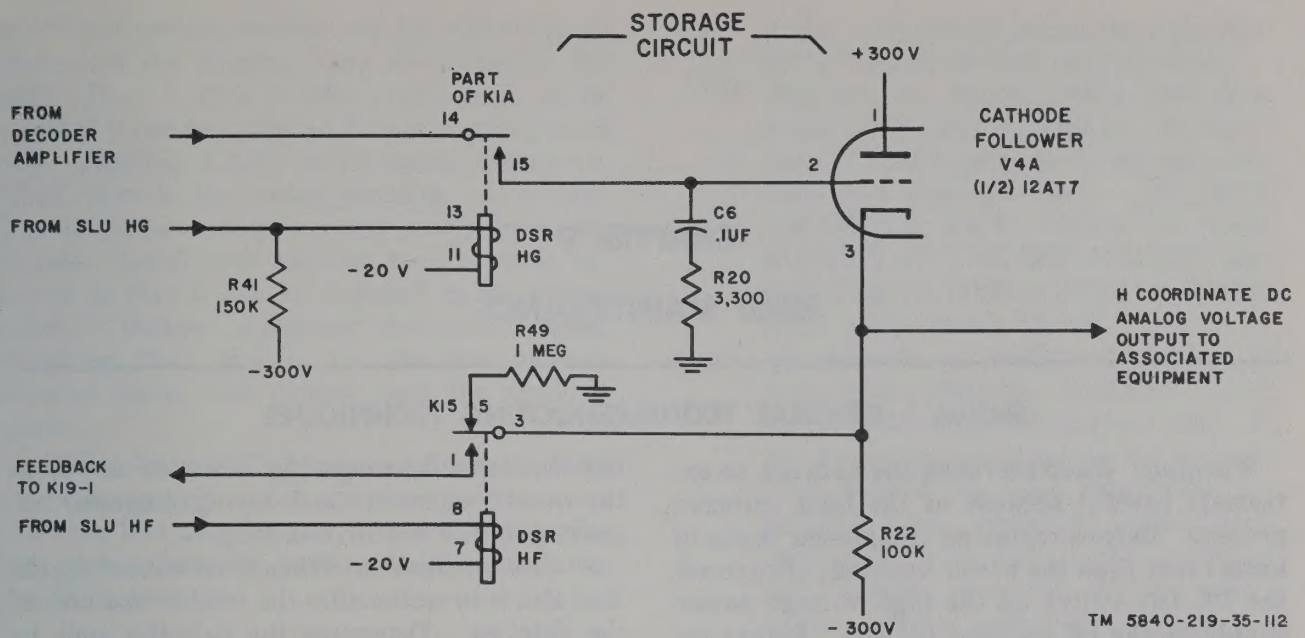


Figure 130. Storage circuit and cathode follower (H coordinate), schematic.

there is no discharge path for C6, and it maintains the grid at the dc analog voltage to which the capacitor had been charged.

d. Cathode follower V4A is conventional. Bias, proportional to the dc analog voltage from the decoder amplifier, is applied while relay DSR HG contacts are closed, and is maintained during encoding of the other two coordinates by the charge on C6. The voltage developed across cathode resistor R22 is the H coordinate output voltage. This voltage is also applied to relay

DSR HF and is sent to the decoder network through contacts 1-3 when the relay is energized (par. 190). When the relay is unenergized, the decoder network circuit is terminated in R49 (1 megohm) through contacts 3-5.

Figure 131. Receiver, block diagram.
(Contained in separate envelope)

Figure 132. Receiver, timing diagram.
(Contained in separate envelope)

CHAPTER 9

FIELD MAINTENANCE

Section I. GENERAL TROUBLESHOOTING TECHNIQUES

Warning: When servicing the data set, be extremely careful because of the high voltages present. Before replacing component parts in units other than the power supplies, always set the DC ON switch on the high voltage power supply at the off position (down). Before replacing component parts in either of the power supplies, always disconnect the 115 volts ac at the source.

193. Extent of Instructions

Troubleshooting at a field maintenance level includes the techniques given in paragraphs 195 and 196 and any other techniques that may be required to isolate a defective part. The systematic troubleshooting procedure begins with the Performance and Trouble Location Checklist (par. 199) which covers all functions of the data set. Paragraph 200 lists the circuits having common functions which appear at various parts of the data set. Paragraphs 201 through 204 provide procedures for testing transistors, diodes, and packages. Paragraphs 205 through 210 cover additional troubleshooting information not included in the other paragraphs.

194. Troubleshooting Techniques

a. General. To be effective, troubleshooting must be systematic. It is seldom possible to observe a trouble symptom and diagnose the cause immediately. Generally it will be necessary to perform a sequence of operational checks, observations, and measurements before the fault can be located. If the proper sequence is employed, the trouble will be traced first to a unit, then to a portion of a unit, and finally to the defective part. The sequence of steps is referred to commonly as the sectionalization, localization, and isolation of trouble. Full use should be made of

the functional drawings (fig. 202–208) as well as the overall schematic and wiring diagrams appearing at the end of this chapter.

b. Sectionalization. When troubleshooting, the first aim is to sectionalize the trouble to a unit of the data set. Determine the defective unit by observing the operation of the indicator lamps on the panels. Tests are outlined in paragraph 48.

c. Localization. After determining the defective unit, make additional checks and measurements to localize the trouble to a portion, or package, of the unit. As in the case of sectionalization, use inspection, observation of the indicator lamps, and the performance checklist in paragraph 199.

d. Isolation. After trouble has been localized to a portion of a unit, for example to a package, use the troubleshooting technique described in paragraphs 203 and 204. Use paragraph 213 to find the physical location of parts of the units.

Note. When instructions call for terminating the transmitter or receiver properly, disconnect the connecting line and substitute a 600-ohm, ½-watt terminating resistor for the line. In the event reference or target circuits are used as a part of the testing procedure, remove the external circuits first unless otherwise specified. Never ground a reference or target voltage line while it is still connected to an external source or voltage. The terminal numbers for all external wiring will be found on the interconnecting schematic drawing (fig. 162).

195. Removal Instructions for Plug-in Parts

a. Fuses. To remove a fuse from the power supplies, push the fuse cap in and turn it in the direction indicated by the arrow on the cap. Pull out the cap and fuse.

b. Electron Tubes. To remove electron tubes from the equipment, first remove the tube covers or loosen the spring clamps. When tubes have

cooled sufficiently, remove them by pulling up on them with the fingers. Grip the tubes by the base. Do not rock a tube or jiggle it in its socket if it can be extracted by a straight upward pull. Jiggling a tube in its socket during removal spreads the socket contacts. If a tube does not release easily, move it *gently* from side to side. Label each tube as soon as it is removed so that it can be replaced in its proper socket. Before replacing miniature tubes, straighten their pins in the pin straighteners mounted inside each cabinet near the terminal boards.

c. *Pilot Lamps.* To remove a pilot lamp from the power supply panels in either cabinet, unscrew the lens covering the lamp and remove the bayonet-base lamp by pushing it in and turning it counterclockwise.

196. Electron Tube Replacement Technique

When trouble occurs, make the inspection given in paragraph 47. If tube failure is suspected, check and replace tubes as follows:

a. Using Electron Tube Test Set.

- (1) Remove and test *one* tube at a time. If it is necessary to remove more than one tube at a time, label each one so that it can be replaced, if satisfactory, in its original socket.
- (2) Replace a tube only when a defect is obvious, such as broken glass envelope, open filament, or a broken connecting prong or lead; or when a test in a tube tester or other equipment shows the tube to be defective.
- (3) Do not discard a tube because it tests *on or near* the minimum test limit of the tube tester. Some new tubes test near the low end of the acceptability range of the tube specification. These tubes may provide satisfactory service over a long period of time.
- (4) Do not discard a tube merely because it has been in use for a specified length of time. *Satisfactory operation in a circuit is the final proof of tube quality.*

b. Tube Substitution Method.

- (1) Replace the suspected tubes, *one* at a time, with new tubes. Note the sockets from which the original tubes were re-

moved. If the equipment becomes operative, discard the last tube removed.

- (2) Reinsert the original tubes, one at a time, in the original sockets. If equipment failure occurs during this step, discard the original tube. **DO NOT LEAVE A NEW TUBE IN THE SOCKET IF THE EQUIPMENT OPERATES SATISFACTORILY WITH THE ORIGINAL TUBE.**
- (3) If there is an insufficient number of spare tubes available, substitute a new tube for the suspected original tube. If the equipment continues to be inoperative, replace the new tube with the original tube. Similarly, check each original tube, in turn, until the equipment becomes operative. If tube substitution does not correct the trouble, *reinsert the original tubes in the original sockets* before forwarding the defective equipment to a higher echelon for repair.
- (4) Retain any removed tube until its condition can be checked in a tube tester.

197. Test Equipment Required

The test equipment required for troubleshooting the data set is listed below. A common usage name is indicated after each component. If the technical manual is not specified, refer to the literature packed with the equipment.

Nomenclature	Common name	Technical manual
Oscilloscope AN/USM-81-----	Oscilloscope.	
Oscilloscope AN/USM-89-----	Oscilloscope.	
Multimeter AN/URM-105----	Multimeter.	
Voltmeter, Electronic, AN/USM-98.	Differential voltmeter.	
Multimeter, Electronic TS-505/U.	VTVM (dc)	TM 11-5511.
Voltmeter, ME-30A/U-----	VTVM (ac)	TM 11-5132.
Frequency Meter, AN/TSM-16.	Frequency meter.	
Resistance Bridge ZM-4/U----	Resistance bridge.	
Test Set, Electron Tube TV-7/U.	Tube tester--	TM 11-2661.
Test Set, Electron Tube TV-2/U.	Tube tester--	TM 11-5083.
Tool Kit, TK-100/MSQ-18----	Tool kit.	
Test Facilities Kit (consists of cable extensions, patch cordage, and package test adapters).	Test facilities kit.	

Section II. TROUBLE LOCATION

Warning: When servicing the data set, be extremely careful because of the high voltages present. Before working on units other than the power supplies, always set the DC ON switch on the high voltage power supply at the off position (down). Before working on either of the power supplies, always disconnect the 115 volts ac at the source.

198. Use of Performance and Trouble Location Checklist

a. General. The performance and trouble location checklist, table VII, describes the procedure for checking the performance of every functional section of the data set and indicates the probable location of trouble. This table may be used as a periodic performance test, or as a trouble location procedure, or both. The maintenance manual for the system in which the AN/TSQ-36 is being used, will sectionalize trouble to the receiver or transmitter function. After checking the power supplies for proper outputs, proceed to the steps given for the applicable function. Each step of the test in the table is numbered and is listed in table VI immediately preceding table VII for quick reference. Unless otherwise directed, preset all operational controls as specified in table III.

b. Checking Procedure. The checking procedures described in table VII are based on test facilities which have been built into the equipment, and on the use of the test equipment listed in paragraph 197. The built-in test facilities include provisions for single-step (static) time slot advance, and neon indicator lamps for all important bistable circuits. When these facilities are used, each programming operation may be observed, first on a static basis (observe F/F circuits coming ON and OFF).

Note. The digital circuits may be stopped without danger of overloading the encoder only if care is taken not to stop the encoder while it is in the process of sweeping. This process occurs during the following time slots: 6 to 15, 18 to 27, and 30 to 39, inclusive. Stopping the equipment on any of these time slots requires a period of delay while the encoder recovers from the overload. During tests which do not involve the encoder, switch S1 on the encoder panel (fig. 14) can be set at ADJ. If this is done, the program generator section can be stopped at any time slot desired.

Second, on a dynamic basis, the dynamic test duplicates actual operating conditions and thus tests gates and other functional circuits for marginal operation. For example, a gate having an excessively long charging rate (possibly because of high series resistance) may appear to function properly in single step operation, but will prove defective under dynamic conditions.

c. Probable Location of Fault. If any of the tests in table VII reveals faulty operation of the data set, use the final column, Probable Location of Fault. Terminals of jacks referred to in the table are generally accessible from the wiring side of the chassis. In the few cases where they are not accessible, use the appropriate adapter (fig. 161) (large or small) provided in the test facilities kit. To use the adapter, remove the package to be checked and replace it with the adapter. Plug the package into the adapter. All terminals are then available for testing.

Caution: Use great care when applying the test probe to a jack terminal. If the probe accidentally shorts adjacent active terminals, it is probable that the transistor in the package associated with that jack will be damaged. Use insulated probes when checking package and jack terminals where terminals are close together to avoid accidental shorts.

Voltages appearing at the terminals are shown on the schematic diagram of the unit containing the package. Waveforms of the voltages on the active terminals of the packages are shown in figure 159.

d. Waveforms (fig. 159). Waveforms of the voltages appearing at terminals of the packages and of other important points of the data set are shown in figures 182(1) through 182(12). The waveforms illustrated are representative of typical circuits, but every waveform of every terminal of the packages is not shown. For example, a representative D package showing the output waveform for a typical package is shown, and it is understood that all other D packages having the same external circuits will have the same waveforms at the corresponding terminals. When checking a waveform at a terminal of a package not shown in the figure, refer to the package of

the same kind which is shown, and use the representative waveform illustrated.

e. Checking Clock Pulses. In all cases when checking for the presence of clock pulses in circuits where only one CP appears at the time the circuit is recycled, or stepped (for example, when the PC switch is at the test position), use the following procedure: Set the PC switch to normal and check for continuous clock pulses at the point specified for the test. If clock pulses are present, it is not necessary to make further tests of the clock pulse circuits.

f. Further Troubleshooting. Additional troubleshooting of circuits referred to in table VII, but not described fully in the table, are found in paragraphs immediately following the table. These include common circuit troubleshooting, diode, transistor, and package troubleshooting, and troubleshooting the encoder, decoder, and power supplies. For troubleshooting indicator lamp circuits, see paragraph 203g.

g. Abbreviations. For simplicity, abbreviations are used in table VII for some of the most common terms. These, and their meanings are listed below:

Abbreviation	Meaning
Sel.....	Units and tens ring switches.
TS.....	Time slot.
Step.....	Press single-pulse (SP) button.
Recycle.....	Press recycle button.
ON.....	Associated neon lamp glows (circuit ON, or equivalent to 1).
OFF.....	Associated neon lamp extinguished (circuit OFF, or equivalent to 0).
BC.....	Binary counter.
SR.....	Shift register.
Aux.....	Auxiliary.
UR.....	Units ring.
TR.....	Tens ring.

199. Performance and Trouble Location Checklist

Table VI is an index of the material found in table VII. It is provided to facilitate the use of

table VII as a trouble location guide. It lists the functions and test numbers for that table.

Table VI. Index for Table VII

Function	Step No.
Power supply:	
Power supplies	1
High voltage power supply	2, 5
Filament supply	3
Low voltage power supply	4
Lamp supply voltage	6
Test panel	7
Transmitter:	
Initial set up	8
Clock pulses and set zero pulses	9
Units ring (UR) and tens ring (TR)	10
Recycle test circuit	11
Encoder start and reset pulses	12
Ready tone control	13
Parallax read-in	14
BC reset	15
Shift register	16
Auxiliary data read-in	17
Data read-in	18
Coordinate and earth curvature relay lockups	19
Coordinate data relays	20
Overall digital	21
Encoder and binary counter	22
Modulator	23
Receiver:	
Clock pulse and set zero pulse	24
Manual start	25
Units and tens rings	26
Recycle test circuit	27
Shift register	28
Shift pulse disable	29
Carry storage	30
Serial adder	31
Aux lockups	32
Data lockups	33
Off-scale detection	34
All data present	35
Storage lockups	36
Double scale operation (using oscilloscope)	37
Double scale operation (without oscilloscope)	38
Decoder	39
Amplifier synchronizer	40
Overall analog check	41
Automatic zero set	42
Remote start	43

Table VII. Performance and Trouble Location Checklist

POWER SUPPLIES

Step	Function	Procedure	Normal indication	Probable location of fault
1	Power supplies.	Caution: Always set ENC REF and DEC REF switches at OFF before turning off and turning on the data set. Set the high voltage power supply AC ON and DC ON switches at off (down) and the low voltage power supply +4.5V & -20V SUP switch at off (down).	All indicating lamps go out.	Check AC ON switch S2.
2	High voltage power supply.	Measure the voltage at convenience receptacles J1.	The VTVM (ac) reads 115 volts ac.	Check fuse F1 7A. Check the external supply voltage.
3	Filament supply.	Set the AC ON switch on the high voltage power supply at on (up).	EQUIP POWER and POWER SUPPLY lamps light; all power supply tube filaments light.	a. If both lamps fail to light, check AC ON switch S2. If the POWER SUPPLY lamp fails to light and all tubes in the high voltage power supply fail to glow, check fuse F2 3A. If any tube filaments fail to glow, replace the tube. If all tubes fail to glow and the POWER SUPPLY lamp is on, check transformer T2 (fig. 134). b. If the tubes of the decoder, encoder, automatic zero set, and amplifier synchronizer fail to glow, the low voltage power supply may be faulty. Check fuses as indicated by glowing neon lamp. Check for 6.3 volts ac between terminals C-D, E-F, H-J, and R-S of J2 (fig. 152). (The actual output is $6.5 \pm .5$ volts.) If no voltage exists at these terminals, check F4.
4	Low voltage power supply.	Set +4.5V & -20V SUP switch at on (up). Check voltage at +4.5V test point J7 and GRD test point J3. Check voltage between +20V test point J6 and -20V test point J5.	a. +4.5V & -20V PWR ON lamp lights. b. Meter indicates that 4.5 volts dc is present. c. Meter indicates that 20 volts dc is present.	a. Check for open fuses (F1, F2, and F3) as indicated by associated neon lamp. b. Check fuse and fuse lamp F2. Check CR1 and associated circuitry (fig. 152). c. Check fuse and fuse lamp F3. Check CR2 and associated circuitry. If the meter indicates that +4.5 and -20 volts are present and the +4.5V & -20V PWR ON lamp does not light, check relay K1 (fig. 152).

Table VII. Performance and Trouble Location Checklist—Continued

POWER SUPPLIES—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
5	High voltage power supply.	Set DC ON switch at ON (up).	a. +300 DS3 and -300 DS4 lamps light after a delay of about 45 seconds.	a. If neither lamp lights, check fuse F3 5A and/or time delay relay K1. If the +300 lamp lights and the -300 lamp does not, check fuse F7, tubes V11 and V12, and associated circuitry (fig. 134). If the -300 lamp lights and the +300 lamp does not, check fuse F6, tubes V9 and V10, and associated circuitry.
		Measure voltage between +300 volts and common test point.	b. Meter indicates +300 volts.	b. If there is no voltage present and the +300-volt lamp is ON, check series control tube V6 and/or associated circuitry. If the voltage is not correct, adjust the power supply voltages as indicated in step 1 of table IV. If the voltage cannot be adjusted, check tubes V6, V5, V13, V14, and associated circuitry.
		Measure voltage between -300 volts and common test point.	c. Meter indicates -300 volts.	c. If there is no voltage present and the -300-volt lamp is ON, check series control tube V8 and associated circuitry. If the voltage is not correct, adjust the power supply voltages, as indicated in step 1 of table IV. If the voltage cannot be adjusted, check tubes V2, V3, V4, V8, and associated circuitry.
		Connect the VTVM (dc) between BAL and COM test points.	d. Meter indicates 0 volts.	d. Adjust power supply voltages as indicated in step 1 of table IV. Check Z1 and R35.
6	Low voltage power supply lamp supply voltage.	Connect the VTVM (dc) between LAMP test point J4 and GRD test point J3. These are located on the low voltage power supply.	Meter indicates -70 volts.	Adjust LAMP SUP ADJ VOLTS potentiometer R3 as indicated in step 2 of table IV. Check -300-volt supply (step 5c above). Check V2, CR3, R3, and associated circuitry (fig. 152).
7	Test panel-----	Set meter selector switch at +300V.	a. Meter reads approximately 300 volts.	a. Adjust the +300-volt power supply as indicated in step 1 of table IV. Check the +300-volt supply (step 5 above).
		Set meter selector switch at +150V.	b. Meter reads approximately 150 volts.	b. Check the +300-volt supply (step 5 above). Check V1 and R11 of the low voltage power supply.
		Set meter selector switch at +75V.	c. Meter reads approximately 75 volts.	c. Check the +300-volt supply (step 5 above). Check tube V7, resistors R25, R26, and R27 and capacitor C8.
		Set meter selector switch at -20V.	d. Meter reads approximately 20 volts.	d. Check the -20-volt supply (step 4 above). Check relay K1 in the low voltage power supply.
		Set meter selector switch at +4.5V.	e. Meter reads approximately 4.5 volts.	e. Check the +4.5-volt supply (step 4 above).
		Set meter selector switch at -300V.	f. Meter reads approximately -300 volts.	f. Adjust the -300-volt supply as indicated in step 1 of table IV. Check the -300-volt supply (step 5 above).

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER

Note. Refer to fig. 140 for parts location in the transmitter unit.

Step	Function	Procedure	Normal indication	Probable location of fault
8	Initial setup----	Check that the encoder wiring option is connected properly for target voltage to be used. Set 250V REF and 300V REF switch S5 to correspond to the reference voltage to be used (par. 20). Set S3 on the encoder at ADJ (fig. 14).		
9	Clock pulses and set zero pulses (fig. 163(2) and 133).	Set the PC switch on the transmitter unit at normal (up). Using the oscilloscope, observe set zero (SZ) pulses, CP 1 and CP 2 pulses at J25B-6, J26B-7, and J27B-7, respectively. Check frequency of SR set zero pulses and clock pulses, using the oscilloscope with calibrated time base.	a. Waveforms should appear as shown in figure 159. b. Pulses appear at 750 per second (1.33 milliseconds between pulses).	a. Check for SZ pulse at J25B-6, CP 1 at J26B-7 and CP 2 at J27B-7. If only CP 2 is missing check J27B (par. 203). If only CP 1 and CP 2 are missing, check J26B. If all three are missing, check the input of J25B at pin 2. If the input pulse is present, check J25B. If input is not present, check that S9 (PC) is in the up position and then check for an output pulse at pin 4 of J14A. If output is present at pin 4, check S9, T1, and associated circuitry. If output pulse is not present, check output of J15A-6. If output is present, check J14A (par. 203). If output is not present, check at J20-11. If there is no output at J20-11, check at J20-1. If 1,500 cycles is present at pin 1, check the pulse frequency divider. If there is no 1,500 cycles, check at pin C of J4 (par. 207) in the modulator chassis. If 1,500 cycles is present, check interconnections. If there is no 1,500 cycles, check at TP1 in the modulator. If 1,500 cycles is present at TP1, check Q1, Q2, and associated circuitry. If no 1,500 cycles is present at TP1, check Q8 and associated circuitry. If this does not locate trouble, check all voltages and then power supply (steps 1-7 above). b. If any or all pulses are missing, check the packages listed in a above.

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
10	Units ring (UR) and tens ring (TR).	Set the PC switch at test (down) (fig. 9). Set sel at TS 00 and step through 1 complete frame. Set sel at TS 55 and recycle.	a. UR advances 1 stage at a time and TR advances 1 stage each time UR recycles. b. At TS 57, RC F/F (reset) lamp goes OFF, and on the next step the stages that were ON go OFF (TR 50 and UR 4), and both zero stages (TR 00 and UR 0) come ON. c. TR 50 and UR 6 come ON. RC F/F is ON.	a. Check at J16B-3 for test pulse (par. 198d). If no pulse is present, check J16B and associated circuitry (par. 203). If no units ring works, check at pin 2 of UR 0 (J6B) for clock pulses. If no clock pulses appear, perform step 9a. If clock pulses appear at pin 2 of J6B, check J6B (par. 203). If only 1 UR package does not work, check the associated package. If none of the TR packages come ON, check the output of UR 9 and the associated gate circuitry for the clock pulse input. If only 1 of the TR packages does not come ON, check the associated package (par. 203). If program generator runs continuously, refer to step 11. b. If RC F/F does not go OFF, check for inputs at pins 2 and 7 of J12A. If no input is present at pin 7, check for TSG 56 at J19-15. If no output is present at J19-15 (par. 200b), check J19 inputs (fig. 159). If no input is present, check J11A and J12B (par. 203). If this does not locate trouble, refer to step 10a. If no input is present at terminal 2 of J12A, check for CP 1 at J26B-7. If clock pulses are present at J26B-7, check interconnections. If no CP 1 is present, refer to step 9a. If inputs are present at pins 2 and 7 of J12A, check for output at pin 3 (fig. 159). If no output is present, check J12A (par. 203). If output is present at pin 3, check J13A (par. 203). If TR 00 and UR 0 do not come ON, check for output clock pulses at J21-8 and J21-10. If no clock pulses are present, check for negative bias (RC F/F OFF bias) at J21-5. If no clock pulses but bias is present, check gating circuits CR4, C4, R4 and CR3, C3, R3 of J21. c. If TR 50 and UR6 do not come ON, check the gating circuitry associated with J13A and check J13A (par. 203).

Table VII. Performance and Trouble Location Checklist—Continued
TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
10		Set sel at TS 56 and recycle.	d. TR 50 and UR 7 come ON. RC F/F is OFF.	d. If RC F/F stays ON, refer to step 10b. If TR 50 and UR 7 do not come ON, check J11A and J13B (par. 203). If this does not locate trouble, refer to step 10a.
		Set sel at TS 57 and recycle.	e. TR 00 and UR 0 are ON. RC F/F is ON.	e. Check J21-8 and J21-10 (par. 203).
11	Recycle test circuit.	Set PC switch down. Set sel at TS 10 and recycle.	a. Rings stop at TS 11---	a. If program generator runs continuously when RECYC button is depressed, check output of J17B. If J17B goes OFF, check diode CR5 in J20. If J17B does not go OFF, set PC switch up and check input at pin 2. If there is no input, perform step 9a. If the clock pulse is present, set PC switch down and check pin 6 of J17B (fig. 159). If no input is present at terminal 6, check S10, S11, and appropriate packages (par. 203). Appropriate packages for TS 10 are J7A and J6B. (Remember that the indicator lamps will indicate one time slot later than the switch positions indicate.) If either S10 or S11 does not have an output, refer to step 10a to check appropriate package. If no input is present at pin 2, check at J26B-7, and if no output is present at J26B-7, refer to step 9a. If there is an output at J26B-7, check interconnections. If there are inputs at terminals 2 and 6, check for output at terminal 5 of J17B (par. 198d). If there is an output, check gating circuitry associated with J17B. If there is no output, check J17B (par. 203) and switch S3. If program generator stops at other than designated time slot, check switches S10 and S11. If the program generator stops correctly but the indicator lights do not come on, check appropriate packages and lights.
		Set sel at TS 20 and recycle.	b. Rings stop at TS 21---	b. Refer to step 11a. Appropriate packages for TS 20 are J8A and J6B and for indicator lights for TS 21 are J7A and J7B.
		Set sel at TS 30 and recycle.	c. Rings stop at TS 31---	c. Refer to step 11a. Appropriate packages for TS 30 are J9A and J6B and for indicator lights for TS 31 are J8A and J7B.
		Set sel at TS 40 and recycle.	d. Rings stop at TS 41---	d. Refer to step 11a. Appropriate packages for TS 40 are J10A and J6B and for indicator lights for TS 41 are J10A and J7B.

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
11		Set sel at TS 50 and recycle. Set sel at TS 00 and recycle. Set sel at TS 1 through TS 8, and recycle each time.	e. Rings stop at TS 51--- f. Rings stop at TS 1---- g. Rings stop at TS 2 through TS 9.	e. Refer to step 11a. Appropriate packages for TS 50 are J11A and J6B and for indicator lights for TS 51 are J11A and J7B. f. Refer to step 11a. Appropriate packages for TS 00 are J6A and J6B and for indicator lights for TS 1 are J6A and J7B. g. Refer to step 11a. Appropriate package for TR 00 is J6A and for UR 2 through UR 9 are J8B through J15B. <i>Note.</i> Each unit time slot used in this circuit with switches S10 and S11 is made up of tens ring 00 and the appropriate units ring. Each multiple of tens time slot is made up of UR 0 and the appropriate multiple of tens ring. Each time slot between 11-19, 21-29, 31-39, 41-49, and 51-59 is made up of the appropriate units ring and tens ring.
12	Encoder start and reset pulses.	Connect the oscilloscope to V10B, pin 8 (fig. 135). Use care in setting oscilloscope to avoid instability. Set sel at TS 6 for trigger voltage. Set sel at TS 18-----	a. First encoder start pulse (ESP) occurs at beginning of trace (TS 6). b. Second ESP appears at beginning of trace (TS 18).	a. If no first (H) ESP is present, check inputs at pins 2 and 7 of J16A. If no input is present at pin 2, check output at J26B-7. If no output appears at J26B-7, refer to step 9a. If there is an output at J26B-7, check interconnections. If no input is present at terminal 7, refer to note below. <i>Note.</i> When any TSG bias voltage is missing check for an output at the appropriate numbered terminal of J19 (fig. 149 and 159). If no output is present at the appropriate numbered terminal check for inputs from the appropriate units ring and tens ring packages at the appropriate lettered terminals of J19. If the inputs are present, check the gating circuitry inside the T/R package (par. 204). If no inputs are present, or if only one of the inputs is present, check the appropriate units ring and/or tens ring. Troubleshooting of units and tens rings is explained in step 10a. If output is present at numbered terminal of J19, check interconnections to find point where bias is lost. b. If second (X) ESP is not present at terminal 3 of J16A, check input at terminal 8 of J16A (fig. 159). If input is present, check J16A (par. 203). If no input is present, check for inputs at terminals H and C of J20 (fig. 159). If no input is present at terminal H, refer to note following step 12a. If no input is present at terminal C, refer to step 9a. If both inputs are present, check the appropriate gating circuitry of J20.

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
12		Set sel at TS 30-----	c. Third encoder start pulse (ESP) appears at beginning of trace (TS 30). These pulses, as well as the reset pulses, are positive and have an amplitude of approximately 21 volts peak (14 volts minimum) at the leading edge, and approximately 11 volts at the trailing edge (less than 10 volts peak decay after 15 usec). The duration is approximately 30 usec (15 usec min.).	c. If no third (Y) ESP is present at pin 3 of J16A, check input at terminal 8 of J16A (fig. 159). If input is present, check J16A. If no input is present, check inputs at pins E and C of J20. If both inputs are present, check appropriate gating circuits in T/J package (par. 204). If no input is present at C of J20, refer to step 9a. If no input is present at E of J20, refer to note following step 12a.
		Connect the oscilloscope to V10A pin 3. Set sel at TS 15.	d. First encoder reset pulse occurs at the beginning of the trace (TS 15).	d. If no encoder reset pulse appears at pin 3 of J18A, check inputs at terminals 2 and 7 of J18A (fig. 159). If inputs are present, check J18A (par. 203). If no input is present at J18A-7, refer to note following step 12a. If no input is present at J18A-2, refer to step 9a.
		Set sel at TS 27-----	e. Second encoder reset pulse occurs at the beginning of the trace (TS 27).	e. If no ERP is present at pin 3 of J18A, check for an input at terminal 8; if there is an input, check J18A (par. 203). If no input appears at terminal 8, check for inputs at J20-C and J20-8 (fig. 149). Refer to step 9a. If no input appears at J20-C, refer to note following step 12a. If no input appears at J20-8, refer to note following step 12a. If both inputs are present, check the appropriate gating circuits of the T/J package.
		Set sel at TS 39-----	f. Third encoder reset (ERP) pulse occurs at the beginning of the trace (TS 39).	f. If no ERP is present at pin 3 of J18A, check for an input at pin 8. If there is an input, check J18A. If there is no input, check for inputs at J20-A and J20-C. If there is no input at J20-C, refer to step 9a. If there is no input at J20-A, refer to note following step 12a. If both inputs are present, check appropriate gating circuit of T/J package.

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
13	Ready tone control.	Set PC switch at test (down). Set CDG/TAC switch at CDG/TAC. Set CONTINUOUS-REMOTE START switches at CONTINUOUS. Set sel at TS 55 and recycle.	a. RTC F/F is OFF-----	a. If recycle circuit does not function properly, refer to step 11. If RTC F/F is ON, check S6A, S60A, and the gating voltage at terminal 5. The voltage at terminal 5 normally is approximately -15 volts. If it is approximately -2.5 volts or more positive, the clock pulse at pin 2 is allowed to pass, turning the package ON. If this happens, check the TSG voltage as outlined in note following step 12a. The voltage at terminal 2 is normally -2.5 volts. A voltage of approximately -12 volts or more (not counting the clock pulse) allows the clock pulse to pass without a gating bias at terminal 5. If this does not correct the trouble, check the clock pulse circuit as outlined in step 9a.
		Step-----	b. RTC F/F comes ON--	b. If RTC F/F does not come ON and the recycle test circuit is all right (step 11), check J24A (par. 203). Check the inputs at pins 2 and 5 of J24A (fig. 159). If no input appears at pin 2, refer to step 9a. If no input appears at terminal 5, refer to note following step 12a.
		Set sel at TS 00 and recycle.	c. RTC F/F is ON-----	c. If RTC F/F does not stay ON, check J24B. Refer to step 13b.
		Step-----	d. RTC F/F goes OFF--	d. If RTC F/F does not go OFF, check the inputs at pins 2 and 7 of J24B. If there is no input at J24B-2, refer to step 9a. If no input is present at J24B-7, refer to note following step 12a. If both inputs are present, check for an output at J24B-3 (fig. 159). If there is no output, check J24B. If output is present, check J24A.
		Set CDG/TAC-OC switch at CDG/TAC. Have the associated equipment send a RTC start signal. Recycle.	RTC comes ON-----	If RTC does not come ON, refer to b above.

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
13		Have the associated equipment send a RTC stop signal. Recycle.	RTC goes OFF-----	If RTC does not go OFF, refer to <i>d</i> above.
		If the associated equipment is not set up to furnish RTC start and stop signals at this time, use the following alternate method: Set the CDG/TAC-OC switch at CDG/TAC. Remove pins 27 and 28 from J18 on the cabinet (par. 19). Ground J3-8 on the transmitter unit with a clip lead. Recycle.	RTC comes ON-----	If RTC does not come ON, refer to <i>b</i> above.
		Remove the clip lead from J3-8 and connect it to J3-7. Recycle.	RTC goes OFF-----	If RTC does not go OFF, refer to <i>d</i> above.
14	Parallax read-in.	Set in H parallax word of 1010101010. Set S1 on the encoder at ADJ. Set sel at TS 5, recycle, and step.	<i>a.</i> 1010101010 appears in binary counters.	<i>a.</i> If no binary counters come ON, check for TSG voltage at the end of R2 away from CR1 and for CP 2 at the junction of CR1 and CR2. If no TSG voltage is present, refer to note following step 12 <i>a</i> . If no CP 2 is present, refer to step 9 <i>a</i> . If both voltages are present, check the gating circuits. If one or more, but not all, of the binary counters do not come ON, check for an input to terminal 7 of the associated K package, J44A through J53A. Check the parallax read-in diode associated with the package. If no input is present, check the associated switch, S38 through S47. If an input appears at terminal 7, check the package (par. 204).
		Reverse all parallax switches. Recycle and step. Set in X parallax of 10101010101.	<i>b.</i> 0101010101 appears in binary counters.	<i>b.</i> Same procedure as in <i>a</i> above except check for TSG voltage at the end of R4 away from CR2.

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
14		Set sel at TS 17, re-cycle, and step. Reverse all parallax switches. Recycle and step. Set in Y parallax word of 10101010101. Set sel at TS 29. Re-cycle and step. Reverse all parallax switches. Recycle and step. <i>Note.</i> The following step is necessary only if step 14 reveals binary counter trouble. If step 14 is satisfactory, do not perform step 15. Set all H, X, and Y parallax switches at 1 (up). Set sel at TS 17, TS 28, and TS 1 and recycle each time.	c. 1010101010101 appears in binary counters. d. 0101010101010 appears in binary counters. e. 1010101010101 appears in binary counters. f. 0101010101010 appears in binary counters.	c. Same procedure as in <i>a</i> above except check for TSG voltage at the end of R4 away from CR2. The switches are S25 through S37 and the packages are J44A through J56A. d. Same procedure as in <i>c</i> above except check for TSG voltage at the end of R6 away from CR3. e. Same procedure as in <i>a</i> above except check for TSG voltage at the end of R6 away from CR3. The switches are S12 through S24 and the packages are J44A through J56A. f. Same as <i>e</i> above.
15	BC reset-----		BC is clear-----	If 1 binary counter stage stays ON: a. Check the corresponding K package, J44A through J56A (par. 203). b. Check the corresponding C or L package, J31 through J42. If all binary counters for which parallax switches were thrown stay ON, check the appropriate TSG voltage at J23. If it is not present, refer to the note following step 12a. If it is present, check for the CP 2 input. If CP 2 is not present, or is incorrect, refer to step 9a. If both the TSG voltage and CP 2 are present, check the gating circuitry (par. 204).

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
16	Shift register---	Set all parallax switches at 0 (down). Set CONTINUOUS-REMOTE START switches at CONTINUOUS. Set sel at TS 55 and recycle. Step----- Step 9 times-----	All SR stages are OFF--- a. Sync word 0111111010000 appears in SR. b. Sync word moves 1 place toward SR 1, and then out, on each step.	a. If no part of the sync word appears in the shift register, check for inputs at C and E of J22 (T/S package). If no input is present at C, refer to note following step 12a. If no input is present at E, refer to step 9a. If inputs are present at both E and C, check the gating circuit (par. 204). If one or more parts of the sync word do not appear in the shift register, check the individual package concerned (J44A through J56B (par. 203)) and the diode gates CR2, 5, 8, 11, 14, 20 in the T/S package (fig. 150), and CR20 and 22 in the T/N package. b. If the shift register does not shift properly, check the set zero pulse at J25B-6 (fig. 159). If set zero pulse is not present, refer to step 9a. If SZ pulse is present and a number of the packages stay ON, a likely trouble is that the last package is staying ON and is causing the other packages to come ON in turn due to its memory circuit. This could result from a shorted transistor in this package. Check the last package that stays ON (highest numbered SR package). If the reverse happens and packages do not come ON, check the last package that was ON but did not turn ON the next package. The trouble may result from either the memory circuit of this package (par. 203) or the loss of the clock pulse input. Check for CP 1 at J26B-7. If no clock pulse is present, refer to step 9a.

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
17	Auxiliary data read-in.	Set in auxiliary word of 1010101010. Set sel at TS 6 and re-recycle. Step----- Reverse all auxiliary switches. Recycle and step.	a. All SR stages except SR 1 are OFF. Sync bit is in SR 1. b. Auxiliary word 1010101010 is in SR. c. 0101010101 auxiliary word appears in SR.	a. Perform step 16a. b. If auxiliary word does not appear in the shift register, check for ground at the terminals associated with the operated auxiliary switches (J22-K, -V, -10; and J23-D and -J). If these checks do not locate the trouble, check the time slot gate voltage at J22-J. If no voltage is present, refer to the note following step 12a. If gate voltage is present, check for the presence of clock pulses at J22-E. If clock pulses are not present, refer to step 9a. If clock pulses are present, check diodes CR19, 18, 12, and 6 of J22 (fig. 150), and diodes CR19 and CR15 of J23 (fig. 151). Check the gate circuits associated with these diodes. c. Perform the tests in b above, except check for grounds at J22-R, -15, and -7; and J23-11 and -10. Check diodes CR19, 15, and 9 of J22; and CR17 and 13 of J23.
18	Data read-in.	Set in: H parallax 0101010101, X parallax 1010101010101, and Y parallax 111111111111. Set sel at TS 16, recycle, and step.	<i>Note.</i> During a complete recycle period these words are first read into the BC, and are then read from the BC into the SR. a. H word 0101010101010 is in SR.	a. If H word does not appear in shift register, check inputs at J23-7 and J23-15. If no input appears at J23-7, refer to step 9a. If no input is present at J23-15, refer to note following step 12a. If both inputs are present, check the gating circuit (CR6, C4, and R6 (fig. 151)). If one of the shift registers does not operate properly, check the package concerned (par. 203). If this does not locate the trouble, check for a bias output from the associated binary counter. If bias is not present, check the binary counter (step 14). If there is a bias output, check the associated gating circuit in the T/S and T/N packages (J22 and J23) (figs. 150 and 151).

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
18		Set sel at TS 17 and recycle.	b. H word is still in SR.	b. Proceed as in <i>a</i> above. If this does not locate the trouble, set sel at TS 16, recycle, and step. If this corrects the trouble, check the recycle test circuit (step 11).
		Set sel at TS 26, recycle, and step.	c. X word 1010101010101 is in SR.	c. If X word does not appear in shift register, check for inputs at J23-7 and J23-13. If no input is present at J23-7, refer to step 9a. If no input is present at J23-13, refer to note following step 12a. If both inputs are present, check for an input at J28B-2. If input is not present at J28B-2, check the gating circuit in J23 (par. 203). If input is present at J28B-2, check for an output at J28B-7. If output is not present, check J28B. If only SR 11 through SR 13 work correctly, check CR23 in J23 (fig. 151). If one of the shift registers does not work, check for a bias at the output of the associated binary counter. If bias is not present, check the binary counter (step 14). If bias is present, check the associated gating circuit in J22 or J23 and the appropriate SR package (J44B and J56B).
		Set sel at TS 27 and recycle.	d. X word is still in SR.	d. Proceed as in <i>c</i> above. If this does not locate trouble, set sel at TS 26, recycle, and step. If this corrects trouble, check recycle test circuit (step 11).
		Set sel at TS 39, recycle, and step.	e. Y word 1111111111111 is in SR.	e. If trouble occurs, proceed as in <i>c</i> above except that the TSG input is at J23-12 instead of J23-13 and the gating circuit consists of CR10, C8, and R11.
		Set sel at TS 40 and recycle.	f. Y word is still in SR.	f. Proceed as in <i>e</i> above. If this does not locate the trouble, set sel at TS 39, recycle, and step. If this corrects trouble, check the recycle test circuit (step 11).

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
19	Coordinate and earth curvature relay lockups.	Set sel at TS 00, recycle, and step. Set sel at TS 1 and recycle. Set sel at TS 13, recycle, and step. Set sel at TS 14 and recycle. Set sel at TS 15, recycle, and step. Set sel at TS 16 and recycle.	a. ECLU and HLU come ON. b. ECLU and HLU are ON. c. ECLU and HLU to OFF. d. ECLU and HLU are OFF. e. XLU comes ON----- f. XLU is ON-----	a. If ECLU does not come ON, check for inputs at J26A-5 and J26A-2. If no input is present at J26A-2, refer to step 9a. If no input is present at J26A-5, refer to note following step 12a. If both inputs are present, check J26A (par. 203). If HLU does not come ON, check the inputs at J27A-2 and J27A-5. If no input is present at J27A-2, refer to step 9a. If no input appears at J27A-5, refer to note following step 12a. If both inputs are present, check J27A. If neither ECLU nor HLU comes ON, or if they come ON and then go OFF, check for an output at J25A-6. If output is present, check J25A. b. Proceed as in a above. If this does not correct trouble, check recycle test circuit (step 11). c. If ECLU and HLU do not go OFF, recycle again, and if ECLU, HLU, XLU, and YLU stay ON, CLR is not furnishing a reset pulse. Check inputs at J25A-5 and J25A-2. If no input is present at J25A-2, refer to step 9a. If no input is present at J25A-5, refer to note following step 12a. If both inputs are present, check J25A. d. Proceed as in c above. If this does not correct trouble, check recycle test circuit (step 11). e. If XLU does not come ON, check the inputs at J28A-2 and J28A-5. If no input is present at J28A-2, refer to step 9a. If no output is present at J28A-5, refer to the note following step 12a. If both inputs are present, check J28A. f. Proceed as in e above. If this does not locate trouble, check the recycle test circuit (step 11).

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
19		Set sel at TS 25, recycle, and step.	<i>g.</i> XLU and ECLU are OFF.	<i>g.</i> If XLU does not go OFF, check for an output at J25A-6. If output is present, check connections between J25A-6 and J28A-8. If output is not present, check input (clock pulse) at J25A-7. If input is present, check J25A. If input is not present, check for inputs at J21-1 and J21-3. If no input is present at J21-1, refer to note following step 12 <i>a</i> . If no input is present at J21-3, refer to step 9 <i>a</i> . If both inputs are present, check the gating circuit (CR1, C1, and R1) (fig. 150).
		Set sel at TS 26 and recycle.	<i>h.</i> XLU and ECLU are OFF.	<i>h.</i> Proceed as in <i>g</i> above. If this does not locate the trouble, check the recycle test circuit (step 11).
		Set sel at TS 27, recycle, and step.	<i>i.</i> YLU comes ON-----	<i>i.</i> If YLU does not come ON, check for inputs at J29A-2 and J29A-5. If no input is present at J29A-2, refer to step 9 <i>a</i> . If no input is present at J29A-5, refer to note following step 12 <i>a</i> . If both inputs are present, check J29A (par. 203).
		Set sel at TS 28 and recycle.	<i>j.</i> YLU is ON-----	<i>j.</i> Proceed as in <i>i</i> above. If this does not locate trouble, check the recycle test circuit (step 11).
		Set sel at TS 38, recycle, and step.	<i>k.</i> YLU and ECLU are OFF.	<i>k.</i> If YLU does not go OFF, check for an input to J29A-8. If no input is present, check at J25A-6. If output is present at J25A-6, check interconnections. If no output is present at J25A-6, check for an input (clockpulse) at J25A-7. If input is present, check J25A. If input is not present, check for inputs at J21-3 and J21-4. If no input is present at J21-3, refer to step 9 <i>a</i> . If no input is present at J21-4, refer to note following step 12 <i>a</i> . If both inputs are present, check the gating circuit (CR2, C2, and R2) (fig. 150).
		Set sel at TS 39 and recycle.	<i>l.</i> YLU and ECLU are OFF.	<i>l.</i> Proceed as in <i>k</i> above. If this does not locate trouble, check the recycle test circuit (step 11).

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
20	Coordinate data relays.	Disconnect H, X, and Y target voltages from P18C, terminals 17, 16, and 15. Connect the ohmmeter to J2-1 and J2-4. Set sel at TS 00 and recycle. Step----- Connect ohmmeter to J2-2 and J2-4. Set sel at TS 15 and recycle. Step----- Connect ohmmeter to J2-3 and J2-4. Set sel at TS 27 and recycle. Step----- Set sel at TS 38, recycle, and step. Reconnect H, X, and Y target voltages to P18C (par. 19).	a. Meter reads open----- b. Meter reads continuity-- c. Meter reads open----- d. Meter reads continuity-- e. Meter reads open----- f. Meter reads continuity. g. Meter reads open-----	<i>Note.</i> Before checking these relays, be sure that step 19 has been performed to eliminate the packages as a source of trouble. When the relay is suspected, make a check of continuity as outlined in the procedure column. Next check the external circuitry, especially the diode across the relay. a. Check relay K1C and external circuitry (fig. 135). b. Check relay K1C and external circuitry. c. Check relay K1A and external circuitry. d. Check relay K1A and external circuitry. e. Check relay K1D and external circuitry. f. Check relay K1D and external circuitry. g. Check relay K1D and external circuitry.
21	Overall digital---	Set PC switch at normal (up). Set all auxiliary and parallax switches at 0 (down). Connect the oscilloscope to the data lead, terminal C of J23. Synchronize the oscilloscope at the beginning of the frame by setting sel at TS 57 and obtaining synchronizing signal from SYNC test point on panel. Set sweep to observe a full frame. Build up a full frame by setting in, one at a time, auxiliary digits and H, X, and Y parallax digits.	Sync word 111111010000 shows on oscilloscope. As each switch is thrown, another 1 is added to the frame pattern.	See all previous steps.

Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
22	Encoder and binary counters.	Set OPR-ALIGN switch S4 at ALIGN. Have reference voltages on and use appropriate target voltage option and REF switch setting (par. 20). Operate S3 on the encoder to OPR (up). Set PC switch on transmitter unit at normal (up) and wait one minute for the sweep amplifier and zero set amplifier to stabilize. Set PC switch on transmitter unit at test (down). Set all parallax switches at 0 (down). Set sel at TS 15 and recycle. See note in par. 198b----- Recycle several times. Set in H parallax word of 0100000000 and recycle. Set sel at TS 27 and recycle. Set in X parallax word 0100000000000 and recycle.	----- Half-scale code, appears in BC: 0000000001 or 1111111110. Either represents half-scale code or 512, the difference between them being 1 quantum. This checks the encoder count. A variation of 1 quantum is possible because of slight uncertainty of 100-kc pulse start and reset time. Same code as above. Half-scale code plus 2 quanta: Half scale_ 0000000001 2 quanta__ 0100000000 sum----- 0100000001 or: Half scale_ 1111111110 2 quanta_ 0100000000 sum----- 1000000001 This verifies that the binary counter counts correctly with the parallax in BC 1. Half-scale code in BC. Half-scale plus 2 quanta.	Refer to par. 205.

TRANSMITTER—Continued

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Table VII. Performance and Trouble Location Checklist—Continued

TRANSMITTER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
23		Set the XMTR AT (db) on the test panel at 0 db and set the meter selector switch at XMTR SIG LVL. Set REC LINE switch S4 to EXT. Set sel at TS 56 and re-cycle.	d. Reads near 4 on the meter scale. Make a note of this reading. e. Reads the same as 1,500-cycle tone in preceding step.	d. See step 5 of table IV. Also refer to c above. e. If 600 cycles is not present, check at pin 1 of T6. If 600 cycles is present at pin 1 of T6, check T2. If 600 cycles is not present at pin 1 of T6, check at pin 1 of T5. If 600 cycles is present at pin 1 of T5, check at pin 1 of Z3. If waveform is incorrect at pin 1 of Z3, check the ready tone control circuit (step 13). If waveform at pin 1 of Z3 is correct, check at pin 3 of Z3. If waveform at pin 3 of Z3 is incorrect, check Z3. If waveform at pin 3 of Z3 is correct, check CR8, CR9, Q5, and associated circuitry. If 600 cycles is not present at pin 1 of T5, check at pin 4 of T5. If 600 cycles is present at pin 4 of T5, check T5. If 600 cycles is not present at pin 4 of T5, check at pin 1 of T4. If 600 cycles is present at pin 1 of T4, check Q3, Q4, and associated circuitry. If 600 cycles is not present at pin 1 of T4, check at pin 4 of T4. If 600 cycles is present at pin 4 of T4, check T4. If 600 cycles is not present at pin 4 of T4, check at pin 3 of T3. If 600 cycles is present at pin 3 of T3, check Q7 and associated circuitry, including adjustment of R22 (step 4 of table IV). If 600 cycles is not present at pin 3 of T3, check at pin 1 of T3. If 600 cycles is present at pin 1 of T3, check T3. If 600 cycles is not present at pin 1 of T3, check Q9 and associated circuitry.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER

Note. Refer to fig. 141 for parts location in the amplifier synchronizer and to fig. 142 for parts location in the receiver.

Step	Function	Procedure	Normal indication	Probable location of fault
24	Clock pulse and set zero pulse.	On the receiver unit set READY, DATA, and TPC switches at TEST (down). Set the TDC switch (effective only when DATA switch is at TEST) at 0 (down). Set PC switch at NORM (up). Connect the oscilloscope to observe waveforms of SR set zero pulses, CP 1, CP 2 and CP 3 at J36A-6, J37A-7, J38A-7, and J568-7, respectively.	Pulses are the same as the SR set zero and clock pulses in the transmitter, step 9 (fig. 159(1)). Clock pulse waveform (fig. 159(1)).	a. Check for CP 2 at J38A-7, CP 1 at J37A-7, and set zero pulse at J36A-6 (fig. 159(1)). If only CP 2 is missing, check J38A (par. 203). If only CP 1 and CP 2 are missing, check J37A (par. 203). If all three are missing, check for an input (clock trigger pulse) at J36A-2. If input is present, check J36A (par. 203). If input is not present, check that switch S39 is in NORM position; then check for an output at J2-C in the amplifier synchronizer. If output is present at J2-C, check interconnections for output at J1-15 on the receiver group, and check S39. If output is not present at J2-C, proceed as in b below. b. Check for an output at J8-E in the amp sync (fig. 159(9)). If no output is present, check that the TPC switch is at the TEST position; this will put J8-U at ground potential. Then check the gating circuit (CR5, CR6, and CR8; C7; and R10, R13, and R14 in the AS/B package). If there is an output at J8-E, check for an output at J9B-6 (fig. 159(8)). If no output is present at J9B-6, check J9B (par. 203). If there is an output at J9B-6, check for outputs at J7-3 and J7-4 (fig. 159(6) and 159(8)). If either of these outputs is missing or if they do not occur once for every two inputs to J9B-4, check J7 (par. 203). If outputs are present at J7-3 and J7-4, check for an output at J12B-6 (fig. 158(8)). If no output is present, check J12B (par. 203). If output is present at J12B-6, check for outputs at J9A-3 and J9A-4 (fig. 159(6) and 159(8)). If either output is missing or if these outputs do not occur once for each two inputs to J12B-8 (fig. 159(9)), check J9A (par. 203). If

Table VII. Performance and Trouble Location Checklist—Continued

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Step	Function	Procedure	Normal indication	Probable location of fault
24				outputs are present at J9A-3 and J9A-4, check for output at J11B-6 (fig. 159(8)). If no output is present for J11B-6, check J11B (par. 203). If output is present, check for output at J11A-3 (fig. 159(4)). If output is present at J11A-3 and occurs once for every two inputs to J11B-8 (fig. 159(9)), check gating circuit in J13 (fig. 141 and par. 204). If output is not present at J11A-3, check J11A (par. 203). c. If trouble is not located after following procedure in <i>a</i> and <i>b</i> above, it is possible that the frequency divider reset control gate is allowing a pulse to pass continually, and in doing so, keeps turning the binary counters OFF. Putting TPC switch in TEST position should ground J8-11 (fig. 141), disabling this gate. Check this, and if J8-11 is not grounded, check the TPC switch.
25	Manual start. (Note. When making tests of the receiver, operating independently of the transmitter, always press the MS button first to start the ring counters.)	Set EXT-LOCAL switch on the test panel at EXT. Set READY switch on the receiver unit at TEST. Set PC switch at NORM. Set TDC switch at 0 (down). Set DATA switch at TEST. Set TPC switch at TEST. Turn the receiver on and let it run. Place the READY switch at NORM. Put PC switch at TEST. Press MS button.	a. All lights but the TC light go OFF. b. MS light comes ON.	d. Check for clock pulse at J56B-7 (fig. 142). If no clock pulse is present, check for CP input at J56B-2. If no clock pulse is present, perform <i>a</i> through <i>c</i> above. If clock pulse is present check J56B (par. 203). a. If any lights but TC light stay ON, check the associated package or circuit connected with that light. If TC light does not stay ON, check recycle test circuit (step 27). b. If MS light does not come ON, check switch S48. Then check J55A and J23B (par. 203).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
25		Step-----	c. RC 1 F/F comes ON. MS goes OFF.	c. If MS light does not go OFF, check J23B (par. 203). If MS goes OFF and RC 1 F/F does not come ON, check J24B (par. 203). Then check CR10, T1, and C8 in the R/K package.
		Step-----	d. RC 1 F/F goes OFF. RC 2 F/F, TR 00, and UR 0 go ON.	d. If RC 2 F/F, TR 00, or UR 0 do not come ON, check the package that does not come ON. If none of the three come ON, check gating circuit associated with these three packages (fig. 142). The following conditions are necessary for this gating circuit to work correctly: all applied voltages must be correct; RC 1 F/F must be ON; RC 2 must be OFF; a negative bias must be applied from the ready control circuit (F/F No. 2) in the amplifier synchronizer.
26	Units and tens rings.	Set PC switch at TEST. Set sel at TS 00 and recycle twice. Using SP button, single step through a complete frame, stopping when ring counter lights, TR 50 and UR 1 come ON.	a. UR advances 1 stage for each step and TR advances 1 stage each time UR recycles. (Only 1 stage of each ring is ON at 1 time.)	a. If set does not recycle properly, refer to step 27. If units rings do not advance one at a time and tens rings once for each 10 units rings, check that the PC switch is in the TEST position; then check for an output at J54A-3 (par. 199d). If no output is present at J54-3, check J54A-3 (par. 203) and S49. If output is present at J54A-3, check for an input at J36A-2 (par. 198d). If input is present at J36A-2, check J36A, J37A, and J38A as outlined in step 24a. If there is no input at J36A-2, check S39. If one of the lights does not come ON and all others do, it is likely that the trouble is in the light circuit or is a burned out lamp. If none of the lights past a certain time slot comes ON, check the first package that did not come ON and the package on each side of it (par. 203).

Note. The troubleshooting of TSG's in the receiver is the same as in the transmitter except that J20 (the R/T package) is used instead of J19. The troubleshooting procedure when the TSG bias is missing is outlined in the note following step 12a.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
26		Set READY switch at TEST and step.	b. All ring stages are OFF. RC 2 lamp is OFF. RC 1 lamp is ON.	b. If RC 2 and the ring stages do not go OFF, check for inputs at J19-4 and J19-11 (fig. 159(1)). If no input is present at J19-4, refer to note following step 26a. If no input is present at J19-11, refer to step 24. If both inputs are present, check for inputs at J21A-2 and J21B-2 (par. 198d). If no inputs are present, check gating circuit (CR5, C3, and R7 of the R/K package). If inputs are present at J21A-2 and J21B-2, check for outputs at J21A-6 and J21B-6 (fig. 159(1)). <i>Note.</i> J21A resets the units ring and J21B resets the tens ring and RC 2 F/F. If no output is present at J21A-6, check J21A (par. 203). If this does not locate trouble in units ring circuit, check the package that stays ON and the one preceding it (J22A through J31A). If no output is present at J21B-6, check J21B (par. 203). If this does not locate the trouble in the tens ring and RC 2 circuits, check the package that stays ON and the one preceding it (J25B through J31B). If RC 1 does not come ON, check for TSG voltage at J20-1 and for a clock pulse at J24B-2 (fig. 159(1)). If no TSG voltage is present at J20-1, refer to note following step 26a. If TSG voltage is present, check READY switch S40. If no clock pulses are present, refer to step 24. Under ordinary operating conditions with the READY switch in NORM position, the bias voltage for RC1 F/F comes from the output of F/F No. 2 in the amplifier synchronizer. To check this circuit, refer to step 40e. If RC 2, TR 00, and UR 0 lamps do not come back ON, check that RC 1 is ON and negative bias is applied from the ready control circuit (F/F No. 2) to the combination gate in the R/K package (fig. 142). The conditions for RC 2 and TR 00 and UR 0 lamps to come ON are that RC 1 F/F must be ON, furnishing a positive bias; RC 2 F/F must be OFF, furnishing a negative bias; and F/F No. 2 must be OFF, furnishing a negative bias from the ready control circuit.
		Step-----	RC 2 is ON and RC 1 goes OFF. TR 00 and UR 0 are ON. <i>Note.</i> RC 1 and RC 2 are the indicator lights for RC 1 F/F and RC 2 F/F.	See step 25.
		Set sel at TS 51 and recycle.	All ring stages are OFF. RC2 is OFF and RC 1 is ON.	See step 25.

Table VII. Performance and Trouble Location Checklist—Continued

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Step	Function	Procedure	Normal Indication	Probable location of fault
27	Recycle test circuit.	Set sel at TS 00 and recycle. Set sel at TS 10 and recycle. Set sel at TS 20 and recycle. Set sel at TS 30 and recycle. Set sel at TS 40 and recycle. Set sel at TS 00 and recycle. Set sel at TS 1 and recycle. Set sel at TS 2 and recycle. Similarly set sel at TS 3, TS 4, TS 5, etc., to TS 47 and recycle each time to TS 9.	TR 00 and UR 1 are ON. Rings stop at TS 11 (no other). Rings stop at TS 21. Rings stop at TS 31. Rings stop at TS 41. Rings stop at TS 1. Rings stop at TS 2. Rings stop at TS 3. Rings stop at TS 4, TS 5, TS 6, etc. to TS 00.	The procedure for troubleshooting the recycle test circuit is identical to that of the recycle test circuit in the transmitter, with the exception of the symbol designations. Refer to step 11 for the procedure, to figure 172(1) for the package designation.
28	Shift register----	Set PC and DATA switches at TEST (down). Set SLANT-GROUND switches at GROUND. Set H, X, and Y parallax switches No. 1 at OFF (down). Set sel at TS 10 and recycle. Set sel at TS 20 and recycle. Set sel at TS 33 and recycle. Set H, X, and Y parallax switches No. 1 at 1 (up). Set sel at 10 and recycle. Set sel at TS 20 and recycle.	a. PSR is OFF (If PSR is ON, a 1 is read in by mistake.) b. PSR is OFF----- c. PSR is OFF----- d. PSR is ON----- e. PSR is ON-----	a. If PSR comes ON, check PH1 switch S27. b. If PSR comes ON, check PX1 switch S14. c. If PSR comes ON, check PY1 switch S1. d. If PSR does not come ON, check for a clock pulse at J32B-7 (fig. 159(1)). If clock pulse is present check J32B (par. 203). If clock pulse is not present, check for CP at C of S27 (fig. 172(2)). If a clock pulse is present, check S27. If a clock pulse is not present, check for CP 1 at the cathode of CR3 (fig. 172(2) and 159(1)). If CP 1 is present, check the gating circuit CR3, C3, and R3. If CP 1 is not present, refer to step 24. e. Proceed as in d above except that the switch is S14 and the gating circuit is CR2, R2, and C2.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
28		Set sel at TS 33 and recycle.	<i>f.</i> PSR is ON-----	<i>f.</i> Proceed as in <i>d</i> above except that the switch is S1 and the gating circuit is CR1, R1, and C1.
		Set all X and Y parallax switches at 1 (up). Set in H parallax word of 1010101010. Set sel at TS 10, recycle, and step.	<i>g.</i> H word read into SR: PSR-0. SR 1-1. SR 2-0. SR 3-1. SR 4-0. SR 5-1. SR 6-0. SR 7-1. SR 8-0. SR 9-0. SR 10-0. SR 11-0. SR 12-0. SR 13-1. At this time SR 13 contains the first digit of H word and PSR contains the second digit.	<i>g.</i> If all SR's are OFF, set selector switch at TS 11 and recycle. If the shift register works properly, check the single pulse circuit (step 26a). If SR 1 through SR 8 are all OFF, check for an output at J20-16. If the TSG is not present, refer to the note following step 26a. If a TSG is present, check for a CP at the cathode end of CR15 of J17 (fig. 172(2) and 159(1)). If no CP is present, refer to step 24. If a CP is present, check the gating circuit, CR39, R8, C6, and R9 of the receiver unit. If one or more, but not all of SR 1 through SR 8 are incorrect, check the corresponding parallax read-in diode and switch (CR28 through CR36 and S28 through S36). Also check the appropriate package (J33B through J40B, par. 203 and fig. 133). If SR 13 does not come ON, check the serial adder (step 31).
		Set sel at TS 11 and recycle.	<i>h.</i> Same pattern in SR---	<i>h.</i> If <i>g</i> above has been done and the shift register works correctly for that step but not when selector switch is at TS 11, check the recycle test circuit (step 27).
		Reverse all H parallax switches to form H word 0101010101 and recycle.	<i>i.</i> H word read into SR: PSR-1. SR 1-0. SR 2-1. SR 3-0. SR 4-1. SR 5-0. SR 6-1. SR 7-0. SR 8-1. SR 9-0. SR 10-0. SR 11-0. SR 12-0. SR 13-0.	<i>i.</i> Proceed as in <i>g</i> above except that SR 13 should not come ON.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure.	Normal indication	Probable location of fault
28		Set all H parallax switches at 1 (up) and recycle. Set all H and Y parallax switches at 1 (up). Set in X parallax word of 1010101010101. Set sel at TS 20, recycle, and step. Set sel at TS 21 and recycle.	<i>j.</i> H word read into SR: PSR-1. SR 1-1. SR 2-1. SR 3-1. SR 4-1. SR 5-1. SR 6-1. SR 7-1. SR 8-1. SR 9-1. SR 10-0. SR 11-0. SR 12-0. SR 13-1. <i>k.</i> X word read into SR: PSR-0. SR 1-1. SR 2-0. SR 3-1. SR 4-0. SR 5-1. SR 6-0. SR 7-1. SR 8-0. SR 9-1. SR 10-0. SR 11-1. SR 12-0. SR 13-1. At this time SR 13 contains the first digit of the X word and PSR contains the second digit. <i>l.</i> Same pattern in SR---	<i>j.</i> Proceed as in <i>g</i> and <i>h</i> above. <i>k.</i> If all shift registers are OFF, set selector switch at TS 21 and recycle. If this corrects the trouble, check the single pulse circuit (step 26<i>a</i>). If this does not correct the trouble, proceed as follows. If no shift register comes ON, check for TSG voltage at J20-13 (fig. 172(1) and 159(1)) and for a clock pulse at the cathode of CR38 (fig. 172(2) and 159(1)). If no TSG voltage is available, refer to step 26<i>a</i>. If no clock pulse is available, refer to step 24. If both are present, check the gating circuit, CR38, C5, R6, and R7. If one or more, but not all, of the shift registers do not operate properly, check the appropriate parallax read-in switch and diode (S15-S26 and CR16-CR27) and the appropriate package (J32B-J43B, J44 and J45; par. 203 and fig. 133). If SR 13 does not come ON, check the serial adder (step 31). <i>l.</i> If <i>k</i> above has been done and the shift registers work correctly when the selector switch is set at TS 20, recycled, and stepped, but not when set at TS 21 and recycled, check the recycle test circuit (step 27).

Table VII. Performance and Trouble Location Checklist—Continued
RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
28		Reverse all X parallax switches to form X word 0101010101010 and recycle.	<i>m.</i> X word read into SR: PSR-1. SR 1-0. SR 2-1. SR 3-0. SR 4-1. SR 5-0. SR 6-1. SR 7-0. SR 8-1. SR 9-0. SR 10-1. SR 11-0. SR 12-0. SR 13-0.	<i>m.</i> Proceed as in <i>k</i> and <i>l</i> above except that SR 13 does not come ON.
		Set all X parallax switches at 1 (up) and recycle.	<i>n.</i> X word read into SR: PSR-1. SR 1-1. SR 2-1. SR 3-1. SR 4-1. SR 5-1. SR 6-1. SR 7-1. SR 8-1. SR 9-1. SR 10-1. SR 11-1. SR 12-0. SR 13-1.	<i>n.</i> Proceed as in <i>k</i> and <i>l</i> above.
		Set all H and Y parallax switches at 1 (up). Set in Y parallax word of 1010101010101. Set sel at TS 33, recycle, and step. (One purpose of this test is to check the operation of diodes, e.g., that there is no cross-talk between coordinates.)	<i>o.</i> Y word read into SR: PSR-0. SR 1-1. SR 2-0. SR 3-1. SR 4-0. SR 5-1. SR 6-0. SR 7-1. SR 8-0. SR 9-1. SR 10-0. SR 11-1. SR 12-0. SR 13-1.	<i>o.</i> If all shift registers are OFF, set selector switch at TS 34 and recycle. If this corrects the trouble, check the single pulse circuit (step 26a). If this does not correct the trouble, proceed as follows. If all shift registers are OFF, check for a TSG voltage at J20-7 (fig. 159(1)) and for a clock pulse at the cathode of CR37 (fig. 172(2) and 159(1)). If no TSG voltage is present, refer to the note following step 26a. If no clock pulse is present, refer to step 24. If both voltages are present, check the gating circuit (R4, CR37, C4, and R5). If one or more, but not all, of the shift registers do not work properly, check the appropriate parallax read-in switch and diode (S2-S13 and CR4-CR15) and appropriate packages (J32B-J43B, J44, and J45, fig. 172(2) and 159(1)). If shift register 13 does not come ON, check the serial adder (step 31).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
28		Set sel at TS 34 and recycle.	<i>p.</i> Same pattern in SR.	<i>p.</i> If <i>o</i> above has been done and the shift registers work properly when the selector switch is set at TS 33, recycled, and stepped but not when at TS 34 and recycled, check the recycle test circuit (step 27).
		Reverse all Y parallax switches to form Y word 0101010101010. Set sel at TS 34 and recycle.	<i>q.</i> Y word read into SR: PSR-1. SR 1-0. SR 2-1. SR 3-0. SR 4-1. SR 5-0. SR 6-1. SR 7-0. SR 8-1. SR 9-0. SR 10-1. SR 11-0. SR 12-0. SR 13-0.	<i>q.</i> Proceed as in <i>o</i> and <i>p</i> above except that SR 13 does not come ON.
29	Shift pulse disable.	Set all Y parallax switches at 1 (up) and recycle.	<i>r.</i> Y word read into SR: PSR-1. SR 1-1. SR 2-1. SR 3-1. SR 4-1. SR 5-1. SR 6-1. SR 7-1. SR 8-1. SR 9-1. SR 10-1. SR 11-1. SR 12-0. SR 13-1.	<i>r.</i> Proceed as in <i>o</i> and <i>p</i> above.
		Set sel at TS 00 and recycle.	<i>a.</i> SPD F/F is ON.	<i>a.</i> If SPD F/F does not come ON, check for a TSG voltage at J16A-5 (fig. 159(1)) and for a clock pulse at J16A-2 (par. 198 <i>d</i>). If no TSG voltage appears, refer to note following step 26 <i>a</i> . If no clock pulse appears, refer to step 24. If both voltages are present, check J16A (par. 203).
		Set sel at TS 9 and recycle.	<i>b.</i> SPD F/F still ON.	<i>b.</i> If SPD F/F does not stay ON, check for an input at J16A-10 (J24B-3, fig. 159(5)). If an input is present, check J42A (fig. 133 and par 203) and recycle test circuit (step 27). If there is no input at J16A-10, check J16A (par. 203).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
29		Set sel at TS 10 and re-cycle.	c. SPD F/F is OFF.	c. If SPD F/F stays ON, check for an input at J16A-10 (J24B-3, fig. 159(5)). If an input is present, check J16A (par. 203). If an input is not present, check for a clock pulse at J42A-2 and a time slot gate at J42A-7 (fig. 159(1)). If no input is present at J42A-2, refer to step 24. If no input is present at J42A-7, refer to the note following step 26a. If both inputs are present, check J42A (par. 203).
		Set sel at TS 11 and re-cycle.	d. SPD F/F is ON-----	d. If SPD F/F does not come ON, check for an input (clock pulse) at J16A-7. If an input is present, check J16A (par. 203). If an input is not present, check for an input (CP) at J17-8 and a TSG voltage at J17-M (fig. 172 (2) and 159 (1)). If no input is present at J17-8, refer to step 24. If no input is present at J17-M, refer to note following step 26a. If both inputs are present, check gating circuit (R15, CR15, and C12 of the R/W package).
		Set sel at TS 19 and re-cycle.	e. SPD F/F still ON-----	e. Proceed as in b above.
		Set sel at TS 20 and re-cycle.	f. SPD F/F is OFF-----	f. If SPD F/F stays ON, check for an input at J16A-10 (J24B-3, fig. 159(5)). If an input is present, check J16A (par. 203). If input is not present, check for an input (CP) at J42A-8 (fig. 159(1)). If input is present, check J42A (par. 203). If no input is present, check for inputs at J17-11 (TSG) and a clock pulse at J17-8 (fig. 159(1)). If no input is present at J17-8, refer to step 24. If no input is present at J17-11, refer to note following step 26a. If both inputs are present, check the gating circuit (CR7, CR8, C5, R6, and R7 of the R/W package).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
29		Set sel at TS 21 and re-cycle.	<i>g.</i> SPD F/F is ON-----	<i>g.</i> If SPD F/F does not come ON, check for an input (CP) at J16A-7 (fig. 159 (1)). If an input is present, check J16A (par. 203). If there is no input, check for an input (CP) at J17-8 and a TSG at J17-V (fig. 159 (1)). If there is no input at J17-8, refer to step 24. If there is no input at J17-V, refer to note following step 26 <i>a</i> . If both inputs are present, check the gating circuit (CR13, C10, and R13 of the R/W package).
		Set sel at TS 32 and re-cycle.	<i>h.</i> SPD F/F is still ON---	<i>h.</i> Proceed as in <i>b</i> above.
		Set sel at TS 33 and re-cycle.	<i>i.</i> SPD F/F is OFF-----	<i>i.</i> If SPD F/F stays ON, check for an input at J16A-10 (J24B-3, fig. 159(5)). If an input is present, check J16A (par. 203). If there is no input, check for an input (CP) at J42A-8 (fig. 159(1)). If there is an input at J42-8, check J42A (par. 203). If there is no input at J42A-8, check for an input (CP) at J17-8 and a TSG at J17-9 (fig. 159(1)). If there is no input at J17-8, refer to step 24. If there is no input at J17-9, refer to note following step 26 <i>a</i> . If both inputs are present, check the gating circuit (CR6, C4, R4, CR8, and R7).
		Set sel at TS 34 and re-cycle.	<i>j.</i> SPD F/F is ON-----	<i>j.</i> If SPD F/F does not come ON, check for an input (CP) at J16A-8 (fig. 159 (1)). If input is present, check J16A (par. 203). If there is no input, check for inputs at J17-8 (CP) and J17-T (TSG) (fig. 172(2) and 159(1)). If there is no input at J17-8, refer to step 24. If there is no input at J17-T, refer to note following step 26 <i>a</i> . If both inputs are present, check the gating circuit (CR14, C11, and R14 of the R/W package).
		Set sel at TS 45 and re-cycle.	<i>k.</i> SPD F/F is still ON---	<i>k.</i> Proceed as in <i>b</i> above.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
		Set sel at TS 46 and recycle.	1. SPD F/F is OFF-----	1. If SPD F/F stays ON, check for an input at J16A-10 (J24B-3, fig. 159(5)). If an input is present, check J16A (par. 203). If there is no input, check for input (CP) at J42A-8 (fig. 159(1)). If an input is present, check J42A (par. 203). If there is no input, check for inputs at J17-8 (CP) and TSG at J17-5 (fig. 159(1)). If no input is present at J17-5, refer to note following step 26a. If both inputs are present, check the gating circuit (CR5, CR8, C3, R5, and R7 of the R/W package). <i>Note.</i> The shift pulse generator (J33A) is a F/O that puts out one negative pulse to the shift registers for each time slot that the SPD F/F is ON. This output (CP) is from J33A-7 (fig. 159(1)). If the shift registers do not advance properly, check for this output. If the output is not present, check for an output at J16A-6 and a clock pulse at J17-J (fig. 159(1)). If there is no clock pulse, refer to step 24. If there is no output at J16A-6, check J16A (par. 203). If both are present, check the gating circuit (CR18 and R20 of J17 and C2, CR2 and R1 of J33A) and J33A (par. 203).
30	Carry storage---	Set TDC switch at 1 (up). Set SLANT-GROUND switches at GROUND. Set all parallax switches at 1 (up). Set DATA switch at TEST. Set sel at TS 19 and recycle.	a. CCS lamp I12 is ON--	a. If CCS lamp I12 does not come ON, check that J18-B is grounded and that J18-C has a voltage level of approximately -2.5 volts. If J18-B is not grounded, check TDC switch S47 and DATA switch S38. If the voltage at J18-C is incorrect, check the output voltage at J32B-6 (fig. 159(3)). (This is the output of the PSR package and should be approximately -2.5 volts when the PSR is ON as it should be at this time. If PSR is not ON, check J32B (par. 203) and the shift register and shift pulse disable stages (steps 28 and 29)). If voltages at J18-B and J18-C are correct,

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
30				check the voltage at J18-S. This voltage should be between -2.5 volts and ground. If this voltage is incorrect, check the AND gate (CR14, CR16, and R14). If the voltage is correct, check for a clock pulse at J15A-2 (par. 198d). If there is no clock pulse, refer to step 24. If a clock pulse is present and the voltage at J15A-5 or J18-S is correct, check J15A (par. 203). If this does not locate the trouble, check for an input at J15A-10 (J24B-3, fig. 159(5)). If this input is present, check J41A (par. 203) and the recycle test circuit (step 27).
	Set sel at TS 20 and recycle.		b. CS is OFF-----	b. If CS F/F does not go OFF, check for an input at J15A-10 (J24B-3, fig. 159(5)). If the input is present, check J15A (par. 204). If the input is not present, check for a TSG voltage at J18-2 and for a clock pulse at J18-1 (fig. 159(1)). If no TSG voltage is available, refer to the note following step 26a. If there is no clock pulse, refer to step 24. If both are present, check for an input at J41A-8 (par. 199d). If the input is not present, check the gating circuit (CR22, C11, R21, CR21, and R20). If input is present, check J41A (par. 204).
	Set sel at TS 32 and recycle.		c. CS is ON-----	c. Proceed as in <i>a</i> above.
	Set sel at TS 33 and recycle.		d. CS is OFF-----	d. If CS F/F does not go OFF, check for an input at J15A-10 (J24B-3, fig. 159(5)). If the input is present, check J15A (par. 203). If there is no input, check for TSG voltage at J18-3 and for a clock pulse at J18-1 (fig. 159(1)). If there is no TSG voltage, refer to note following step 26a. If there is no clock pulse, refer to step 24. If both are present, check for an input at J41A-8 (par. 198d). If an input is present check J41A (par. 203). If an input is not present, check the gating circuit (CR23, CR21, C12, R22, and R20).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
31	Serial adder-----	Set all H and Y parallax switches at 0 (down). Set in X parallax word of 1110001110000. Set sel at TS 20 and recycle. Insert data word 0011001100110 as follows: Set DATA switch at TEST. Start with TDC switch at 0 (down) and step twice. Set TDC switch at 1 (up) and step twice. Set TDC switch at 0 (down) and step twice. Set TDC switch at 1 (up) and step twice. Set TDC switch at 0 (down) and step twice. Set TDC switch at 1 (up) and step twice. Set TDC switch at 0 (down) and step once.	Sum word of X parallax and data word appears in SR (stages 1-13). PX----1110001110000 Data---0011001100110 Sum---1100100101110	To check the serial adder, observe the sum word as it goes into SR 13. If SR 13 does not go ON when it should, check for an input at J45B-7 (par. 198d). If the input is present, check J45B (par. 203). If the input is not present, then the serial adder must be checked. To check the serial adder: - Determine by binary addition which gate should be working (data only, parallax only, carry only, or all present). - Check the components of the appropriate gate. - At those times in the binary addition when it is necessary for a ONE to be carried into the next column (i.e., when both data and parallax are present), the CS F/F should turn ON. When neither data nor parallax is present, the CCS F/O should turn ON, turning the CS F/F OFF. Troubleshooting of these stages is explained in step 30. The components of the gates for these stages are: - CS F/F gate (fig. 113 and 142). - CCS F/O gate (fig. 112 and 142).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
31				d. If the sum word comes into SR 13 right but one or more of the other shift registers do not work properly, refer to steps 28 and 29. If this does not locate the trouble, it is likely that the memory circuit in one of the packages is bad. Check the last package that goes ON properly (par. 203). Also check the set zero inputs and the shift pulse generator output. If the set zero pulse is missing, refer to step 24. If the SP output is missing, refer to step 29.
32	Aux lockups----	Set all parallax switches at 0 (down). Set PC switch at TEST. Set TDC switch at 0 (down). Set DATA switch at TEST. Set SGL SCALE—DBL SCALE switches at SGL SCALE. Set sel at TS 10 and re-cycle. Remove the plug from J3 in order to disconnect the associate equipment from these circuits. Connect the ohmmeter between Aux Com and each of the 10 aux outputs (J3-1 through 10) (fig. 172(3)), one at a time. Set TDC switch at 1, re-cycle, and step.	All aux lockups are OFF. a. Meter reads open circuit for each. b. All aux lockups are ON. Meter reads continuity for each.	a. If the meter reads continuity for any of the 10 leads (J3-1 through 10), check the AUX LOCK-UPS lights 1 through 10 to be sure the auxiliary lock-ups packages are OFF. If any of them come ON, check the corresponding package (J4A through J13A, par. 203). If none of the lockups are ON, check the associated relay (K1A through K1E and K2A through K2E). b. If none of the auxiliary lockups come ON, check for TSG voltage at J17-K (be sure that all SGL SCALE-DBL SCALE switches are in the SGL SCALE position) and for a clock pulse at J17-8 (par. 198d). If no TSG voltage is present, check S54A and then refer to note following step 26a. If no clock pulses are present, refer to step 24. If both are present, check for an output (clock pulse) at J17-R (par. 198d). If an output is not present, check the gating circuit (CR16, C13, R16, and R17).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
32		Set sel at TS 11 and recycle. Set TDC switch at 0 (down) and recycle.	c. All aux lockups are ON. d. All aux lockups are OFF.	If an output is present at J17-R, check the connections from J17-R to the auxiliary lockups. If one or more, but not all, of the auxiliary lockups fail to come ON, check the associated package (J4A through J13A, par. 203). If this does not locate the trouble, check the associated relay (K1A-K1E and K2A-K2E). c. If auxiliary lockups do not stay ON and b above has been done, check the recycle test circuit. d. If auxiliary lockups do not go OFF, check for an output from J32A-6 (SZ, fig. 159(1)). If an output is present, check connections from J32A-6 to auxiliary lockups. If an output is not present, check for a TSG voltage at J32A-5 and for a clock pulse at J32A-2 (par. 198d). If there is no TSG voltage, check S54A; then refer to the note following step 26a. If there are no clock pulses, refer to step 24. If both are present, check J32A (par. 203). If one or more, but not all, of the auxiliary lockups stay ON, check the associated package (J4A-J13A, par. 203) and the input connections from J32A-6 to pin 8 of the associated package.
33	Data lockups----	Set the TDC switch at 0 (down). Set the DATA switch at TEST. Set the PC switch at TEST. Set all parallax switches at 0 (down). Set sel at TS 21 and recycle. Set sel at TS 31 and recycle. Set sel at TS 44 and recycle. Set in H parallax word 1010101010. Set in X parallax word 0101010101000. Set in Y parallax word 1010101010000. Set sel at TS 20 and recycle.	a. All data lockups are OFF each time. b. All data lockups are OFF.	a. If any of the data lockups come ON when sel is set at either TS 21, TS 31, or TS 44, check the associated shift register package (steps 28 and 29 and par. 203). If the associated SR is not ON, check the data lockup package (J4B through J13B, par. 203). b. If data lockups do not stay OFF, check the recycle test circuit (step 27) and J34A (par. 203).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
33		Set sel at TS 21 and recycle.	c. H word is in DLU stages.	c. If none of the H word appears in the data lockups, check for TSG voltage at J17-V and for a clock pulse at J17-8 (fig. 159(1)). If there is no TSG voltage, refer to the note following step 26a. If there is no clock pulse, refer to step 24. If both are present, check for an output (CP) at J17-10 (par. 198d). If an output is present, check connections to data lockups. If there is no output, check gating circuit (CR12, C9, R12, and R11). If one or more, but not all, of the data lockups fail to operate properly, check the associated data lockup package (J4B through J13B, par. 203). If this does not locate the trouble, check the associated shift register package (steps 28 and 29 and par. 203).
		Set sel at TS 30 and recycle.	d. All data lockups are OFF.	d. If data lockups do not go OFF, check for TSG voltage at J17-3 and for a clock pulse at J17-8 (fig. 159(1) and par. 198d). If there is no TSG voltage, refer to note following step 26a. If there is no clock pulse, refer to step 24. If both are present, check for input at J34A-7 (par. 198d). If no input is present at J34A-7, check the gating circuit (CR4, R3, C2, R2, and CR1). If the input is present at J34A-7, check for output at J34A-6 (SZ, fig. 159(1)). If an output is present at J34A-6, check the connections to the data lockups. If there is no output at J34A-6, check J34A (par. 203). If one or more, but not all, of the data lockups do not go OFF, check the connections to that package and the package itself (J4B-J13B, par. 203).
		Set sel at TS 31 and recycle.	e. X word is in DLU stages.	e. Proceed as in c above except that the TSG voltage appears at J17-16 and the TSG voltage gate is composed of R9, CR10, and C7.
		Set sel at TS 43 and recycle.	f. All data lockups are OFF.	f. Proceed as in d above except that the TSG voltage comes in at J17-1 and the TSG voltage gate is composed of R1, CR3, and C1.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
33		Set sel at TS 44 and recycle. Set all parallax switches (H, X, and Y) at 1 (up). Set sel at TS 20 and recycle. Set sel at TS 21 and recycle. Set sel at TS 30 and recycle. Set sel at TS 31 and recycle. Set sel at TS 43 and recycle. Set sel at TS 44 and recycle. Set DBL SCALE-SGL SCALE switch at DBL SCALE. Set all parallax switches at 0 (down). Set sel at TS 21 and recycle.	<i>g.</i> Y word is in DLU stages. <i>h.</i> All data lockups are OFF. <i>i.</i> All data lockups are ON. <i>j.</i> All data lockups are OFF. <i>k.</i> All data lockups are ON. <i>l.</i> All data lockups are OFF. <i>m.</i> All data lockups are ON. <i>n.</i> All DLU's are OFF except DLU 10. DLU 10 is ON.	<i>g.</i> Proceed as in <i>c</i> above except that TSG voltage comes in at J17-12 and gate is composed of CR9, C6, and R8. <i>h.</i> Proceed as in <i>d</i> above except that TSG voltage input is at J34A-5 and clock pulse input is at J34A-2. <i>i.</i> Proceed as in <i>c</i> above. <i>j.</i> Proceed as in <i>d</i> above. <i>k.</i> Proceed as in <i>e</i> above. <i>l.</i> Proceed as in <i>f</i> above. <i>m.</i> Proceed as in <i>g</i> above. <i>n.</i> If DLU 10 does not come ON, check that SR12 is OFF. If SR12 is not OFF, refer to step 28. Check for TSG voltage at J17-L and for clock pulse at J17-8. If TSG voltage is not present, refer to note following step 26<i>a</i>. If clock pulse is not present, refer to step 24. If both are present check gates in R/W package (J17), R20, C14, R18, CR17; and CR22, R21, C15.
34	Off scale detection.	Set the TDC switch at 0 (down). Set the DATA switch at TEST. Set all H, X, and Y parallax switches at 0 (down). Set sel at TS 33 and recycle.	<i>a.</i> OSD F/F is ON.	<i>a.</i> If OSD F/F does not come ON, check the voltage at pin 6 of J43B, J44B, and J45B. This voltage should be approximately -16 volts as these three packages should be OFF. If the voltage is approximately -2.5 volts at any of these pins, check the associated package (par. 203). If these voltages are correct, check the gating circuit (J19) associated with each (fig. 172(2) and par. 198<i>d</i>). If these gating circuits are all right, there should be no clock pulse at pin 2 of J43A. If this clock pulse is not present and OSD F/F is still ON, check J43A and J16B (par. 203).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
34		Set X parallax switch No. 11 at 1 (up). Set sel at TS 34 and recycle.	b. OSD F/F is OFF.	b. If OSD F/F does not go OFF, check the voltage at pin 6 of J43B. This voltage should be approximately -2.5 volts. If this voltage is incorrect, check J43B (par. 203). If J43B is all right, check the shift register and serial adder circuits (steps 28 and 31). If the voltage is correct, check for a clock pulse at J19-11 (par. 198d). If there is no clock pulse, refer to step 24. If clock pulse is present, check for an input at J43A-2 (fig. 172(2) and par. 198d). If there is no input at J43A-2, check the gating circuit (CR14, C12, R18, and R16 of the R/K package). If an input is present at J43A-2, check TSG voltage at J43A-7 (fig. 159(1)). If there is no TSG voltage, refer to note following step 26a. If a TSG voltage is present, check J43A and J16B (par. 203).
		Set X parallax switch No. 11 at 0 (down), set X parallax switch No. 12 at 1 (up), and recycle.	c. OSD F/F is OFF.	c. Proceed as in b above except that the voltage is measured at J44-6 and the gating circuit consists of CR16, R20, and C14 of the R/K package.
		Set X parallax switch No. 12 at 0 (down). Set parallax switch No. 13 at 1 (up).	d. OSD F/F is OFF.	d. Proceed as in b above except that the voltage is measured at J45-6 and the gating circuit consists of CR15, C13, and R19 of J19 of the R/K package.
		Set X parallax switch No. 13 at 0 (down). Set sel at TS 46 and recycle.	e. OSD F/F is ON.	e. Proceed as in a above except that triggering pulse goes into J43A-8 instead of J43A-2.
		Set Y parallax switch No. 11 at 1 (up). Set sel at TS 47 and recycle.	f. OSD F/F is OFF-----	f. Proceed as in b above except that TSG voltage is applied at J19-F and has an external gate (CR13, R17, CR16, and C11 of the R/K package).
		Set Y parallax switch No. 12 at 0 (down), set Y parallax switch No. 13 at 1 (up), and recycle.	g. OSD F/F is OFF-----	g. Proceed as in b above except that the gate consists of CR16, R20, and C14 and the TSG voltage is applied as in f above.
		Set sel at TS 34 and recycle.	h. OSD F/F is OFF-----	h. Proceed as in b above except that the gate consists of CR15, R19, and C13, and the TSG voltage is applied as in f above.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
35	All data present.	Set PC switch at NORM. Set all parallax switches at 0 (down). Synchronize the oscilloscope at the SYNC test point on the receiver panel. Set sel at TS 00. Set sweep to show one frame. Connect the oscilloscope probe to J1-14 (fig. 142(2)). One at a time set each of the six X and Y parallax switches concerned (Nos. 11, 12, and 13) at 1 (up). Set all the parallax switches at 0 (down). Synchronize the oscilloscope at TS 13. Transfer probe to J1-9 (fig. 142) or to TB3-2 (fig. 136).	a. All data present signal is a positive-going pulse lasting $1\frac{1}{2}$ milliseconds (one time slot). b. Operation of any of these switches causes the signal to disappear. <i>Note.</i> When the $1\frac{1}{2}$ millisecond pulse disappears, a spike at the leading edge remains. This does not interfere with the normal operation of the equipment. c. Aux data present signal appears at the beginning of the trace.	a. Check at J19-4 for a voltage from TSG 51. If this voltage is not present, refer to the note following step 26a. If this voltage is present and OSD F/F is ON, then the all data present pulse should be present. If OSD F/F does not come ON, refer to step 34. b. Refer to step 34. c. This signal is TSG 14. Check it out as outlined in the note following step 26a.
36	Storage lockups.	Set PC switch at TEST. Set sel at TS 19 and re-cycle. Set sel at TS 21 and re-cycle.	a. All 6 SLU's and FLU are OFF. b. SLU HG is ON.	a. If all SLU's and FLU stay ON, check for an output at J52A-6 (SZ, fig. 159(1)). If an output is present, check connections to SLU's and FLU. If an output is not present, check for TSG voltage at J52A-5 and for a clock pulse at J52A-2 (par. 198d). If there is no TSG voltage, refer to note following step 26a. If there is no clock pulse, refer to step 24. If both are present, check J52A (par. 203). If one or more, but not all, of the SLU's and FLU stay ON, check the connections from J52A-6 to the package or packages that stay ON. Also check the package (J46 through J52A and B, par. 203). b. If SLU HG does not come ON, check for TSG voltage at J47-5 and for a clock pulse at J47-2 (par. 198d). If there is no TSG voltage, refer to step 24. If both are present, check J47 (par. 203).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
36		Step-----	c. SLU HG and SLU HF are ON.	c. If SLU HG goes OFF, check for an input at J47-8. If input is not present, check J47 (par. 203). If input is present, check J52A (par. 203). (SLU HG must be ON for SLU HF to go ON. If SLU HF does not go ON and SLU HG is ON, check for a bias voltage at J46-5. This voltage should be approximately -2.5 volts. This is the output of SLU HG. Also check for a clock pulse at J46-2 (par. 198d). If no bias voltage exists, check connections to SLU HG. If no clock pulse exists, refer to step 24. If both are present, check J46 (par. 203).
		Step-----	d. FLU goes ON-----	d. If FLU does not go ON and SLU HF is ON, check the bias voltage at J52B-5. This voltage should be approximately -2.5 volts. If this voltage is incorrect and the voltage is correct at J46-3 (approximately -2.5 volts), check CR29 and R28. If this voltage is correct, check for a clock pulse at J52B-2 (par. 198d). If no clock pulses exist, refer to step 24. If a clock pulse is present, check J52B (par. 203).
		Set sel at TS 29 and re-cycle.	e. All 6 SLU's and FLU are OFF.	e. If all SLU's and FLU do not go OFF, check for an output at J52A-6 (SZ, fig. 159(1)). If an output is present, check connections to SLU's and FLU. If an output is not present, check for TSG voltage at J18-9 and for a clock pulse at J18-1 (par. 198d). If a TSG voltage is not present, refer to note following step 26a. If there are no clock pulses, refer to step 24. If both are present, check for CP output at J18-8 (fig. 142(3) and par. 198d). If an output is not present at J18-8, check gating circuit (R23, CR24, and C13 in the RIV package). If output is present at J18-8, check J52A (par. 203).
		Set sel at TS 31 and recycle.	f. SLU XG is ON-----	f. Proceed as in b above except that package is J49 (SLU XG).
		Step-----	g. SLU XG, SLU XF---	g. Proceed as in c above except that packages are J49 and J48 (SLU XG and SLU XF).
		Step-----	h. FLU comes ON-----	h. Proceed as in d above except that bias comes from J48 (SLU XF) and gate is CR30.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
36		Set sel at TS 42 and recycle.	i. All 6 SLU's and FLU are OFF.	i. Proceed as in <i>e</i> above except that TSG voltage appears at J18-10, and gating circuit consists of R24, CR25, and C14.
		Set sel at TS 44 and recycle.	j. SLU YG is ON-----	j. Proceed as in <i>b</i> above except that package is J51 (SLU YG).
		Step-----	k. SLU YG, SLU YF are ON.	k. Proceed as in <i>e</i> above except that packages are J51 and J50 (SLU YG and SLU YF).
		Step-----	l. FLU comes ON-----	l. Proceed as in <i>d</i> above except that bias comes from J50 (SLU YF) and gate is CR31.
		Set sel at TS 19 and recycle.	m. ALL SLU's and FLU are OFF.	m. Proceed as in <i>a</i> above.
37	Double-scale operation (using oscilloscope).	Set PC switch at TEST. Set DATA switch at TEST. Set TDC switch at 0 (down). Set SGL SCALE-DBL SCALE switch at DBL SCALE. Set sel at TS 51 and recycle.	a. All ring stages are OFF.	a. If ring stages do not go OFF, check for TSG voltage at J19-4 and check for clock pulses at J19-11 (par. 198d). If no TSG voltage is present, refer to note following step 26a. If no clock pulses are present, refer to step 24. If both are present, check for an output (CP) at J19-7 (par. 198d). If no output is present, check gating circuit (R3, CR3, and C2 of the R/K package). If no output is present, check connections to J21 and J22B (URR and TRR). If only the units rings do not go OFF, check J21A (par. 203). If only the tens rings and RC 2 F/F do not go OFF, check J21B (par. 203).
		Step-----	b. TR 50 and UR 9 are ON.	b. Check switch S54A and J31B (par. 203) if TR 50 does not come ON. Check S54A and J31A (par. 203) if UR 9 does not come ON.
		Step-----	c. TR 00 and UR 0 are ON.	c. Check J26B (par. 203) if TR 00 does not come ON. Check J22A (par. 203) if UR 0 does not come ON.
		Set sel at TS 59 and recycle. Set TDC switch at 1 (up). Set sel at TS 59 and recycle.	d. TR 00 and UR 0 are ON. e. TR 00 and UR 0 are ON.	d. If <i>c</i> above has been done, check the recycle test circuit (step 27). e. Check switch S54A.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
37		Step----- Set sel at TS 00 and re-cycle. Set sel at TS 9 and re-cycle. Step----- Set sel at TS 10 and re-cycle. Set TDC switch at 0 (down). Set sel at TS 20 and re-cycle. Step----- Set sel at TS 21 and re-cycle. Set PC switch at NORM. Set up the oscilloscope as in step 36. Set X parallax switch No. 13 at 1 (up). Recycle. Return X parallax switch No. 13 to 0 (down) and set Y parallax switch No. 13 at 1. Recycle. Return Y parallax switch No. 13 to 0 (down).	<i>f.</i> All aux lockups are OFF. <i>g.</i> All aux lockups are OFF. <i>h.</i> All aux lockups are OFF. <i>i.</i> All aux lockups are ON. <i>j.</i> All aux lockups are ON. <i>k.</i> DLU 10 is ON----- <i>l.</i> DLU 10 is ON----- <i>m.</i> All data present signal. <i>n.</i> All data present signal.	<i>f.</i> Check switch S54A, the TSG voltage at J20-18, and the clock pulse input at J17-8 (par. 198d). Refer to step 32 to locate trouble. <i>g.</i> If <i>f</i> above has been done, check recycle test circuit (step 27). <i>h.</i> Proceed as in <i>g</i> above. <i>i.</i> If auxiliary lockups do not come ON, check for TSG voltage at J20-17 and for clock pulses at J17-8 (par. 198d). If no TSG voltage is present, refer to note following step 26a. If no clock pulses are present, refer to step 24. If both are present, check for CP output at J17-R (par. 198d). If no output is present at J17-R, check S54B and the gating circuit (R16, R17, CR16, and C13). If output is present at J17-R, check connections to auxiliary lockups. <i>j.</i> If <i>i</i> above has been done, check the recycle test circuit (step 27). <i>k.</i> If DLU 10 does not come ON, check for TSG voltage at J20-13 and for clock pulses at the cathode of CR17 of the r/w package (par. 198d). If no TSG voltage is present, refer to note following step 26a. If no clock pulses are present, refer to step 24. If both are present, check for an input (CP) at J13B-7 (par. 198d). If no input is present at J13B-7, check S54B and the gating circuit (R18, CR17, and C14 of the r/w package). If input is present at J13B-7, check J13B (par. 203). <i>l.</i> If <i>k</i> above has been done, check the recycle test circuit (step 27). <i>m.</i> Check switch S54B. <i>n.</i> Check switch S54B.

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
37		One at a time set X parallax switches 11 and 12 and Y parallax switches 11 and 12 at 1 (up). Recycle.	a. On each of these conditions the all data present signal disappears.	a. Refer to step 35.
38	Double-scale operation (without oscilloscope).	Set PC switch at TEST. Set all parallax switches at 0 (down). Set sel at TS 47 and recycle. Set X parallax switch 13 at 1 (up). Recycle. Return X parallax switch 13 to 0 (down), set Y parallax switch 13 at 1 (up), and recycle. Return Y parallax switch 13 to 0 (down). One at a time, set X parallax switches 11 and 12 and Y parallax switches 11 and 12 at 1 (up). Recycle. Return SGL SCALE-DBL SCALE switch to SGL SCALE.	a. OSD F/F is ON ----- b. OSD F/F is OFF ----- c. OSD F/F is OFF ----- d. With the operation of any of these switches, the OSD F/F is OFF.	a. Refer to step 34. b. Check switch S54B. c. Check switch S54B. d. Refer to step 34.
39	Decoder ----- <i>Note.</i> Refer to fig. 136 for parts location in the decoder.	Set decoder REF switch at 300. On the test panel, set DEC REF switch S3 at INT. On the high voltage power supply adjust the ± 300 volts for a balance (par. 25, table IV, step 1). Synchronize the oscilloscope at TS 21. Using the dc input, ground the input of the oscilloscope to determine the zero reference level of the sweep. Set in a half-scale word by setting H parallax switch 10 at 1 (up) and all other parallax switches at 0 (down). Connect the oscilloscope to the H coordinate output at decoder TP1. Synchronize at TS 18. Recycle.	Reads $0 \pm .08$ volt. (Disregard the spikes which appear as a result of decoder switching.)	Refer to par. 206.

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
39		Return H parallax switch 10 to 0 (down) and set X parallax switch 10 at 1 (up). Connect the oscilloscope to TP 2, synchronize at TS 31, and recycle. Return Y parallax switch 10 to 0 (down). Set in Y parallax code of 682: 0101010101 and recycle. Connect the oscilloscope to TP3 and synchronize at TS 44. Set in Y parallax code of 341: 1010101010 and recycle.	Reads $0 \pm .08$ volt.	Same as above.
			Scope indicates $+16.6$ volts.	Same as above.
			Scope indicates -16.6 volts. <i>Note.</i> The accuracy of the over-all equipment is $\pm \frac{1}{2}$ quantum, or $\pm .05$. For these checks a tolerance of $\pm .08$ volt is suitable. The following check can be made if a more accurate reading is desired.	Same as above.
		Set Y parallax switches 1, 2, and 10 at 1 (up). Set all other parallax switches at 0 (down). Synchronize at TS 44 and recycle. Connect the oscilloscope to TP3.	Oscilloscope indicates $+.35$ volt.	Same as above.
40	Amplifier synchronizer <i>Note.</i> Refer to fig. 141 for parts location in the amplifier synchronizer.	Set the REC LINE switch S4 on the test panel at LOCAL. Set CDG/TAC-OC switch S1 on the amplifier synchronizer at CDG/TAC, and the CONTINUOUS-REMOTE START switches on the transmitter unit at CONTINUOUS. Set XMTR at (db) switch on the test panel at 0. Make sure that steps 6, 7, 8, and 9 of table IV (par. 25) have been done. Set all receiver test switches at NORM. Set in transmitter aux word of 1010101010.		

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
40		Set sel (receiver) at TS 00 for oscilloscope sync. Set the oscilloscope sweep for about the first 10 time slots and connect the probe to the following points, one at a time. Connect the second oscilloscope input to view the output of the 6,000-pps generator at J13-10, unless this oscilloscope is needed to compare waveforms simultaneously in the amplifier synchronizer. Ready slicer output E4---	a. Compare with input waveform at E4 (fig. 159(10)).	a. If output at E4 is incorrect, check Q1, Q2, Q3, and associated circuitry. Check output of the separation filter by placing oscilloscope across terminals 4 and 5 of Z1. If ready output of Z1 is correct, check CR3, CR4, CR5, CR6, and associated circuitry. Also check READY ADJ control R13 (step 9 of table IV (par. 25)). If output of Z1 is incorrect, check at pin 1 of V2A. (Checks made from this point back to the line input check both ready and data signals.) If waveform at pin 1 of V2A is correct, replace Z1. If waveform at pin 1 of V2A is incorrect, check pin 1 of V1. If waveform at pin 1 of V1 is correct, check V1, V2, and associated circuitry. If waveform at pin 1 of V1 is incorrect, check across pins 4 and 5 of transformer T1. If this waveform is incorrect, check across terminals 3 and 4 of Z4. If this waveform is correct, check T1. If T1 is correct, check Z4. If Z4 is correct, check the pad consisting of R37, R38, and R39. If these are correct check S1. If input waveform is incorrect, the trouble is in associated equipment or in lines between transmitter and receiver.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
40		Data slicer output E3	b. Data slicer output E3 (fig. 159(10)).	b. To check out data circuit, proceed as in <i>a</i> above except that test points and reference symbols of parts are different. This difference can be noted easily by referring to figure 170(1).
		Emitter of delay F/F E2	c. Delay F/F (emitter), E2 (fig. 159 (10)).	c. If delay F/F does not start at the proper time, check the output of F/F No. 1 (fig. 88). If F/F No. 1 output is normal, check the delay F/F transistor and associated circuitry (par. 201 and 204). Check the diodes in this circuit very carefully (par. 202). If the F/F No. 1 waveform is incorrect, check that the ready signal is correct (<i>a</i> above). If ready signal is correct, check F/F No. 1 transistor and associated circuitry (par. 201 and 204). F/F No. 1 is turned OFF by F/O No. 1 (J12A) which gets necessary negative bias when ready slicer output ceases and a 6,000-pps pulse when delay F/F goes ON. Check this circuit if F/F No. 1 does not go OFF at proper time. If delay F/F does not go OFF at proper time, check if 6,000-pps triggering pulse is getting through gating circuit (R8, CR7, and C7) biased by the output of the delay F/F and with the addition of R19 by the output of F/F No. 1. The delay F/F must be in the ON condition and F/F No. 1 in the OFF condition for this gate to pass the 6,000-pps triggering pulse. The 6,000-pps triggering pulse circuit is covered in <i>g</i> below.
			d. F/F No. 6 output, J3B-3 (fig. 88).	d. If F/F No. 6 does not come ON at the correct time and delay F/F is ON, check for a negative pulse across terminals 4 and 3 of transformer T2 (J3B-2, fig. 159(3)). If pulse is missing, check transformer T2. If pulse is present, check J3B (par. 203).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
40			e. F/F No. 2 output (receiver ready), J15B-3 (fig. 88). f. F/F No. 3 output, J10B-3 (fig. 88).	e. If F/F No. 2 does not come ON at the correct time, check that F/F No. 6 is ON (<i>d</i> above) and that data is present (<i>b</i> above). If both of these are ON, check for a clock pulse input at J15B-2 (fig. 159(1)). If clock pulse is present at J15B-2, check J15B (par. 203). If clock pulse is not present, check for clock pulse input at J14-V (fig. 159(1)). If clock pulse is not present, refer to step 24. If clock pulse is present at J14-V, check the gating circuit (CR7, R21, and C2) and the AND gate (CR5, CR6, and R24). If F/F No. 2 does not go OFF at the correct time, check that F/F No. 6 is OFF. If F/F No. 6 is OFF, check for a 6,000-pps triggering pulse at J15A-2 (fig. 142(2)). If pulse is present, check J15A (par. 203). If pulse is not present, check for 6,000-pps pulses at J14-J (fig. 142(2)). If pulse is not present, refer to <i>g</i> below. If pulse is present at J14-J, check the gating circuit (CR8, R26, and C3). f. If F/F No. 3 does not come ON at the proper time, check that data is present (<i>b</i> above). If data is present, check for 6,000-pps pulses at the junction of R8 and C5 (fig. 194(2) and 159(10)). If no pulses are present, check for 6,000-pps pulses at the cathode of CR7 (fig. 170(2) and 159(9)). If no pulse is present, refer to <i>g</i> below. If pulse is present, check gating circuit (CR7, R8, C5, and R9). If pulse is present at junction of R8 and C5, check for pulse at J10B-2 (fig. 170(2) and 159(9)). If pulse is present at J10B-2, check J10B (par. 203). If F/F No. 3 does not go OFF at the proper time, check that F/F No. 2 is ON at this time and that data is not present. ON bias from F/F No. 2 and F/F No. 3 and OFF data bias are the three conditions necessary to trigger F/O No. 3 which turns OFF F/F No. 3. The AND gate that is fed
		Note pulse missing when F/F No. 3 goes OFF.		

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
40				by F/F No. 3 and F/F No. 2 consists of CR11, CR13, CR10, R15, R16, and C8. If 6,000-pps pulses are not present at pin 2 of J10A, check for a 6,000-pps pulse at the cathode of CR11 (fig. 170). If no pulses are present at the cathode of CR11, refer to <i>g</i> below. If pulse is present, check the AND circuit cited above and the gating circuit consisting of CR11, R15, and C8. If 6,000-pps pulses are present at J10A-2 and is riding on a level of -12 volts as shown in figure 159 (7), check J10A (par. 203). If pulse is riding on a level of -2.5 volts, then data is present. Refer to <i>b</i> above. <i>g.</i> If 6,000-pps pulse output is not present at J13-10, check at pin 3 of transformer T3. If pulse is present, check connections. If no pulse is present at pin 3 of T3, check at pin 1 of T3. If pulses are present at pin 1, check T3. If no pulses are present at pin 1, check at pin 7 of V3. If waveform at pin 7 of V3 is correct, check V3 and associated circuitry. If waveform at pin 7 of V3 is incorrect, check at pin 3 of T1. If waveform at pin 3 of T1 is correct, check T1 and the input circuit of V3B. If waveform at pin 3 of T1 is incorrect, check waveform at J4-10. If waveform at J4-10 is correct, check Q4 and associated circuitry. If waveform at J4-10 is incorrect, check waveform at J4-R. If waveform at J4-R is correct, check V3A, T2, and associated circuitry. If waveform at J4-R is correct, check waveforms at the collector of Q3. If waveform at the collector of Q3 is correct, check Q5, Q6, and associated circuitry. If this waveform is incorrect, check the waveform at E1 (fig. 159(10)). If waveform at E1 is correct, check Q2, Q3, and associated circuitry. If waveform is incorrect, check Q1 and associated circuitry.
		<i>g.</i> Sampling pulse output, J2-C (slot center output, fig. 88).		

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
40		Set up oscilloscope to view output of data slicer E3 and output of F/F No. 5 (J2-F or J16B-6) at the same time (fig. 88).	<i>h.</i> Data follows aux data word set in, and is $\frac{1}{2}$ time slot later in phase with respect to data slicer output. Aux word appears in aux lockups.	<i>h.</i> If F/F No. 5 does not come ON, check for presence of data signal at J16B-5, and for a clock pulse at J16B-2 (fig. 159 (1) and (3)). If data is not present, refer to <i>b</i> above. If no clock pulse is present refer to step 24. If both are present, check J15B (par. 203). If F/F No. 5 does not go OFF at the proper times, check for a clock pulse riding on a level of approximately -12 volts at J16A-2 (J13A-2, fig. 159(1)). If no clock pulse is present, refer to step 24. If voltage level is approximately -2.5 volts, it means that data is present. There must be an absence of data for F/O No. 5 to be triggered. If data is present at the wrong time, refer to <i>b</i> above. If the waveform at J16A-2 is correct, check J16A (par. 203). <i>Note.</i> The one time when there will be an absence of data but F/O No. 5 will not be turned ON to turn OFF F/F No. 5 is the time slot preceding the sync signal (fig. 88). The reason for this is that no clock pulse is generated at this time slot so F/F No. 5 will remain OFF until the next time slot where there is an absence of data.
		Set attenuator REC AT (db) on test panel first at 10 and then at 0. Return the attenuator first to 10 then to 20.	<i>i.</i> Receiver reproduces the correct aux word without delay. <i>j.</i> Receiver reproduces the correct aux word time within one minute.	<i>i.</i> See step 7 of table IV (par. 25). If this does not correct the trouble, refer to <i>a</i> above. <i>j.</i> Proceed as in <i>i</i> above.
41	Overall analog check.	Set all receiver test switches at NORM. Set S7 on the test panel at LOCAL. Set S4 on the encoder at ALIGN. Connect the VTVM(dc), set at a low scale, to the H, X, and Y outputs (TP1, TP2, TP3), respectively, of the encoder, and ground.	Reads approximately 0 on the meter for each coordinate.	See all previous steps. If trouble is indicated to be in a specific circuit, refer to table VI for an idea of trouble-shooting steps versus steps in table VII.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
41		Set in X parallax word 0101010101 in the transmitter and the complement word 0110101010 at the receiver. Remove the ground connections from J2 and restore the coordinate input connections. Set in X parallax word 0000000011. Set in Y parallax word 0000000010.	Reads approximately 0 on the meter for each coordinate.	Check all previous steps.
		Set S3 on the encoder at ADJ. Set in H, X, and Y parallax words 1010101010 on each. Reverse all parallax switches.	Reads approximately +25 volts. Reads approximately -25 volts. <i>Note.</i> These voltages are not sampled as they will be in actual use, and the measured voltage will not necessarily be accurate because of the averaging of the true dc with transients caused by storage lockup and release. Words appear in data lockups lamps.	Check all previous steps. Check all previous steps.
42	Automatic zero set.	Connect the oscilloscope to terminal 1 of T1 on the automatic zero set (fig. 143). Use any transmitter time slot to synchronize the oscilloscope.	Words appear in all lock-up lamps.	Check all previous steps.
		Set S1 on the encoder at ADJ. Connect the VTVM (DC) between TP1 and ground on the encoder. Turn encoder zero set control, R7, quickly CW and then quickly CCW.	a. 60-cycle output is synchronized with the sweep. Signal level is 33 ± 5 volts. b. Voltage jumps sharply each time the control is turned, and returns slowly to the approximate original value within one minute. Adjust the zero set for minimum amplitude of this signal.	a. Check V1, V2, and V3. Check at J1-K for sync signal (fig. 143(2)). If sync signal is not present, check at J1-S in encoder (fig. 135(4)). If signal is present at J2-S, check connections. If no signal is present at J1-S, check at pin 3 of V17 in encoder (fig. 143(2)). If signal is present at pin 3 of V17, check C48. If no signal is present at pin 3 of V17, check V3 and associated circuitry. b. Check K1, V4 (fig. 135), and associated circuitry (fig. 164(1)). Refer to step 10 of table IV (par. 25).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
42		Set S2 on the encoder at ADJ. Connect the VTVM (dc) between TP2 and ground and turn encoder zero set control R30 quickly CCW. Set S3 on the encoder at ADJ. Connect the VTVM (dc) between TP3 and ground. Turn encoder zero set control R58 quickly CW and then quickly CCW. Reset decoder zero set controls as outlined in step 18 of table IV (par. 25). Set S1 (IN) on the decoder at ADJ. Set the PC switch on the receiver panel at TEST. Connect the VTVM (dc) between E1 and ground on the decoder and turn the decoder zero set control R6 quickly CW and then quickly CCW. Reset zero set control R6 as outlined in step 18 of table IV (par. 25).	c. Voltage jumps sharply each time the control is turned and returns slowly to the approximate original value within one minute. Adjust the zero set for minimum amplitude of this signal. d. Voltage jumps sharply each time the control is turned, and returns slowly to the original value within one minute. Adjust the zero set for minimum amplitude of the signal.	c. Check K2, V5 (fig. 135), and associated circuitry (fig. 164(1)). Refer to step 11 of table IV (par. 25). d. Check K3, V6 (fig. 135), and associated circuitry (fig. 164(2)). Refer to step 12 of table IV (par. 25).
43	Remote start----	Set up the data set for remote start operation: a. Set CONTINUOUS-REMOTE START switches on the transmitter unit at REMOTE START. b. Set the NORM-RS switch on the amplifier synchronizer at RS. Set up H, X, and Y code on the transmitter parallax switches 1010101010, etc.	e. Voltage jumps sharply each time the control is turned, and returns slowly to the original value within one minute. Adjust the zero set for minimum amplitude of this signal.	e. Check K4, V7 (fig. 135) and associated circuitry (fig. 163). Refer to step 18 of table IV (par. 25).

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
42		Connect the oscilloscope between terminals P18E-8 and P18B-9 and on the cabinet terminal board. Set CDG/TAC-OC switch on the transmitter unit and on the amplifier synchronizer at CDG/TAC. Arrange to have the transmitter at the remote end of the receiver line send a remote start signal.	Transmitter supplies one complete frame upon receipt of the remote start signal.	a. If the transmitter does not send a single message frame for a remote start signal, check for transmitter clock pulses at pin 8 of J5 in the amplifier synchronizer. If no clock pulses appear, refer to step 9. If clock pulses are present, ask for a series of remote start signals to be transmitted at agreed-on time intervals. b. Several things are necessary for the remote start circuit to function properly. Near the end of the remote start signal there should be a positive bias at pin 7 of J5 in the amplifier synchronizer and negative bias at pins 3, 4, and J of J5 in the amplifier synchronizer (fig. 141). One time slot after a coincidence of the above, F/F No. 7 will go ON, resulting in a positive bias at pin 2 of J5 (fig. 141). With a positive bias at pin 2 and a negative bias at pin J of J5, the clock pulse checked in a above will be passed to pin J of J5. This clock pulse will go to pin N of J1 (fig. 141) in the amplifier synchronizer, then will go to pin 16 of J1 (fig. 159(1) and 139) in the transmitter, then to the RC F/F in the transmitter, turning it ON and causing the transmitter to send one message frame. The above checks cannot all be made simultaneously unless more than one oscilloscope is used. Make the checks two at a time while a string of remote start signals is being received. If one of the above checks indicates the trouble, check the gating circuits in J5 (fig. 140), the CDG/TAC-OC switch in the amplifier synchronizer, and the CONTINUOUS-REMOTE START switches in the transmitter.

Table VII. Performance and Trouble Location Checklist—Continued

RECEIVER—Continued

Step	Function	Procedure	Normal indication	Probable location of fault
42				c. If only part of the message is received by the transmitter, check the indicated section of the transmitter. If the message is sent continuously, check for TSG 1 at pin 7 of J6A in the amplifier synchronizer (fig. 159 (1) and 141(1)). If there is no TSG 1, refer to the note following step 12a. If TSG 1 is present, check J6A and J6B (par. 203).

200. Common Circuit Trouble Location

a. *General.* Five different types of waveforms appear at various circuits throughout the data set. Each type of waveform is different from the other types; however, wherever a waveform of a specific type appears, it is identical to all others of that type. The five types are time slot gates, clock pulses, set zero pulses, F/O output pulses, and lamp circuit pulses. For example, time slot gate voltages appear at many of the packages and have the same waveform wherever they appear and whatever the time slot number. Similarly, clock pulses appear at many of the circuits and they all have the same waveform. The following subparagraphs indicate where each of these common waveforms will be found in the data set. Illustrations of these waveforms and the waveforms of other important circuits in the data set are found in figures 159(1) through 159(10).

b. *Time Slot Gate Circuits* (fig. 159(1)). Time slot gate voltages appear at the following terminals. All TSG voltages are alike regardless of the time slot number. A short circuit of one time slot gate will disable this voltage wherever this TSG should appear. Use the list below for isolating such a short circuit.

Transmitter		Transmitter		Receiver	
TSG	Terminal	TSG	Terminal	TSG	Terminal
	J1-19	7	J19-3		J17-M
	J3-2		J3-10		J20-16
1	J19-1		J22-J		S54B-4
	J23-17	14	J19-4		R8
	J26A-5		J25A-5	14	J20-P
	J27A-5	15	J17-A7		J1-9
6	J16A-7		J19-5	19	J20-15
	J19-2	16	J19-6		J52-5
	R2		J28A-5		S54A-8
				20	J1-9
					J14A-5
					J14B-5
					J17-11
					J18-2
					J20-14
					J34A-5
					R2
					S54A-7
				21	J15B-5
					J17-V
					J20-13
					V47-5
					S54B-11
					R6
				23	J20-12
					J3-12
				29	J18-9
					J20-11
					J3-11
				30	J17-3
					J20-10
				31	J17-16
					J20-9
					J49-5
				0	J16A-5
					J20-18
					J2-20
					S54A-11
				10	J20-17
					J42A-7
					R3
					S54B-5
					S54A-10
					R4
				33	J17-9
					J18-3
					J20-8
					R1
				34	J16B-5
					J17-T
					J20-7
					J43A-7

Receiver		Receiver	
TSG	Terminal	TSG	Terminal
42-----	J18-10	47-----	J19-F
	J20-6		J20-2
43-----	J17-1		S54B-5A
	J20-5	48-----	J20-R
44-----	J17-12		S54B-4A
	J20-4	51-----	J19-4
	J51-5		J20-1
46-----	J17-5		S40A-NC
	J20-3		J2-12
	S54B-11A		

c. *Clock Pulse Circuits* (fig. 159(1)). Clock pulses appear at each of the terminals listed below. CP 1 and CP 2 are listed separately; for all practical purposes the two clock pulses appear simultaneously and have the same waveform. A short circuit of any clock pulse will disable all clock pulses associated with it. If such a short appears, first determine whether it is CP 1 or CP 2, then check for the trouble at the terminals listed below.

Transmitter	
CP 1	CP 2
Bus	Bus
J1-18	CR3
J6B-2	J22-E
J7B-2	J23-14
J8B-2	J24A-2
J9B-2	J24B-2
J10B-2	J25A-2
J11B-2	J26A-2
J12A-2	J27A-2
J17A-2	J27B-7
J12B-2	J28A-2
J13B-2	J29A-2
J14B-2	J3-3
J15B-2	
J16A-2	
J17B-2	
J20-C	
J21-3	
J23-7	
J26B-7	
J27B-2	
J44B-2	
J45B-2	
J46B-2	
J47B-2	
J48B-2	
J49B-2	
J50B-2	
J51B-2	
J52B-2	
J53B-2	
J54B-2	
J55B-2	
S10-10	

Receiver			Receiver		
CP 1	CP 2	CP 3	CP 1	CP 2	CP 3
Bus	Bus	J56B-7	J52-2	J24B-2	
CR1	J14A-2	J2-9	J53B-2	J25A-2	
J1-17	J14B-2	J2-11	J56A-2	J26A-2	
J17-J	J15A-2	J2-13		J27A-2	
J32A-2	J15B-2			J28A-2	
J34A-2	J16A-2			J29A-2	
J37A-7	J16B-2			J30A-2	
J38A-2	J17-8			J31-2	
J46-2	J18-1			J38A-7	
J47-2	J19-11			J42A-2	
J48-2	J22A-2			J55B-2	
J49-2	J22B-2			S46-10	
J50-2	J23A-2			J56B-2	
J51-2	J24A-2				

d. *Set Zero Pulse Circuits* (fig. 159(1)). Set zero pulses are generated by M packages and appear at terminal 6 of those packages. All set zero pulse waveforms are alike. A short circuit of one set zero pulse will also disable the pulse at all other points. Use the following list to locate such a short circuit.

Transmitter unit			
J25B-6	J47B-8	J51B-8	J55B-8
J44B-8	J48B-8	J52B-8	J56B-8
J45B-8	J49B-8	J53B-8	
J46B-8	J50B-8	J54B-8	
Receiver unit			
J32B-8	J36B-8	J41B-8	
J33B-8	J37B-8	J42B-8	
J34B-8	J38B-8	J43B-8	
J35B-8	J39B-8	J44-8	
J36A-6	J40B-8	J45-8	

e. *F/O Output Circuits* (fig. 159(5)). The output pulse, terminal 3 of the C package, is used throughout the data set to reset the F/F packages. The following is a list of circuits having these F/O output pulses which appear at terminal 3 of the F/O and terminal 10 of the associated F/F.

Transmitter unit		
J12A-3	J14A-3	J24B-3
Amplifier synchronizer		
J3A-3	J7B-3	J12A-3
J6A-3	J10A-3	J15A-3
Receiver unit		
J39A-3	J41A-3	J43A-3
J40A-3	J42A-3	J53A-3
		J55A-3

f. *Lamp Circuit Outputs* (fig. 158(1)). The important bistable (F/F) circuits are furnished with indicating neon lamps to show if the circuit

is in the ON or OFF condition. The lamps are triggered ON by the output from the associated package. All these lamp triggering pulses have the same waveform. The following is a list of terminals having these pulses:

Transmitter unit A packages			
J13A-3	J46B-3	J50B-3	J54B-3
J24A-3	J47B-3	J51B-3	J55B-3
J44B-3	J48B-3	J52B-3	J56B-3
J45B-3	J49B-3	J53B-3	

Transmitter unit B packages			
J6A-8	J8A-8	J10A-8	J12B-8
J6B-8	J8B-8	J10B-8	J13B-8
J7A-8	J9A-8	J11A-8	J14B-8
J7B-8	J9B-8	J11B-8	J15B-8

Transmitter unit D packages			
J26A-3	J27A-3	J28A-3	J29A-3

Receiver unit A packages	Receiver unit A packages	Receiver unit A packages	Receiver unit A packages
J15A-3	J25B-3	J36B-3	J41B-3
J16A-3	J32B-3	J37B-3	J42B-3
J16B-6	J33B-3	J38B-3	J43B-3
J23B-3	J34B-3	J39B-3	J44B-3
J24B-3	J35B-3	J40B-3	J45B-3

Receiver unit B packages	Receiver unit B packages	Receiver unit B packages	Receiver unit B packages
J22A-8	J26A-8	J28B-8	J31A-8
J22B-5	J26B-8	J29A-8	J31B-8
J23A-8	J27A-8	J29B-8	
J24A-8	J27B-8	J30A-8	
J25A-8	J28A-8	J30B-8	

Receiver unit D packages	Receiver unit D packages	Receiver unit D packages	Receiver unit D packages
J4A-3	J6B-3	J9A-3	J11B-3
J4B-3	J7A-3	J9B-3	J12A-3
J5A-3	J7B-3	J10A-3	J12B-3
J5B-3	J8A-3	J10B-3	J13A-3
J6A-3	J8B-3	J11A-3	J13B-3

Section III. TROUBLESHOOTING OF TRANSISTORS AND PACKAGES

Caution: Before removing or replacing a transistor package, always set the +4.5V & -20V SUP switch on the low voltage power supply to OFF. Failure to observe this caution may result in damage to the transistor.

201. Transistors

The data set has no built-in facilities for testing transistors. Do not try to test a transistor by measuring terminal resistances with an ohmmeter, since even a low voltage of the wrong polarity applied to a transistor may damage it. If a transistor is suspected of being defective, unsolder, and solder a new transistor in its place.

Caution: Transistors can be damaged by excessive heat. While soldering and unsoldering transistor leads, always grasp the lead with flat pliers between the transistor and the soldering point. Do not hold a hot soldering iron near a transistor long enough to heat the transistor.

202. Diode Testing

Three types of diodes are used in the data processing sections of the data set (including those in packages): SM-B-181088, SM-B-181092, and SM-B-181094. An ohmmeter (TS-505/U or equivalent) can be used to check diodes since this method of measurement has an accuracy sufficient to determine whether or not the diode is acceptable. In general, if the ohmmeter reading is approximately that shown in the table below, the diode is acceptable. Usually, a diode which has been damaged has a low reverse resistance

or a high forward resistance. Typical values of resistance for the three types follow:

	SM-B-181088	SM-B-181092	SM-B-181094
Forward resistance (use low ohm scale).	25 ohms.	5 ohms.	25 ohms.
Reverse resistance (use high ohm scale).	1 meg.	1 meg.	1 meg.

These diodes can be identified by reference to the parts location illustrations, figure 1 and figures 134 through 151, and the schematic diagrams located at the end of chapter 9.

203. Troubleshooting of Transistor Packages A, B, C, D, E, J, K, L, and M

a. Before rejecting any small packages for failure to turn off or failure to turn on, check with the scope probe to see that the input pulse which should cause the package to perform the particular function under question is equal to or greater than the value shown in the chart below. If it is not, check the circuit which feeds this pulse to the package.

Package	Pin No.	Input	Pulse amplitude
A	8	Turn OFF	+2.4
A	2	Turn ON	-9.0
A	7	AUX turn ON	-6.0
B	4	Turn OFF	+2.4

Package	Pin No.	Input	Pulse amplitude
B	2	Turn ON-----	-8.0
B	3	AUX turn ON-----	-6.0
C	2	Driving-----	-6.5
D	8	Turn OFF-----	+2.4
D	2	Turn ON-----	-8.0
D	7	AUX turn ON-----	-6.0
E	2	Driving-----	-6.5
K	5	Turn OFF-----	+3.0
K	8	Turn ON-----	-9.0
L	2	Driving-----	-6.5
M	2	Driving-----	-6.5

If the input pulses are in agreement with the chart, check the individual parts of the package as follows:

- (1) Replace the transistor as outlined in paragraph 201.
 - (2) Check the diodes as outlined in paragraph 202.
 - (3) Check the printed circuitry and other components as outlined in paragraph 204.
- b. If replacement of the package does not correct the trouble, proceed in the following manner:
- (1) Check the supply voltages at the various terminals of the packages. If any of these are incorrect, check the appropriate power supply (steps 1-6 of table VII).
 - (2) Check all of the input and output bias and trigger voltages of the packages. Remember the following points:
 - (a) Any diode gate passes a pulse if the potentials at the plate and cathode are approximately equal and a negative pulse is applied to the cathode or a positive pulse is applied to the anode.
 - (b) Both the F/F and F/O packages turn ON when a pulse is applied that makes the base of the transistor negative with respect to the emitter. (This is true only of PNP point-contact type transistors, the type used in this equipment.) This is normally done by applying a negative pulse to the base, overcoming the applied reverse bias.
 - (c) The F/F package is a bistable circuit and remains ON until a pulse of the opposite polarity is applied. The F/O package is a monostable circuit. After being triggered ON, it returns to its original OFF condition in a time interval determined by the package circuitry.

- (d) Clock pulses occur at the end of each time slot. Set zero pulses occur immediately prior to the clock pulses.
- (e) Combination gates are usually gating circuits external to the package and need positive or negative biases or both applied to them in order for the triggering pulses (usually clock pulses) to be applied to the packages.
- (f) Some terminals of the package go directly to the base of the transistor, or merely through a capacitor or unbiased diode, and a triggering pulse applied to them turns the transistor ON or OFF (depending on the polarity of the pulse). Sometimes these terminals are connected to external gating circuits and sometimes to a source of triggering pulses that trigger the transistor at a definite time. This time is dependent upon other circuitry in the data set (sometimes other packages and sometimes external signals). Other terminals of the packages are connected to the base through gating circuits in the package itself and sometimes through diodes that are biased so that an external signal (usually a TSG) is required to allow the pulse to reach the base.
- (g) The lights associated with the various packages are a possible source of trouble but not as probable a source as most of the other circuitry (packages, gates, power supply, etc.). When the light is suspected, check the voltage at the output of the associated package that is connected to the light. This voltage should be approximately -2.5 volts when the light is on. If this voltage is correct, step 2 of table IV has been done, and the light does not come on, check the resistor associated with the light. If the resistor is good, replace the neon lamp.
- (h) It is possible that the recycle test circuit is causing troubles by not stopping the action at the correct time. A quick check of this would be to check for the normal sequence of events. A check of the units ring and tens ring lights can be made easily. When the UNITS

RING and TENS RING switches are set and the recycle button is depressed, the next succeeding lights should come ON. For example, when the UNITS RING switch is set at 4 and the TENS RING switch is set at 20, the tens ring light 20 and units ring light 5 should come on. If the UNITS RING switch is set at 9, the units ring 0 light should come on and the next tens ring light should come on. Similarly, if the UNITS RING switch is set at 9, the TENS RING switch is set at 20, and the recycle button is depressed, the units ring light 0 and tens ring light 30 should come on. For a check of the recycle test circuit in the transmitter refer to step 11 of table VII, and for the receiver, refer to step 27 of table VII.

204. Resistance and Static Testing of Package Components

Standard resistance measurements should be used to check the resistors in the packages. Remove the package from the jack and check the

resistors using the VTVM (dc). Identify the value of the resistors by the color coding, referring to the standard resistor color code chart in figure 210, or by reference to the appropriate parts location illustration and the appropriate schematic drawing which contains the values of all components. Check diodes as described in paragraph 202. Shorted or leaky capacitors can be checked with the VTVM (dc). Using the VTVM (dc), check the resistance of the pulse transformer windings against the following chart:

Caution: Do not measure the components of a package without first unsoldering and removing the transistors or shorting all elements of the transistors. When soldering and unsoldering transistor leads always use a heat sink between the soldering iron and the transistor.

	Package	Resistance of windings		Ratio
		1-2	3-4	
AS/E	T1-----	16.6	1.4	4:1
	T2-----	1.2	1.5	1:1
E	T1-----	1.7	1.7	1.3:1
J	T1-----	1.2	1.5	1:1
K	T1-----	1.2	1.5	1:1
M	T1-----	16.6	1.4	4:1
T/J	T1-----	1.2	1.5	1:1
	T2-----	1.2	1.5	1:1

Section IV. ADDITIONAL TROUBLESHOOTING

205. Encoder

Follow the procedure outlined in step 22 of table VII. If the half scale code appears, the encoder is working properly. If the count is incorrect, the trouble can be in either the encoder or the binary counter. If nothing appears in the binary counter, the encoder is the likely source of trouble.

a. Overall Check. To determine if trouble is in the encoder or the decoder, set the oscilloscope to observe the transmitter output. Disable the encoder by setting the ENC REF switch on the test panel at OFF. Set the first and tenth switches of H, X, and Y parallax on the transmitter group panel up, and then set the delayed sweep on the oscilloscope to observe the first and tenth bits of either H, X, or Y. After the oscilloscope is set up to observe the first and tenth bits on the delayed sweep, set the ENC REF switch at EXT and turn all parallax switches OFF. Set the OPR-ALIGN switch on the encoder at ALIGN. This sets in a half scale code for the encoder. The oscilloscope should now

show the first nine bits, the tenth bit only, or the first and tenth bits. This is half scale code plus or minus one 100-kc pulse. Set OPR-ALIGN switch at OPR.

b. 100-kc Pulse Generator Check. If the count is missing, check at pin 3 of XV16 (figs. 135(2) and 61). If pulses and gating voltage are both present, check CR6. If the gating voltage is absent or incorrect, proceed as in *c* below. If the pulses are missing, check for an output at pin 5 of XV15 (figs. 135(3) and 164(2)). If the pulses are present, check CR6 (fig. 135(1)). If the pulses are not present, check V16.

c. Target Comparator Check. If the pulses are present at pin 3 of XV16 but the gating voltage is missing or incorrect, check at pin 6 of XV9 (fig. 135(2) and 164(2)). If the output is present, check V16. If the output is missing or incorrect, check for gate open and gate close pulses at E2 and E1 (figs. 135(4) and 159(10)), respectively. If both pulses are present, check V9. If the gate open pulse is missing, proceed as in *d* below. If both pulses are missing, pro-

ceed as in *c* below. If the gate close pulse is missing, check at pin 4 of T2 (figs. 135(4) and 164(2)). If the pulse is present, check CR8 (fig. 135(4)). If the pulse is missing at pin 4 of T2, check the output at pin 1 of XV7 (figs. 135(3) and 164(2)). If the output is present, check V7B and the associated circuitry. If the output is missing, check the output at TP2 (figs. 135(5) and 164(2)). If the output at TP2 is present, check V7A and the associated circuitry. If the output is missing at TP2, check the sweep generator output at TP1 (figs. 135(5) and 164(2)) and the target voltage at pin 3 of Z2 (fig. 135(6)). Target voltage under test conditions should be zero. If the output at TP1 and the target voltage are both correct, check V4, V5, V6, and associated circuitry. If the waveform at TP2 is incorrect, check for proper setting of ZERO SET control R30 (step 10 of table IV) and target delay control C46 (step 14 of table IV). If these controls are set properly, check CR1 and CR2 (figs. 135(1) and 135(2)) in the feedback circuit.

d. Reference Comparator Check. The reference comparator is identical to the target comparator except for the reference designations of the components (fig. 164). Follow the same procedure as in *c* above, using the appropriate test points in the reference comparator if the gate open pulse is missing when the check is made at E2. The reference voltage should be -50 volts when measured at pin 1 of Z3. (OPR-ADJ switch S1 must be in the ADJ position when this measurement is made.)

e. Sweep Generator Check. If no output is present at TP1, check at pin 1 of XV14 and pin 8 of XV17 (fig. 135(2) and (3)). If the output is present at pin 8 of XV17 but not at pin 1 of XV14, check C32 and R117. If both outputs are present, check for the output at pin 7 of XV14 (fig. 135(2)). If output is present at pin 7 of XV14, check V1, V2, V3 (fig. 135), and associated circuitry (fig. 164). Also check Z1 and the positive reference voltage. If output is not present at pin 7 of XV14, check V14 (fig. 164). If there is no output at pin 8 of XV17, check for output at pin 6 of XV10 (figs. 164 and 135(3)). If output is present at pin 6 of XV10, check V17 (fig. 164(2)). If no output is present at pin 6 of XV17, check for the encoder reset and start pulses at pins 3 and 8, respectively, of XV10. If either or both inputs are present, check V10. If

either or both are missing, refer to step 12 of table VII.

f. Binary Counter Check. If the check outlined in *a* above indicates that the trouble is in the binary counter, make the checks outlined in steps 14 and 15 of table VII. Steps 14 and 15 of table VII do not test the counting capabilities of the binary counter. If the checks made in steps 14 and 15 reveal no malfunctioning of the binary counters and the binary count is still incorrect, proceed as follows. If no count is recorded, check the first binary counter (J44A and J31, par. 203). If there is a count but it is incorrect, check the appropriate K and L or C packages if the count is incorrect in such a manner to make the trouble evident. If the malfunctioning package is not evident, check all the K packages and their associated L or C packages.

206. Decoder

(fig. 135)

Before troubleshooting the decoder, make the following check: set REC LINE switch on the test panel at LOCAL. Place one or more of the parallax keys on the receiver unit in the 1 (up) position and press the MS switch. Observe the data lockup indicator lights with the receiver in continuous operation. The data lockup lights should be ON for each parallax key in the 1 position. If the data lockup lights are ON, the information is being applied to the data relays in the decoder. Always check the data lockup lights prior to troubleshooting the decoder.

a. Connect an oscilloscope between TP1 on the decoder and ground. This is the H output. Place H parallax switch No. 10 in the 1 (up) position. Ground the oscilloscope input lead to get a zero reference point. Set up the oscilloscope to view a full frame. Set the LOCAL-EXT switch in the EXT position. The decoder output should read $0 \pm .08$ volt. If this reading is incorrect, proceed as in *b* below. If the reading is correct, proceed as follows.

- (1) Starting with the oscilloscope sensitivity in the most sensitive position and with H parallax switch No. 10 in the 1 (up) position, start with H parallax switch No. 1 and turn each of the parallax switches to their 1 (up) positions and then back to their 0 (down) positions one at a time.

- (2) The dc level should change by .0975 volt times the binary equivalent of the switch thrown. That is, the first switch should change the dc level by .0975 volt, the second switch by twice .0975 volt, the third switch by four times .0975 volt, the fourth switch by eight times .0975 volt, etc. (The sensitivity of the oscilloscope needs to be changed in order to measure these different levels.) If the level changes correctly each time a switch is thrown, the decoder is functioning properly. If one or more, but not all, of the switches fails to change the level, proceed as in *b* below.

b. If the dc level is incorrect when switch 10 is placed in the 1 (up) position or if one or more of the other switches fails to change the dc level, proceed as follows.

- (1) Place the oscilloscope at pin 8 of Z1. Put the oscilloscope on an ac measurement as the dc level here does not permit measurement of small changes in voltage. Set the oscilloscope to measure at least one frame. Set all parallax switches at 0 (down).
- (2) Place each of the H parallax switches, one at a time, in their 1 (up) positions and then back to their 0 (down) positions. If one of the H parallax switches fails to change the voltage level, check the associated relay (K4 through K13) and the associated 4,700-ohm resistors (R59 through R78). If the waveform at pin 8 of Z1 (figs. 166 and 136(5)) is incorrect, check the reference voltage and the data lockup circuit (step 33 of table VII).
- (3) If the waveform is correct at pin 8 of Z1 (waveform shown with switch No. 10 of H, X, and Y parallax in the 1 (up) position), check at pin 3 of V1 (fig. 136(3)). (The oscilloscope sensitivity may have to be changed to obtain this waveform.)
- (4) If the waveform at pin 3 of V1 is incorrect, check Z1 and R47. If the waveform at pin 3 of V1 is correct, check at pin 1 of V3.
- (5) If the waveform at pin 1 of V3 is incorrect, check V1, V2, V3, and the associated circuitry. If the waveform at pin

1 of V3 is correct, check at pin 2 of V4A (fig. 136(3)). (Since this is only the H input of the storage amplifier, that part of the waveform dealing with X and Y is missing.) If the waveform at pin 2 of V4A is incorrect, check S1A, K1, and the associated circuitry.

- (6) If the waveform at pin 2 of V4A is correct, check at J1-16 as outlined in *a* above. If the dc level at J1-16 is incorrect, check R22, V4A, K15, and the associated circuitry.

c. Check the X and Y outputs as outlined in *a* and *b* above, using X and Y parallax switches, respectively, and check the appropriate storage amplifiers and relays. These components and their reference designations are shown in figure 173.

207. Modulator

The modulator can be removed from the transmitter unit and operated at a test position near the data set cabinet. To do this, remove the four nuts and washers holding the modulator in place. Pull the modulator out of its jack and put it in a place convenient for working (not more than 6 feet from the transmitter unit). Use the adapter cable found coiled at the rear inside of the cabinet (fig. 160). Plug one end of the cable into the transmitter jack formerly occupied by the modulator and plug the other end into the jack on the modulator. Standard troubleshooting techniques can be performed with the use of the schematic (fig. 168), and the component location illustrations (figs. 140(3) and 148). Also refer to step 23 of table VII.

208. Low Voltage Power Supply

(fig. 181)

The low voltage power supply can be bench tested independently of other units of the data set. These bench tests are needed if trouble in the units cannot be determined by usual troubleshooting techniques. Voltage and resistance measurements at tube pins are shown in figure 183. Component locations are shown in figure 152. The schematic diagram is figure 181. The power supply is shown as a part of the power supply functional drawing (fig. 208). The bench testing setup and list of material are given in *a* below and figure 157. The test requirements for the power supplies and directions for using the

bench testing setup are given in b(1) through b(6) below.

a. Equipment Required for Testing and Troubleshooting.

Item	Test equipment
1-----	Ac input supply 105 to 130 volts, 3.5 amperes, 60 cycles.
2-----	Power supply PP-2236/G or equivalent.
3-----	Powerstat, 58 to 62 cycles.
4-----	VTVM (ac) (peak-to-peak).
5-----	Volt-ohm-milliammeter 20,000-ohms-per-volt.
6-----	0-7.5-volt and 0-30-volt dc voltmeter, 2% accuracy.
7-----	C1, capacitor, 1 uf, 200 VDCW.
8-----	CR1, rectifier, 1N93 germanium.
9-----	P1, connector, SM-C-190335.
10-----	P2, connector, SM-C-190335.
11-----	M1, 0-15 ma dc milliammeter, 2% accuracy.
12-----	M2, 0-100 ma dc milliammeter, 2% accuracy.
13-----	M3, 0-5 ampere dc ammeter, 2% accuracy.
14-----	R1, resistor, 15,000 ohms $\pm 5\%$, 4 watts.
15-----	R2, rheostat, 10,000 ohms, 4 watts.
16-----	R3, rheostat, 25 ohms, 4 watts.
17-----	R4, rheostat, 50 ohms, 50 watts.
18-----	R5, resistor, 1 megohm $\pm 5\%$, 1 watt.
19-----	R6, resistor, 2.15 ohms, 25 watts.
20-----	S3, switch, SPDT.

b. Operational Tests. These tests consist of measuring the ac, dc, and ripple voltage.

Note. Before making these tests, disconnect the power supply from all power, and check the following resistances, using the meter, item 5.

From connector—	To connector—	Ohms $\pm 15\%$
*J1 terminal J-----	J1 terminal S-----	100.
J1 terminal J-----	J1 terminal H-----	115K.
J1 terminal J-----	J1 terminal E-----	100K.
J1 terminal A-----	J1 terminal B-----	8K.
J1 terminal M-----	Terminal 5 of relay K1-	250.

*For this measurement connect the positive terminal of the meter to the terminal shown in the "From connector" column.

(1) *Pretest setup and adjustments* (fig. 158).

- Connect items 3, 7, 8, and 11 through 20 as shown in figure 158.
- Connect items 9 and 10 to connectors J1 and J2, respectively, of the power supply being tested.
- Apply 115 volts $\pm 5\%$, 60 cycles.
- Operate the +4.5V & -20V SUP switch to ON. The +4.5V & -20V PWR lamp I1 should light.

Note. The neon lamps on the front panel fuse holders should not light. If lamps light, replace the associated fuse.

- Adjust the 25-ohm rheostat, item 16, for a reading of 600 milliamperes on meters M2, item 12.
- Adjust the 50-ohm rheostat, item 17, for a reading of 2.1 amperes on M3, item 13.
- After making the above adjustments, allow the power supply to warm up for 10 minutes before making voltage measurements.

(2) *Voltage measurements, +4.5-volt dc regulated output.*

- Adjust the ac input voltage to 117 volts.
- Adjust the 25-ohm rheostat, item 16, for a reading of 600 milliamperes on M2, item 12.
- Make voltage measurements as shown in chart below, using the 0-7.5 volt scale of item 6, and item 4 for ac ripple.

4.5-volt Regulated Output

Ac input (volts)	Output taken at test connector P1 terminals	Output load (ma) (adjust item 16)	Dc output (volts)	Max. ripple peak-to-peak (mv)
105	R and S----	600	4.25 min----	60
130	R and S----	250	4.75 max----	50

(3) *Voltage measurements, -20-volt dc regulated output.*

- Adjust the ac input voltage to 117 volts.
- Adjust the 50-ohm rheostat, item 17, for a load of 2.1 amperes on M3, item 13.
- Make voltage measurements as shown in the chart below, using the 0-30-volt scale of item 6, and item 4 for ac ripple.

-20-volt Regulated Output

Ac input (volts)	Output taken at test connector P1 terminals	Output load (amps) (adjust item 16)	Dc output (volts)	Max. ripple peak-to-peak (mv)
105	M and R---	2.1	18.4 min----	250
130	M and P---	0.75	21.7 max----	200

(4) *Voltage measurements, -70-volt lamp supply output.*

- Adjust the ac input voltage to 117 volts.
- Connect the volt-ohm-milliammeter, item 5, as shown in figure 158.

- (c) Connect the VTVM (ac) (peak-to-peak), voltmeter, item 4, to terminals J and H of test connector P1.
 - (d) Operate switch S3, item 20, to OFF.
 - (e) Adjust the -70V SUP ADJ VOLTS control to obtain a plateau voltage of 79 volts on the meter, item 5.
 - (f) Measure the ac signal voltage on the VTVM (ac), item 4. It should be greater than 18 volts peak-to-peak.
 - (g) Adjust the ac input voltage to 105 volts and then to 130 volts. Measure the ac signal voltage on item 4 for each line voltage. The ac signal voltage should be greater than 18 volts for line voltages from 105 to 130 volts.
 - (h) Operate S3, item 20, to ON, and adjust the 10,000-ohm rheostat, item 15, for a reading of 13 ma on meter M1, item 11. (This corresponds to a peak current of 15 ma.) Measure the plateau voltage and the ac signal. The plateau voltage should be less than 82 volts, and the ac signal should be greater than 18 volts, peak-to-peak.
- (5) *Voltage measurements, 150-volt dc regulated output.*
- (a) Adjust the dc input voltage to $+300 \pm 3$ volts.
 - (b) Connect the meter, item 5, to terminals B and J of test connector P1, and measure the output voltage. It should be $+151 \pm 9$ volts.
- (6) *Voltage measurements, 6.4-volt ac outputs.*
- (a) Adjust the ac input voltage to 117 volts.
 - (b) Adjust item 16 for a current of 600 ma.
 - (c) Adjust item 17 for a current of 2.1 amperes.
 - (d) Using meter, item 5, check for $6.5 \pm .5$ volts ac between terminals C and D, E and F, H and J, and R and S of test connector P1.

209. High Voltage Power Supply

Under normal conditions no special maintenance of the high voltage power supply is required except for occasional electron tube replacements. Standard trouble shooting techniques can be performed with the use of the voltage and resistance chart (fig. 186), the schematic (fig. 184), and the component location drawings (fig. 134). This power supply is a part of the power supply functional drawing (fig. 208).

Warning: HIGH VOLTAGE is used in this component. DEATH ON CONTACT may result if personnel fails to observe safety precautions. When checking voltages shown on figure 186, observe the DO NOT MEASURE notations. Avoid contact with socket pins so marked.

Occasionally a type 5755 or 12AX7 tube in the dc amplifier is found which, when tapped, produces sudden changes in the dc output voltage or erratic operation. Tubes having this defect should be discarded. When either of these tubes is replaced, excessive drift of the dc output voltage may occur. This drift disappears after the first few hours of operation as the tubes age and their characteristics stabilize. In any case, after replacing any of these tubes, readjust the dc output voltages in accordance with table IV. A recheck of the dc output voltages after 10 to 20 hours of operation is recommended.

210. Waveforms

(figs. 159(1)-159(10))

Waveforms of the voltages appearing at terminals of the packages and of other important points of the data set are shown in figures 159(1) through 159(10). The waveforms illustrated are representative of typical circuits, but every waveform of every terminal of the packages is not shown. For example, a representative D package showing the output waveform for a typical package is shown, and it is understood that all other D packages having the same external circuits will have the same waveforms at the corresponding terminals. When checking a waveform at a terminal of a package not shown in the figure, refer to the package of the same kind which is shown and use the representative waveform illustrated.

Section V. REPAIRS

211. General Parts-Replacement Techniques

Because of the small size and close spacing of many of the parts of the data set, care must be used when replacing them. Careless replacement of parts makes new faults inevitable. Observe the following precautions and techniques.

a. When replacing diodes and transistors or parts located near them, use a small tipped, hot soldering iron. The iron must be hot enough to melt the solder quickly to prevent overheating the part. Always grasp the pigtail lead of the part with long-nosed pliers between the part and the point of soldering to absorb the heat. Do not hold the iron near the part long enough to heat it appreciably.

b. Before a part is unsoldered, note the position of the leads. If the part has a number of leads, tag each of the leads.

c. Be careful not to damage other leads by pulling or pushing them out of the way.

d. Do not allow drops of solder to fall into the data set; they may cause short circuits.

e. Make well soldered joints; a poorly soldered joint causes faulty operation and is very difficult to find.

212. Removal and Replacement of Units

Warning: It is recommended that two people be on hand while removing and replacing the units of the data set. Most of the units are heavy and dangerous to handle alone. Have one man hold the unit in place while the second man is removing or inserting the mounting screws.

a. *High Voltage Power Supply.*

(1) To remove the high voltage power supply from the rack:

(a) First disconnect the ac power at the source.

(b) Tag the nine wires on the terminal strip on the right hand side of the power supply panel. This will identify them when the unit is replaced.

(c) Remove the wires by removing the terminal screws. Be careful not to lose the screws.

(d) Remove the 10 screws at the ends of the panel holding the unit to the rack. Be careful not to lose the screws.

(e) Remove the unit by drawing it toward the front of the data set.

(2) To replace the high voltage power supply:

(a) Hold the unit in place and fasten it to the rack with the screws removed in (1)(d) above.

(b) Connect the nine wires to the terminal strip, observing the tags attached to the wires in (1)(b) above. Use the same screws that were removed in (1)(c) above to secure the wires to the terminal strip.

b. *All Other Units.*

(1) To remove any of the other units from the rack:

(a) Remove the connecting plug, or plugs, from the jacks on the chassis.

(b) Remove the unit by removing the mounting screws at each end of the panel, and drawing the unit toward the front of the data set. Be careful not to lose the screws.

(2) To replace a unit on the rack:

(a) Hold the unit in place and secure it to the rack by means of the screws removed in b(1)(b) above.

(b) Replace the plugs into the jacks, observing the chassis markings for correct mating.

213. Parts Identification

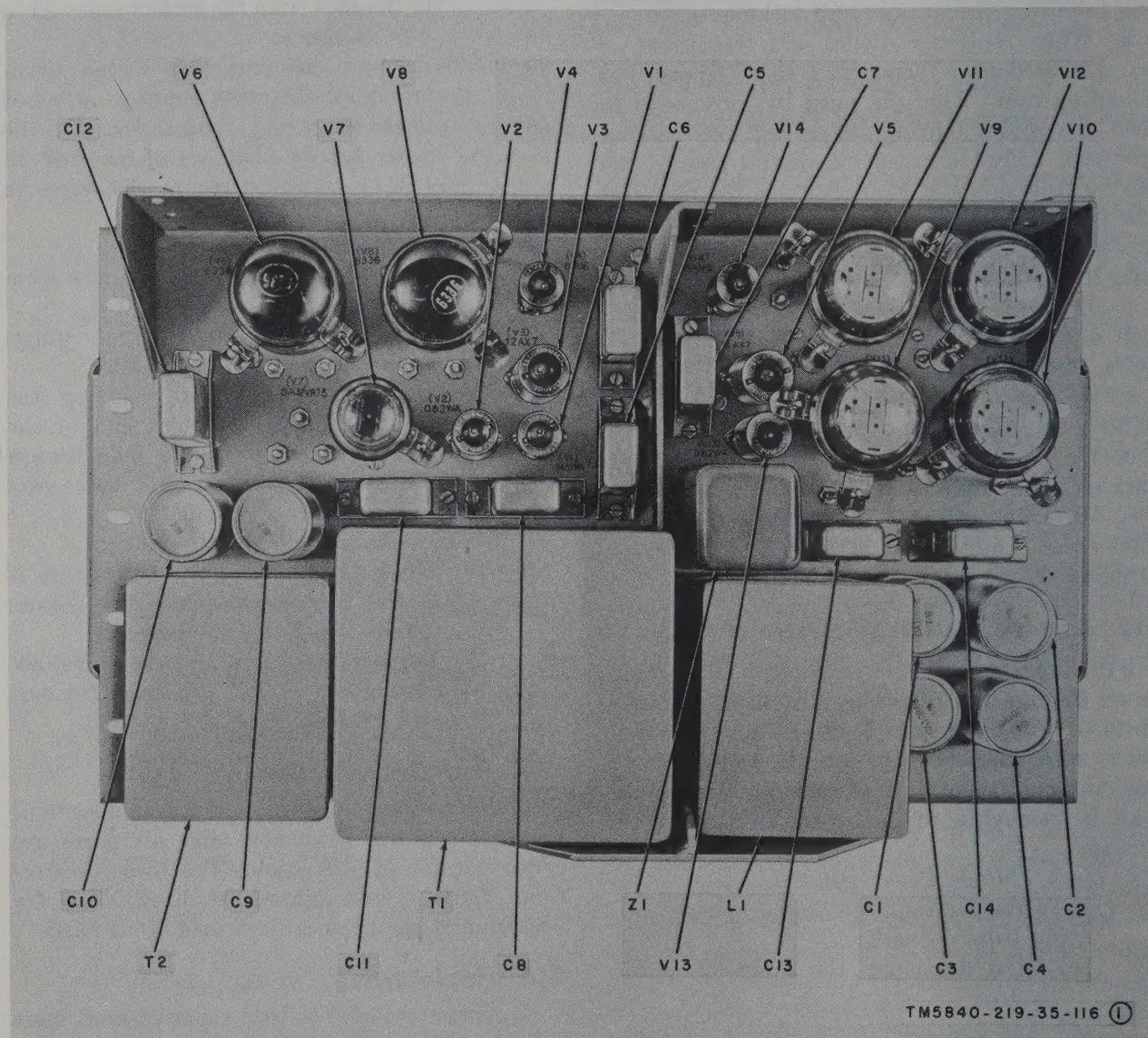
In this paragraph all units and components of the data set are illustrated and all parts are called out for identification. Use these illustrations, figure 1, and figures 134 through 157 for determining the physical locations of all parts.

214. Final Testing

Equipment which has been repaired must meet definite minimum performance standards before it is returned to service. The tests in table VII are designed to measure the performance capability of the repaired data set. Equipment which meets the minimum standards stated in the table will operate satisfactorily.

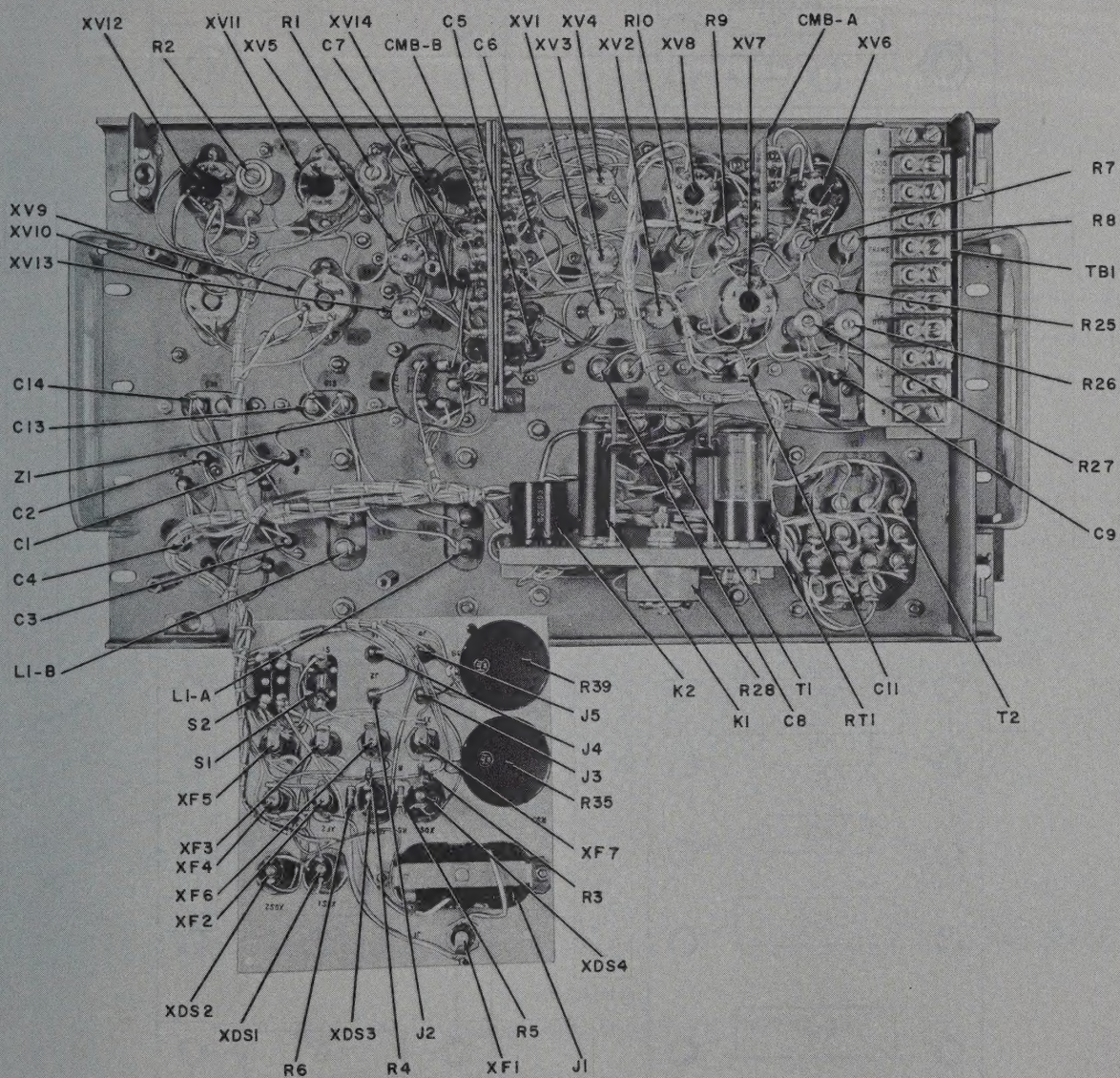
Figure 133. Package schematics.

(Contained in separate envelope)



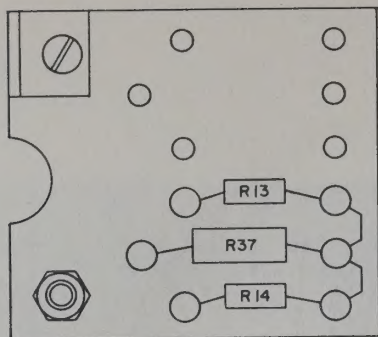
Parts location

Figure 134. Power supply PP-2236/G.

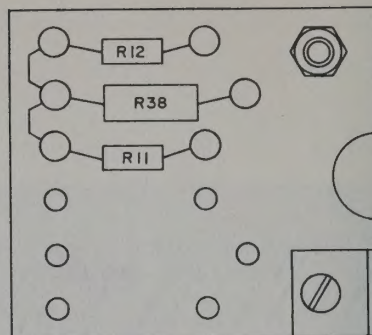


TM5840-219-35-116 (2)

Parts location
Figure 134—Continued.

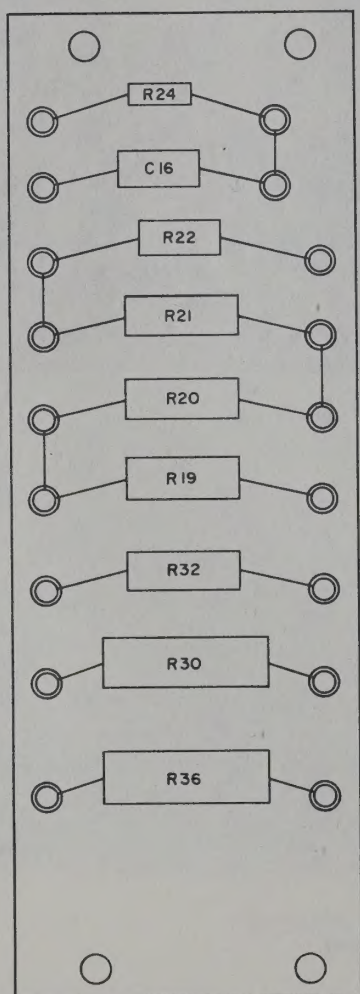


LEFT

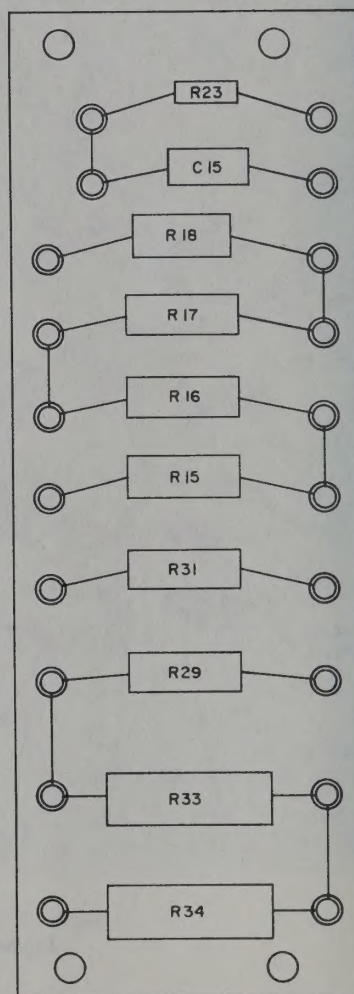


RIGHT

CMB-A



LEFT



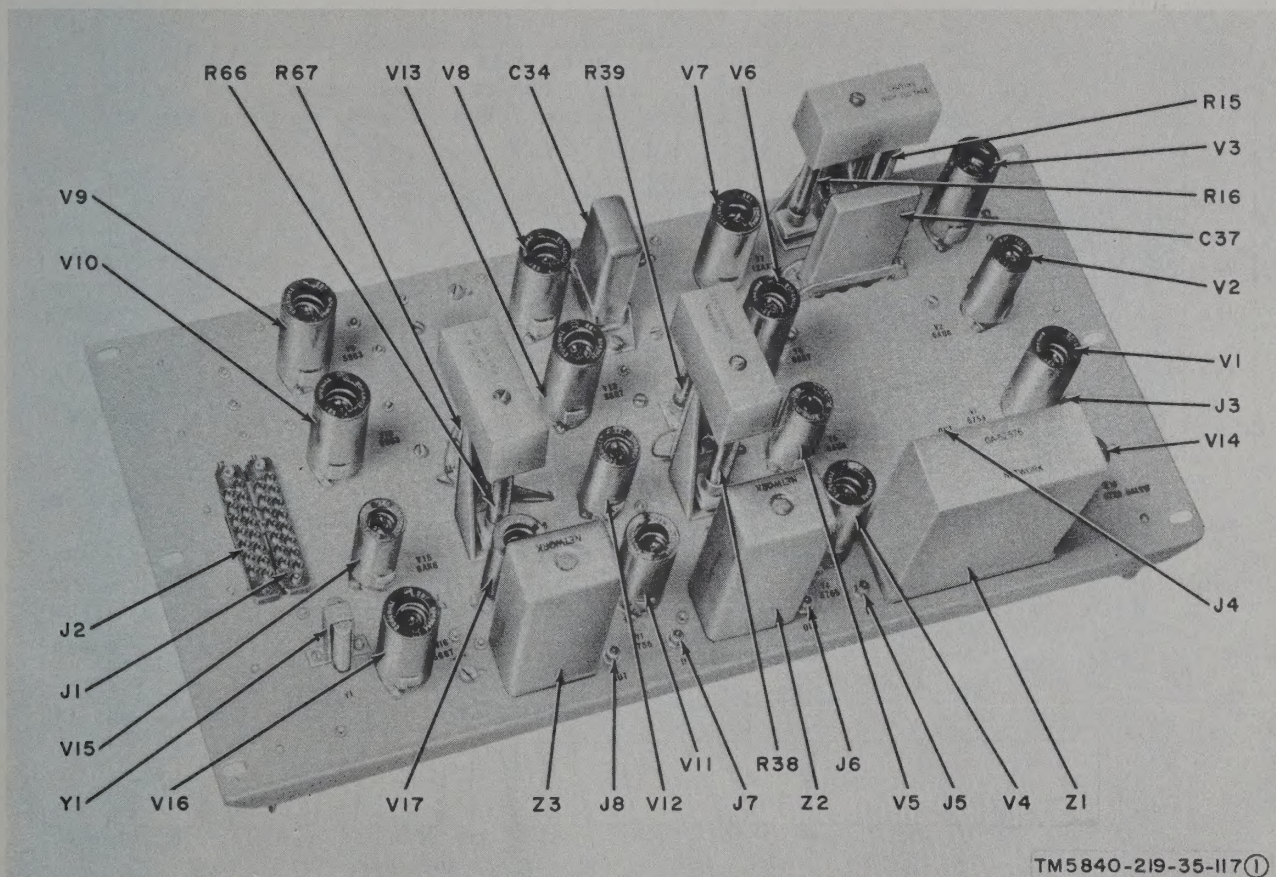
RIGHT

CMB-B

TM5840-219-35-116 (3)

Component boards

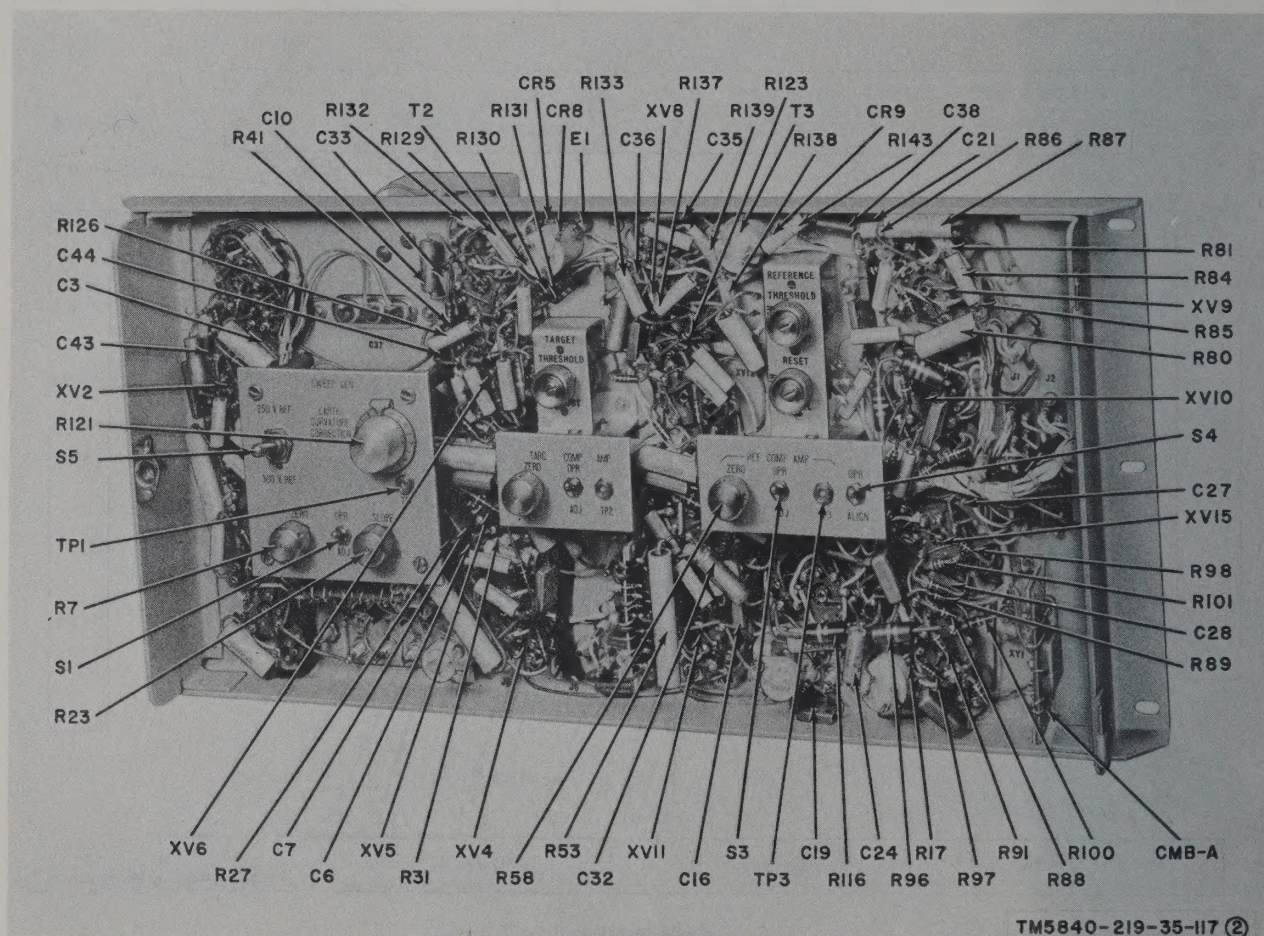
Figure 134—Continued.



TM5840-219-35-117①

Parts location

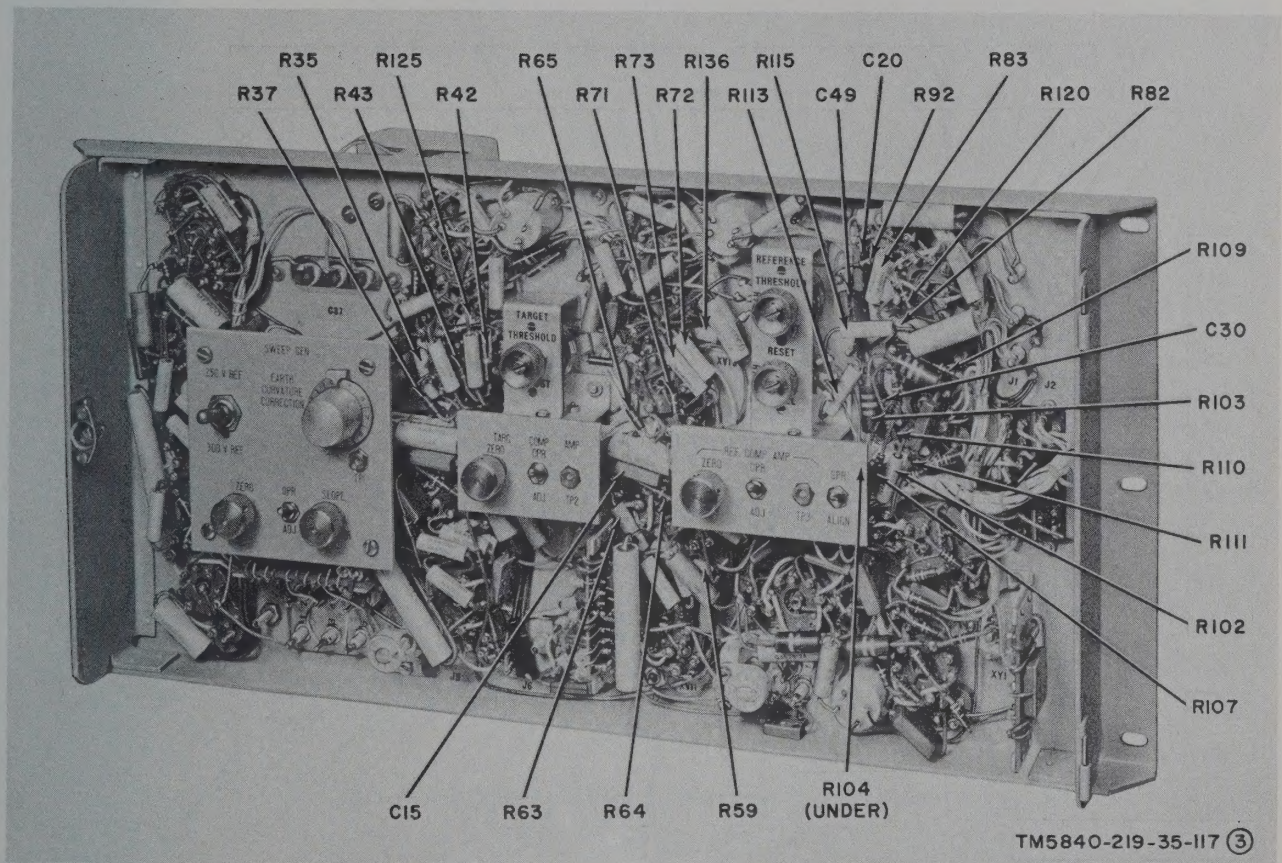
Figure 135.—Coordinate data encoder KY-278/TSQ-36.



TM5840-219-35-117 (2)

Parts location

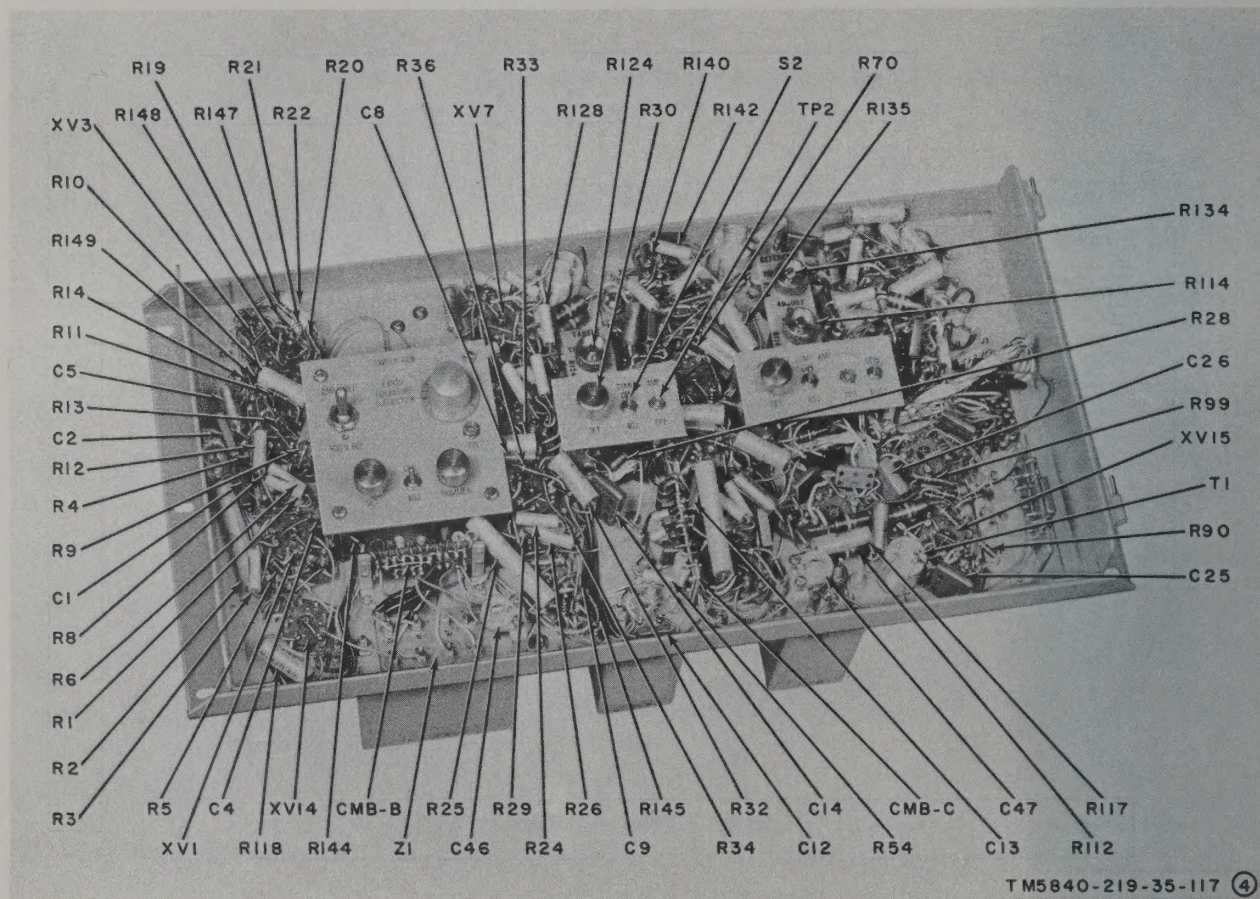
Figure 135—Continued.



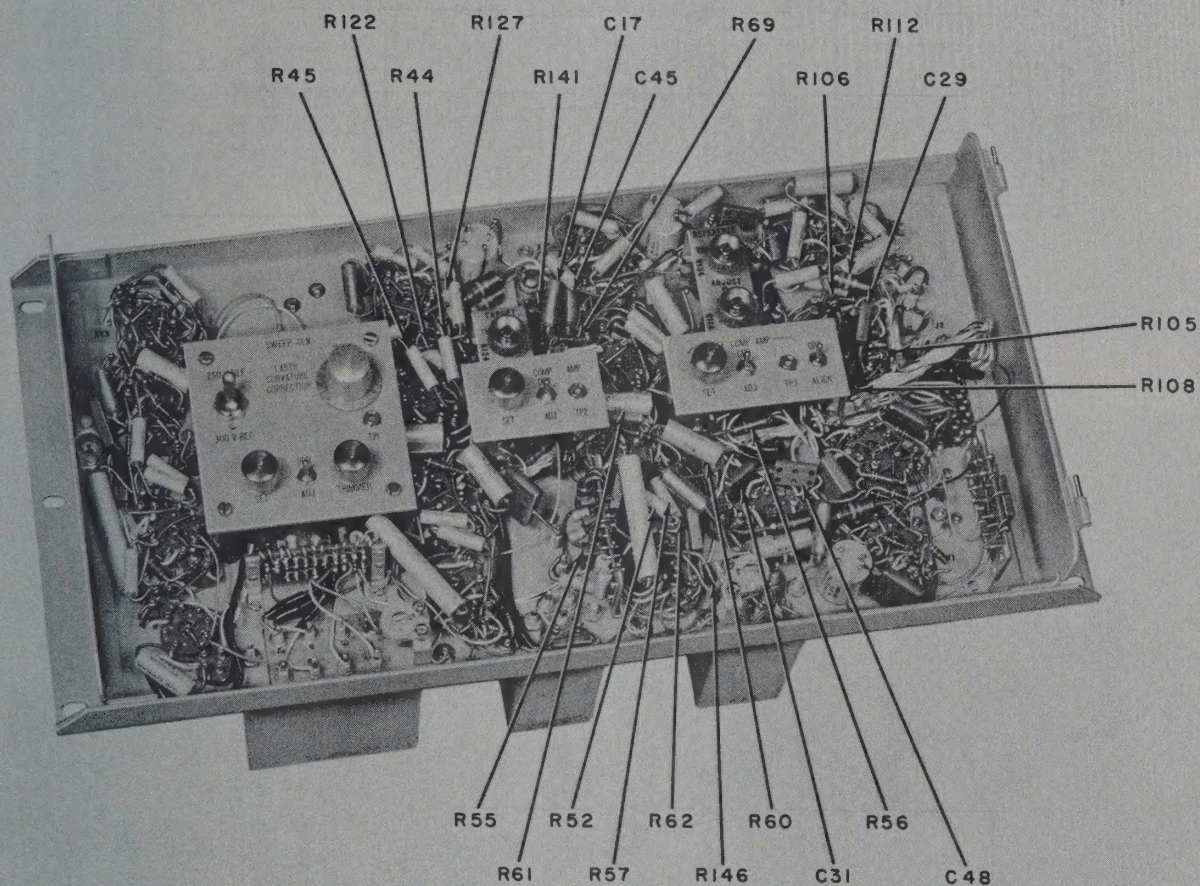
TM5840-219-35-117 ③

Parts location

Figure 135—Continued.



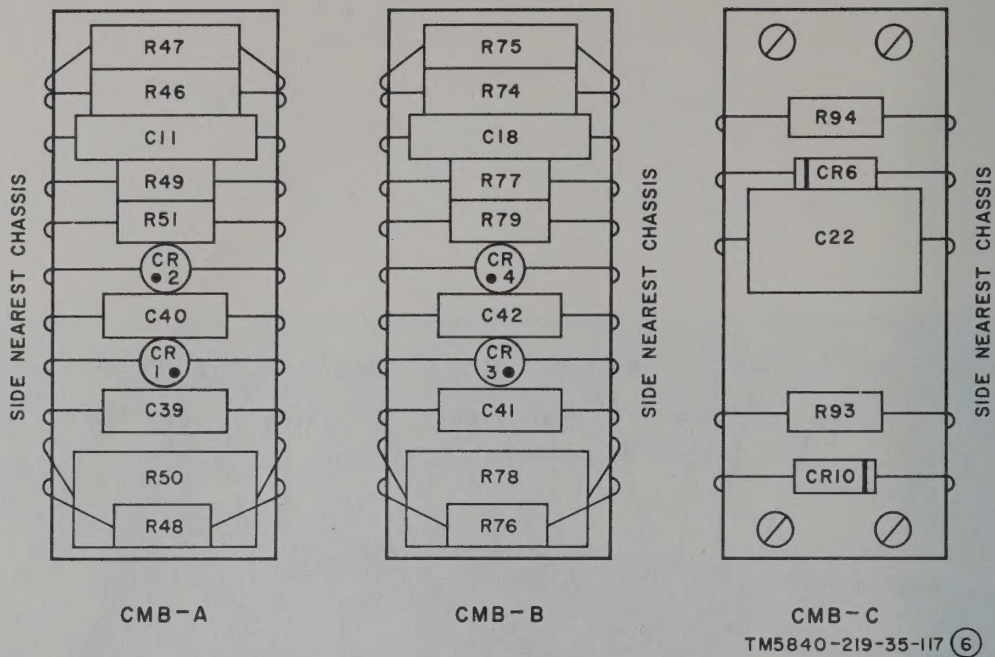
Parts location
Figure 135—Continued.



TM5840-219-35-117 (5)

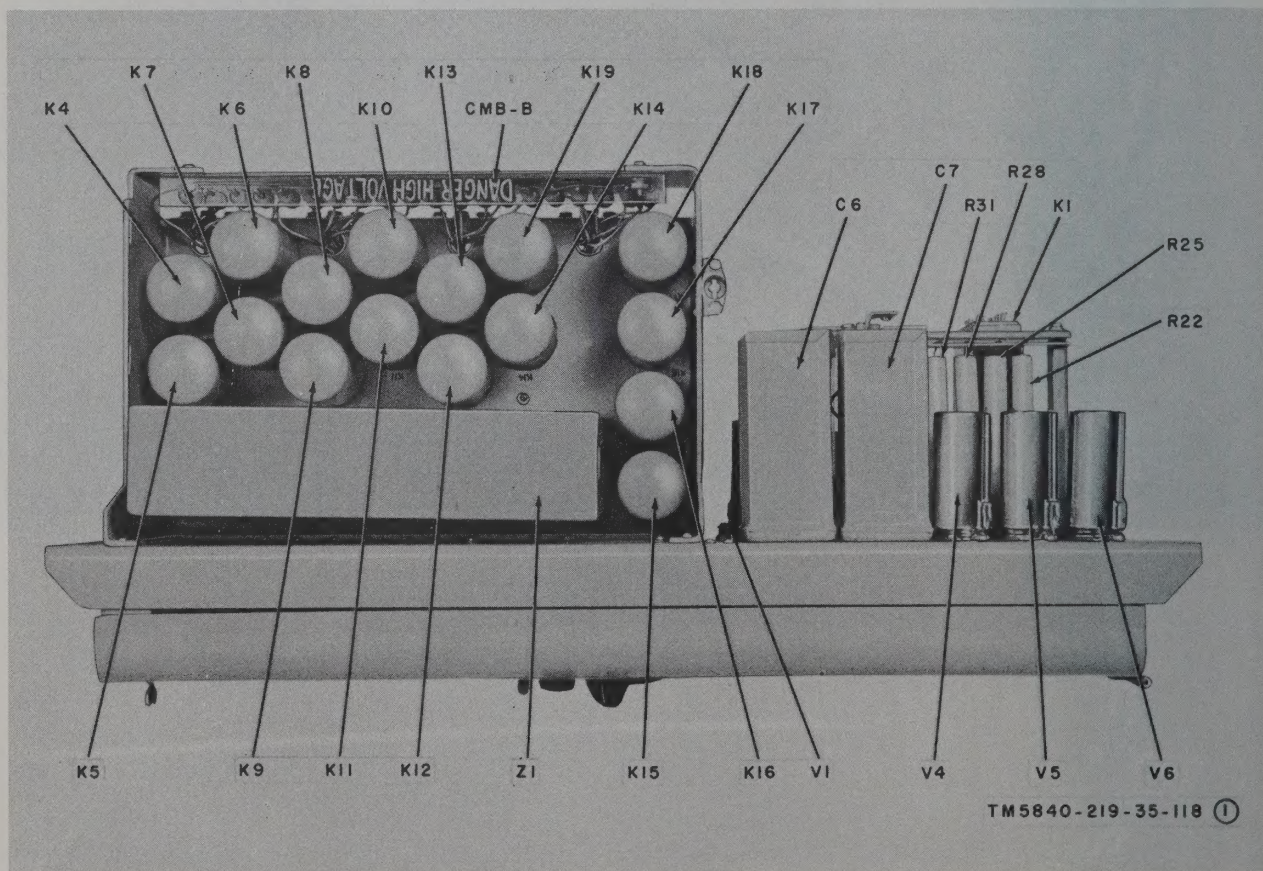
Parts location

Figure 135—Continued.



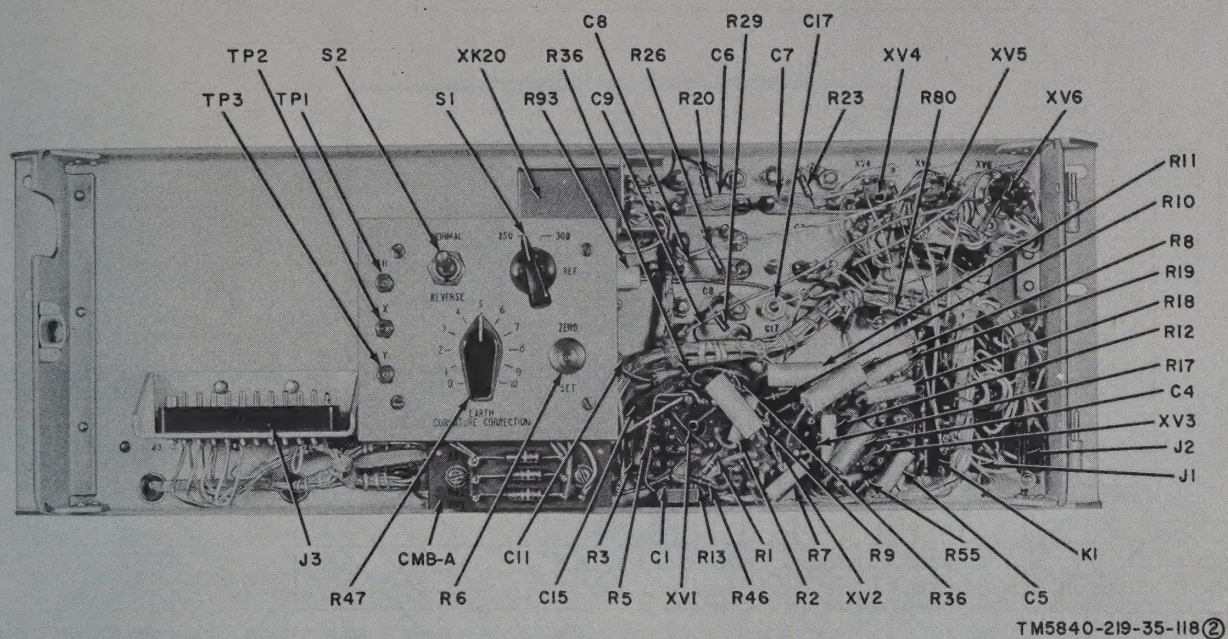
Component boards

Figure 135—Continued.



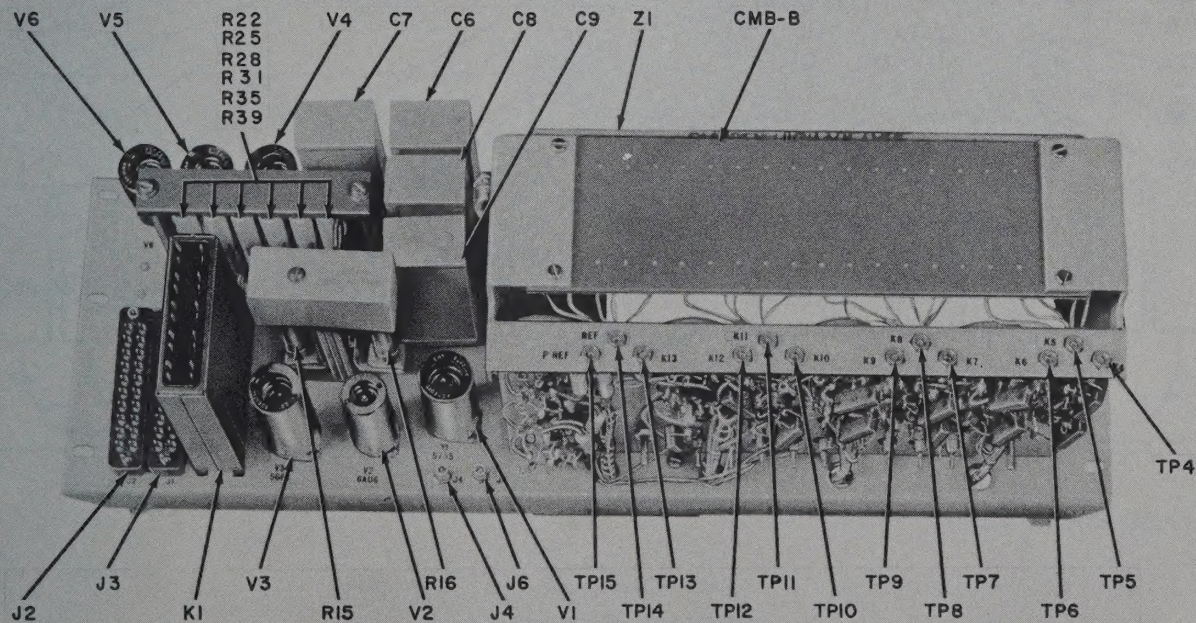
Parts location

Figure 136. Coordinate data decoder KY-277/TSQ-36.



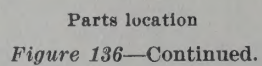
Parts location

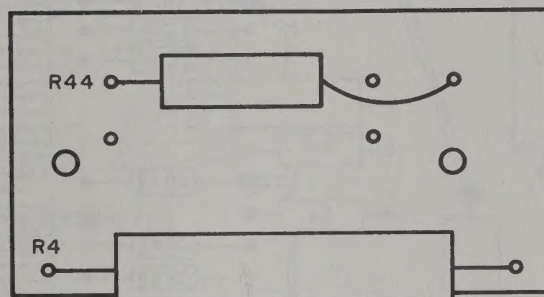
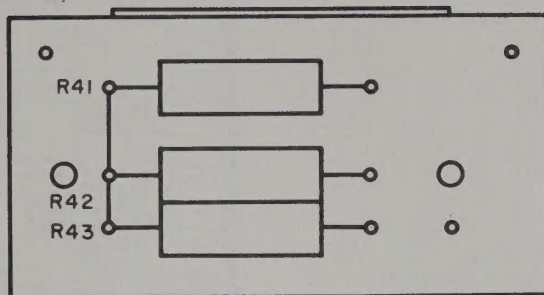
Figure 136—Continued.



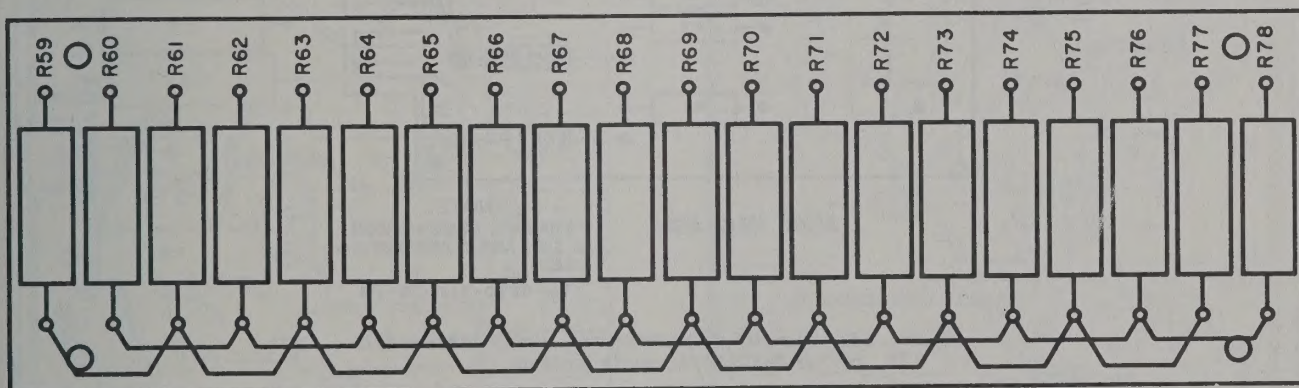
Parts location

Figure 136—Continued.





CMB-A

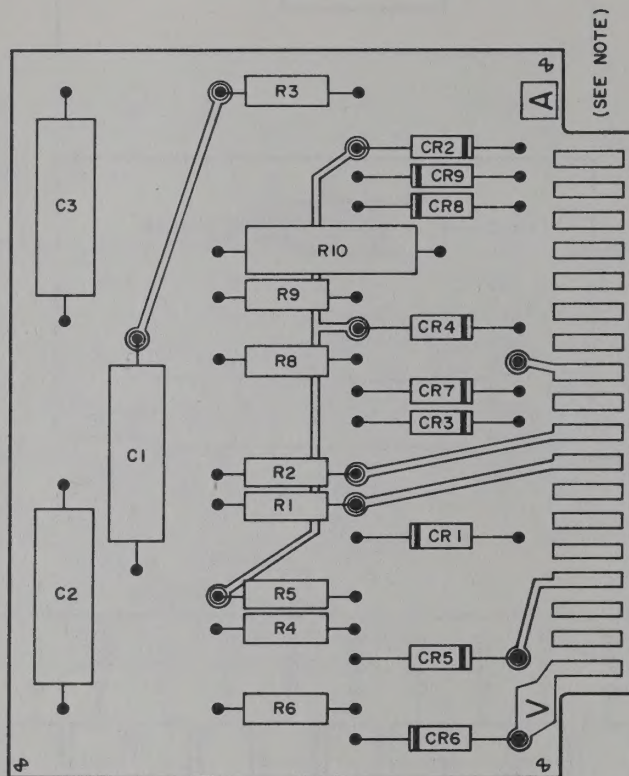


REAR

CMB-B

TM5840-219-35-118 (5)

Component boards
Figure 136—Continued.

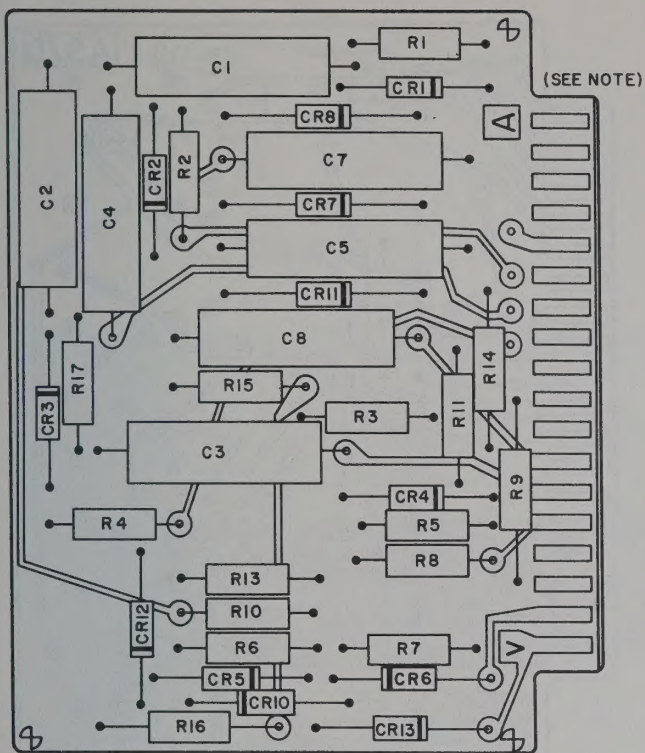


AS/A PACKAGE

NOTE:
TERMINAL DESIGNATIONS
G, I, O, AND Q ARE NOT
USED.

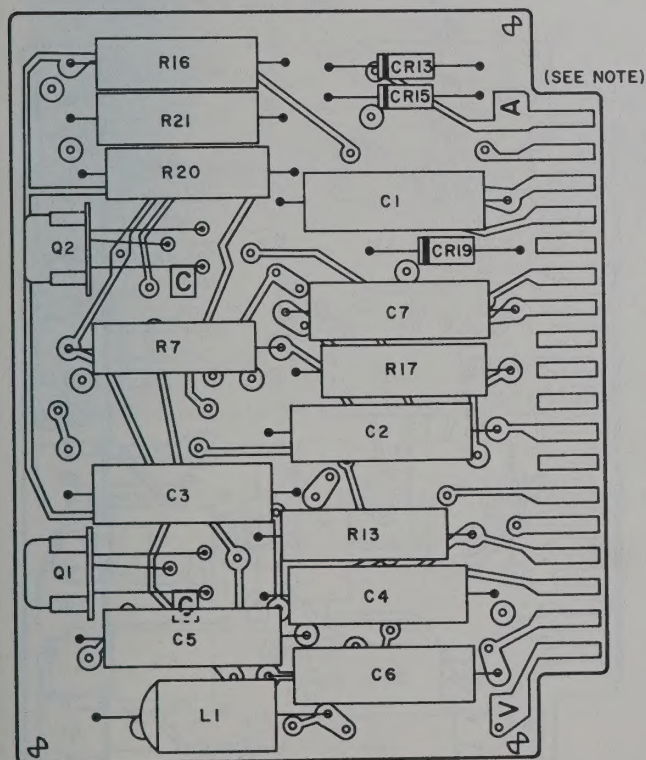
TM-5840-219-35-119

Figure 137. Amplifier-synchronizer unit subassembly
MX-2345A/G, parts location.

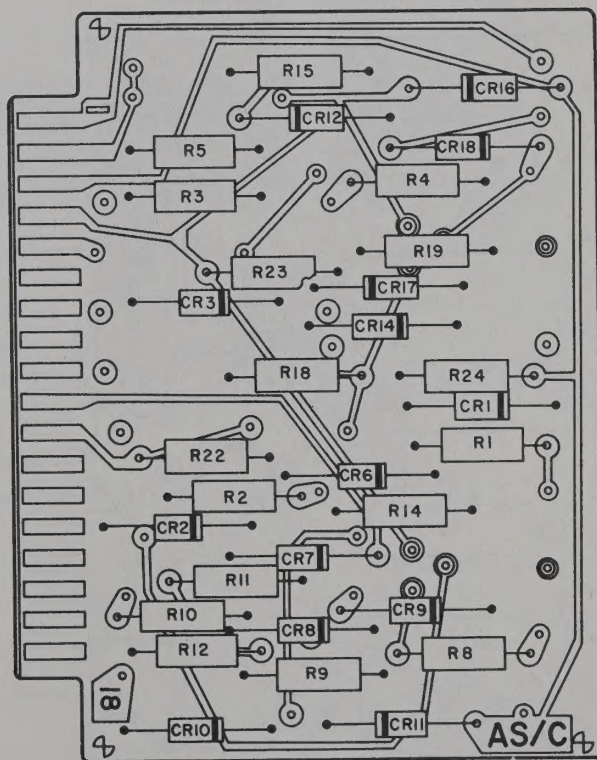


AS/B PACKAGE

NOTE:
TERMINAL DESIGNATIONS G, I, O,
AND Q ARE NOT USED.

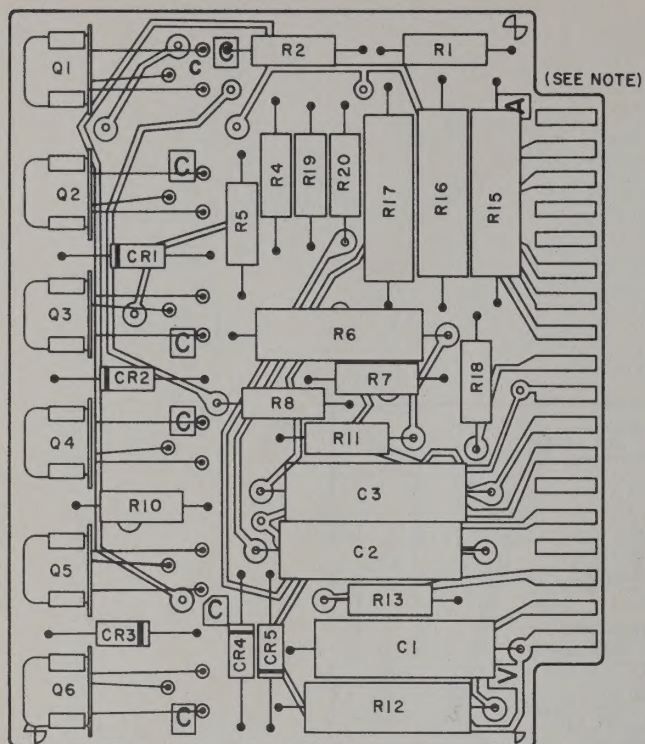


AS/C PACKAGE

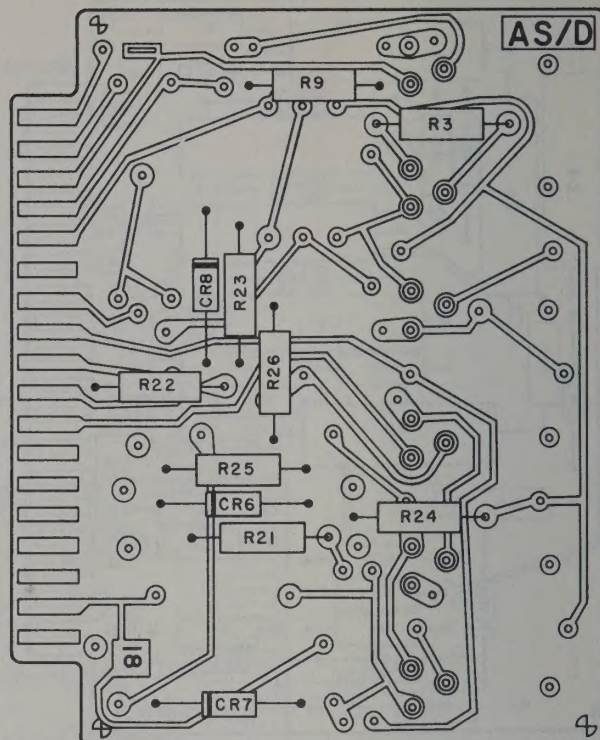


TM 5840-219-35-120

Figure 138. Amplifier-synchronizer unit subassemblies MX-2346A/G and MX-2347A/G, parts location.

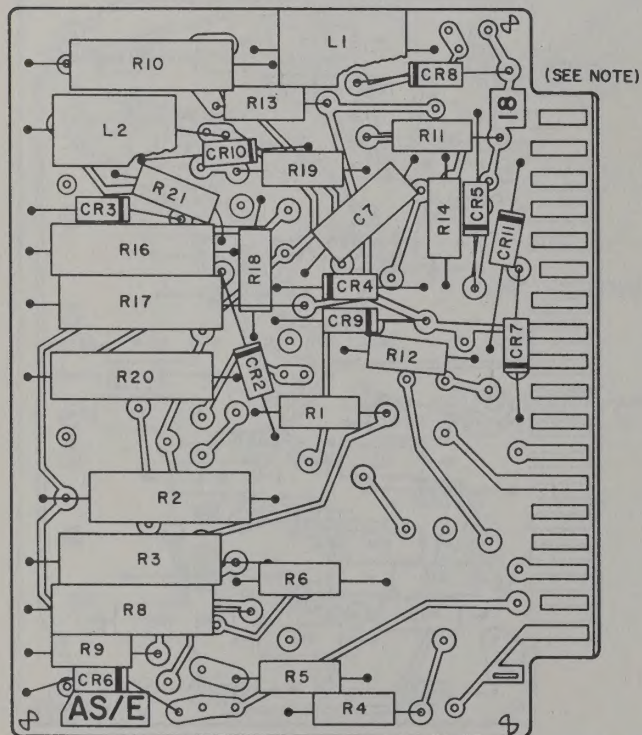


AS/D PACKAGE

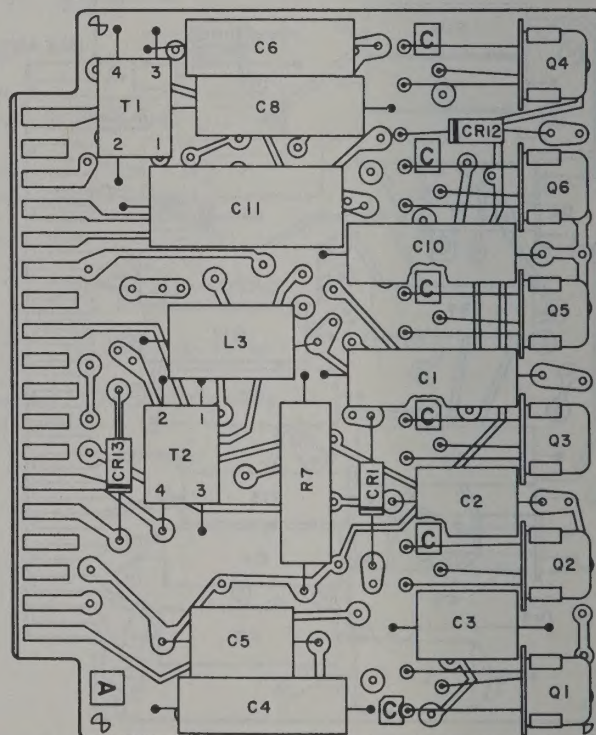


NOTE:

TERMINAL DESIGNATIONS G, I, O,
AND Q ARE NOT USED.

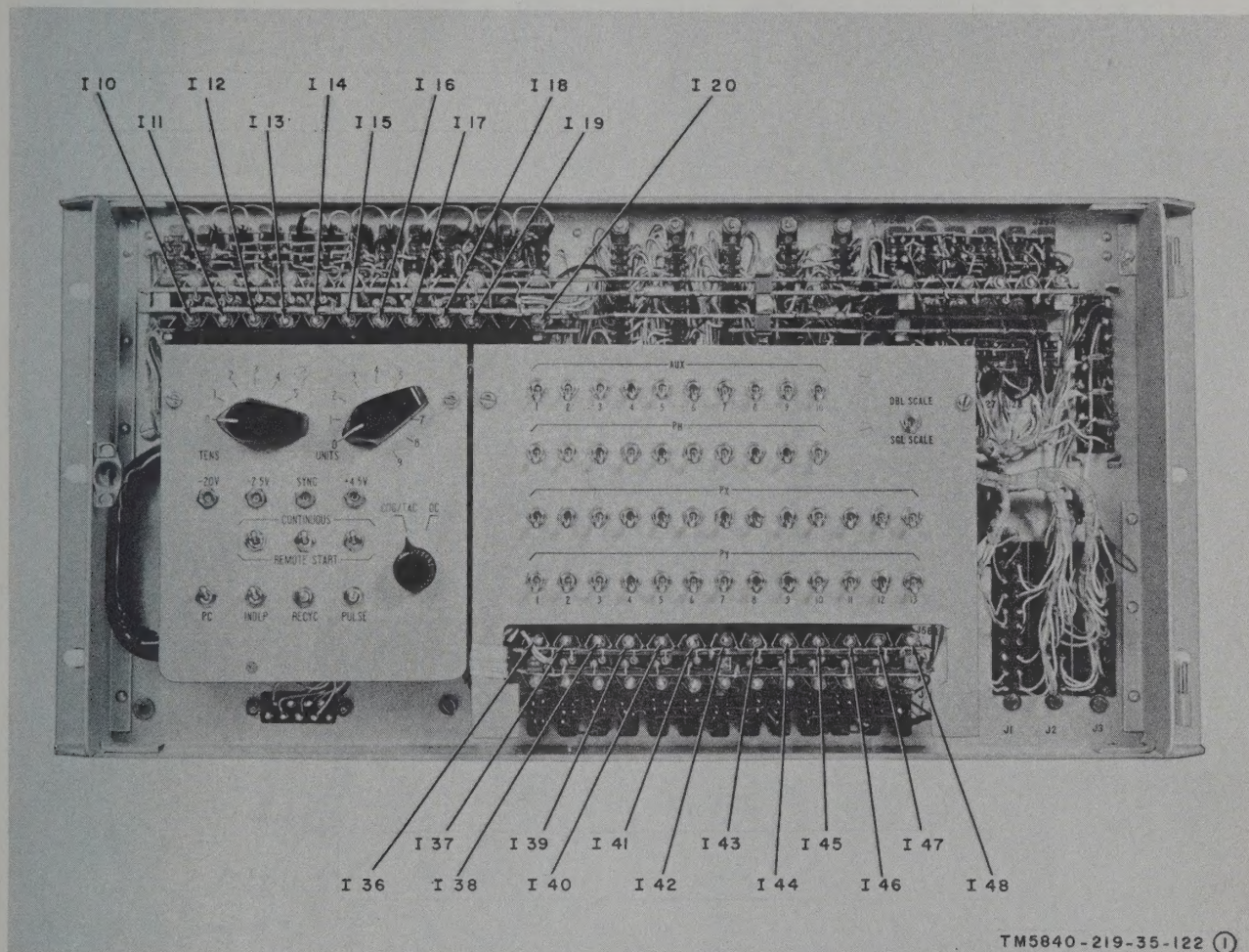


AS/E PACKAGE



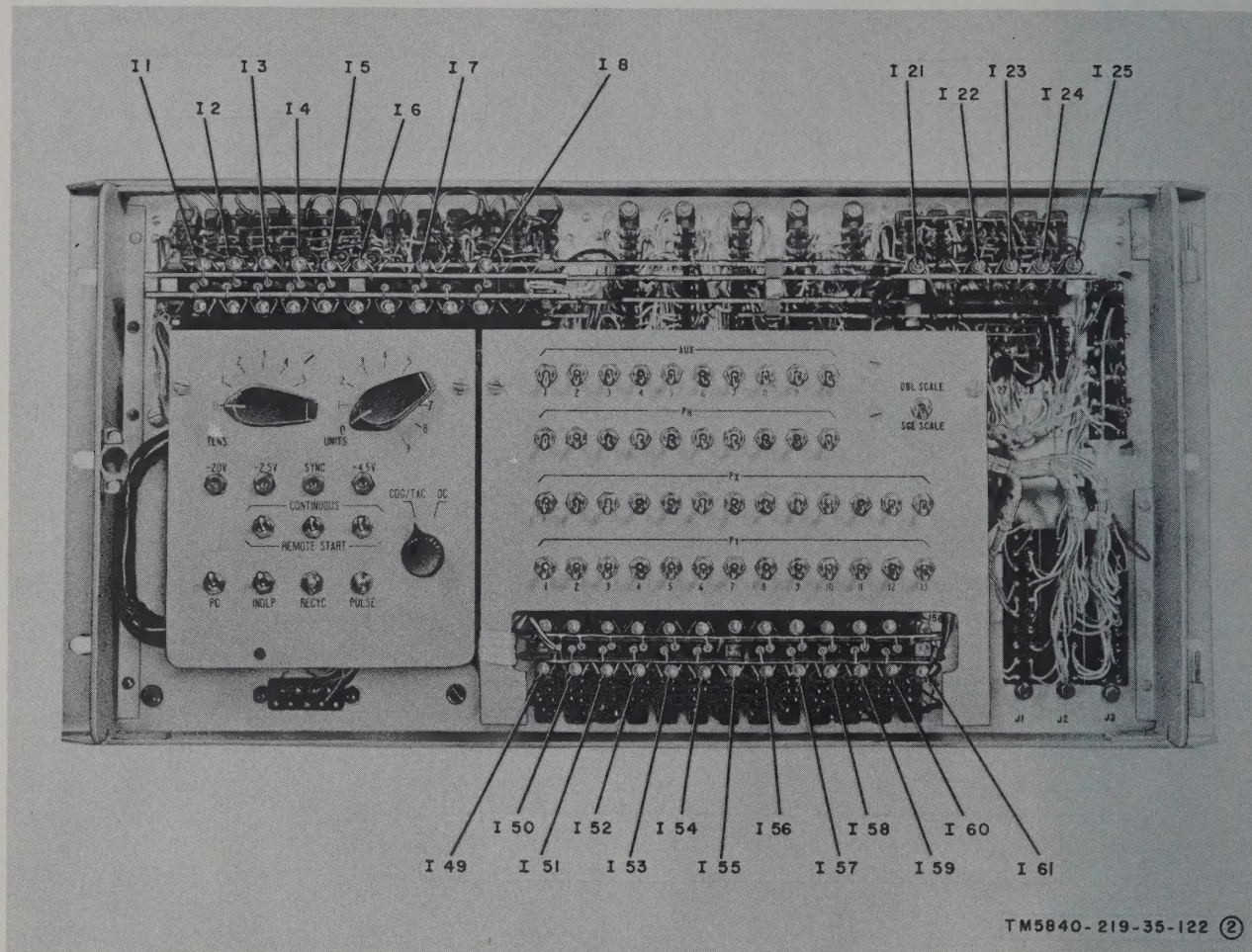
TM 5840-219-35-121

Figure 139. Amplifier-synchronizer unit subassemblies MX-2348A/G and MX-2349A/G, parts location.



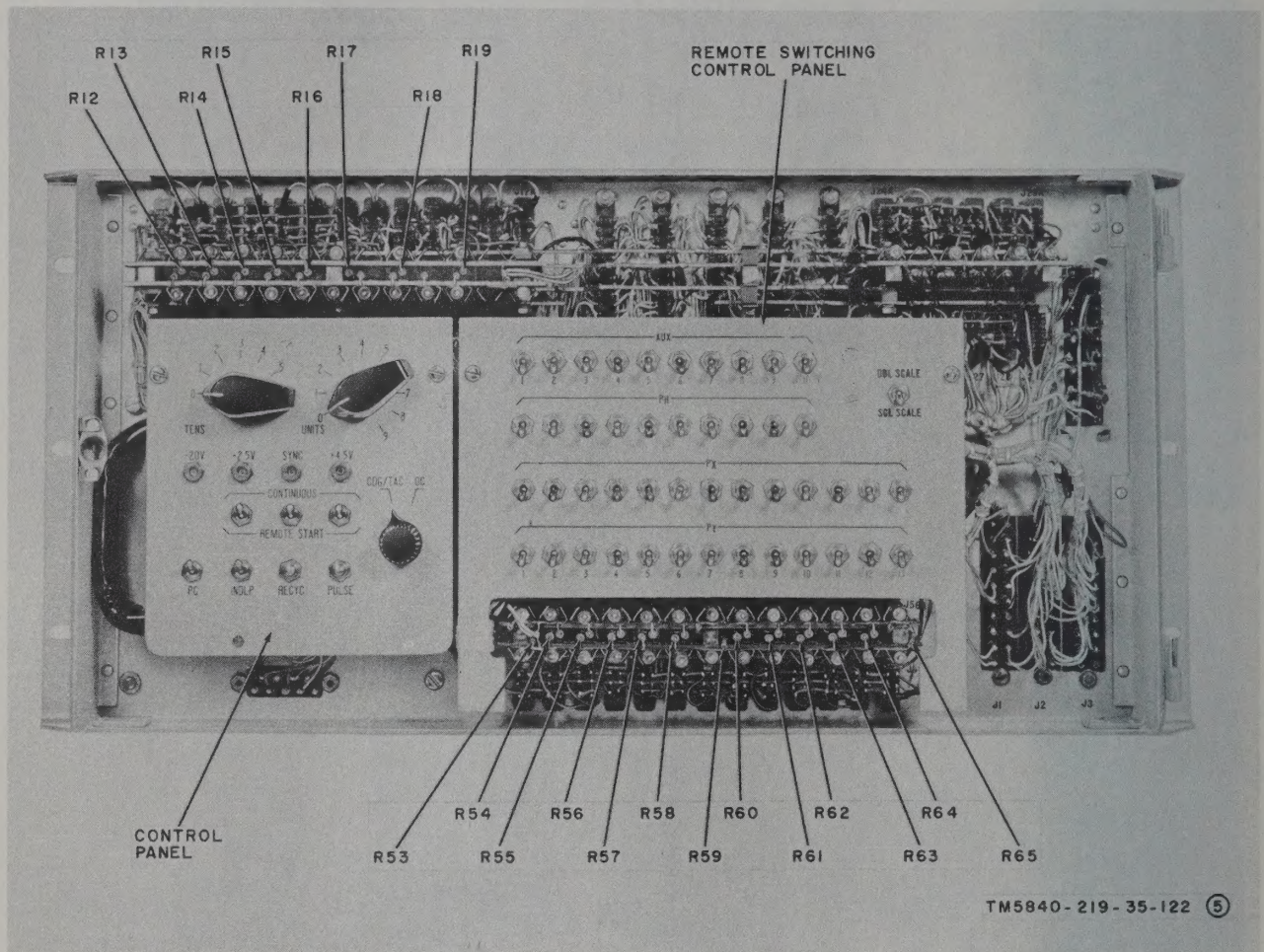
Parts location

Figure 140. Coordinate data transmitter unit T-721/TSQ-36.

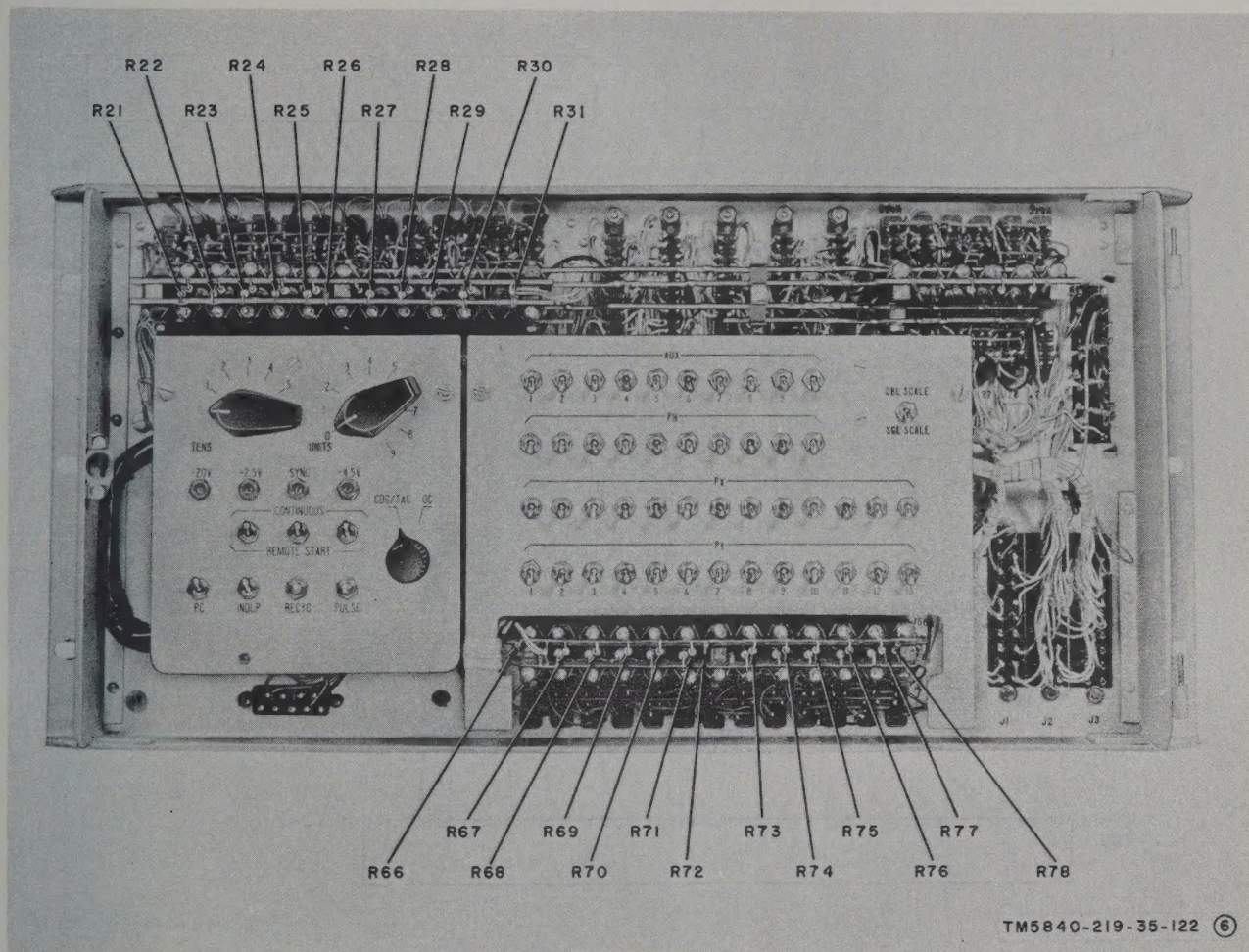


TM5840-219-35-122 (2)

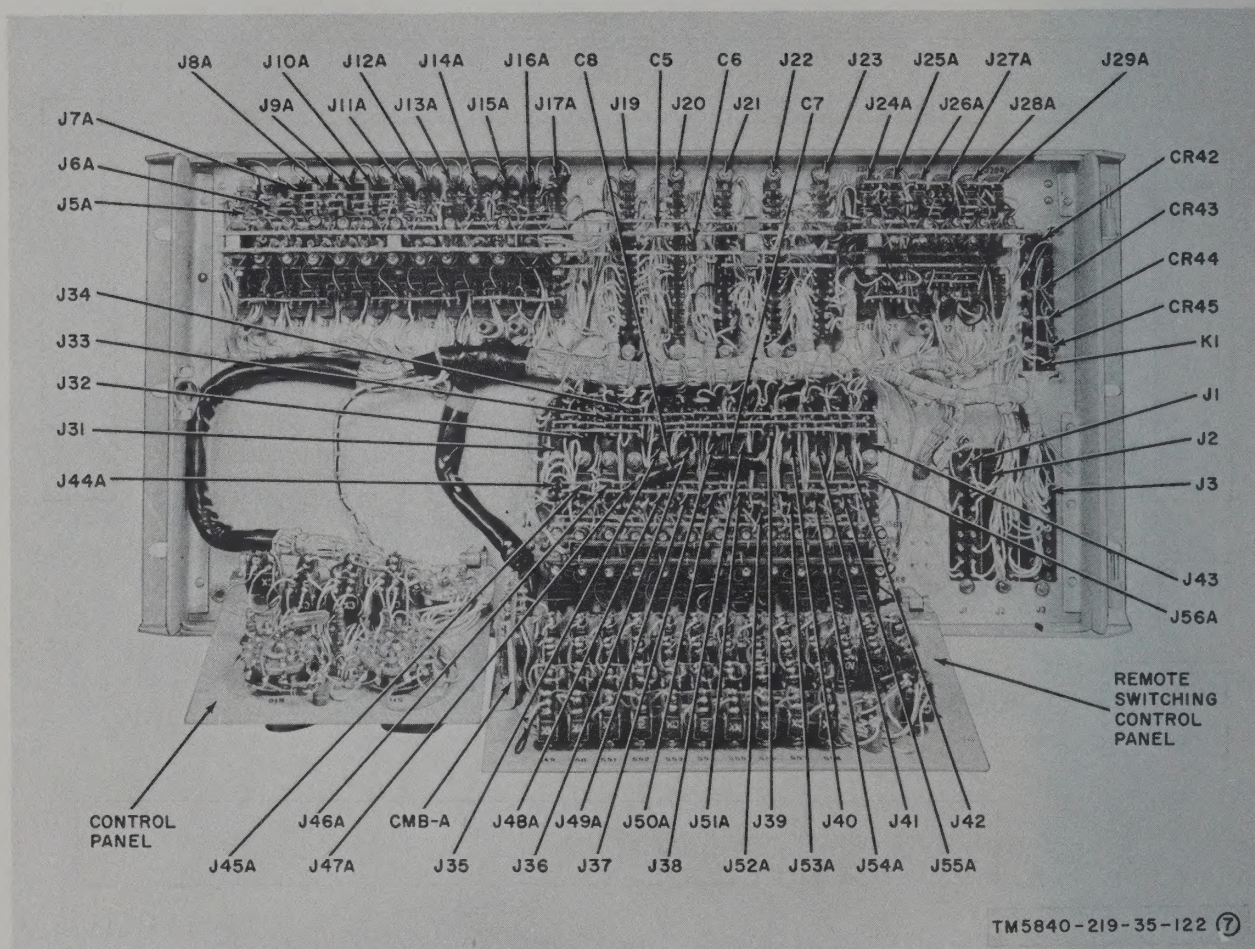
Parts location
Figure 140—Continued.



Parts location
Figure 140—Continued.

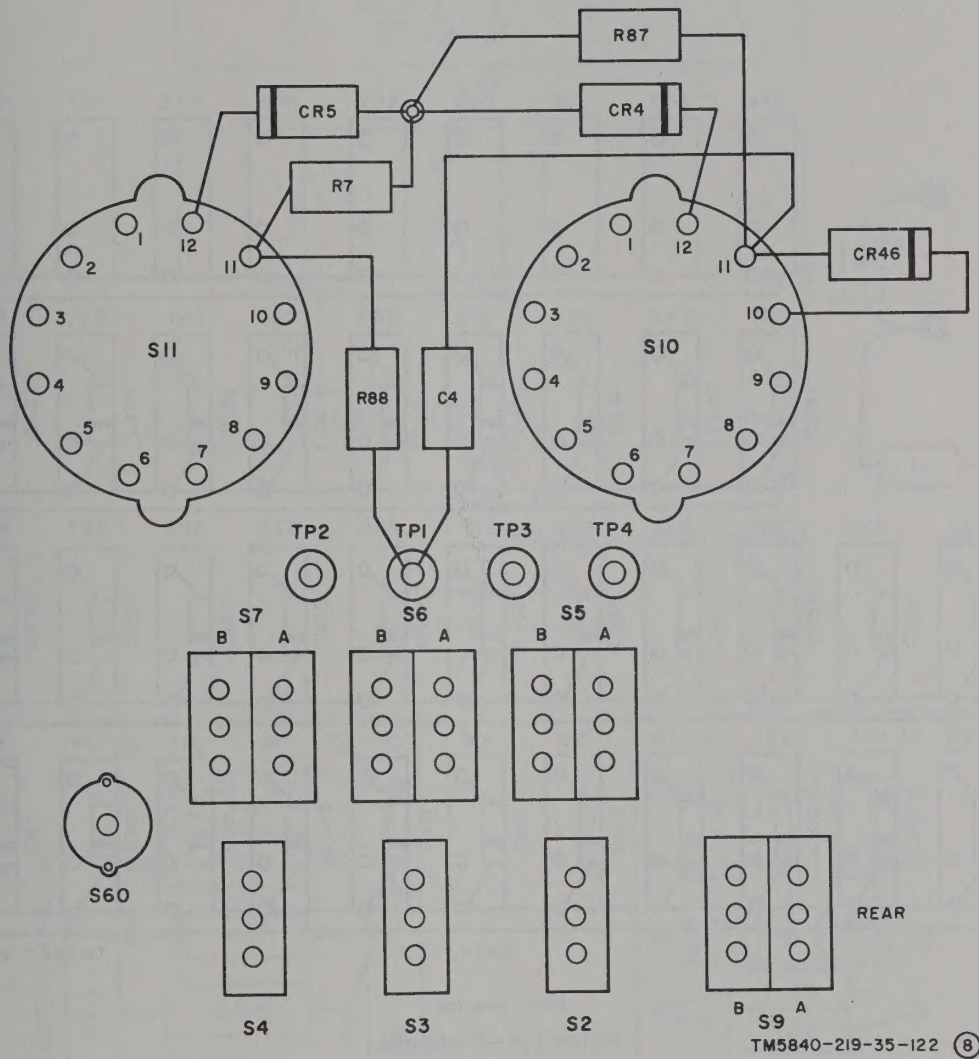


Parts location
Figure 140—Continued.

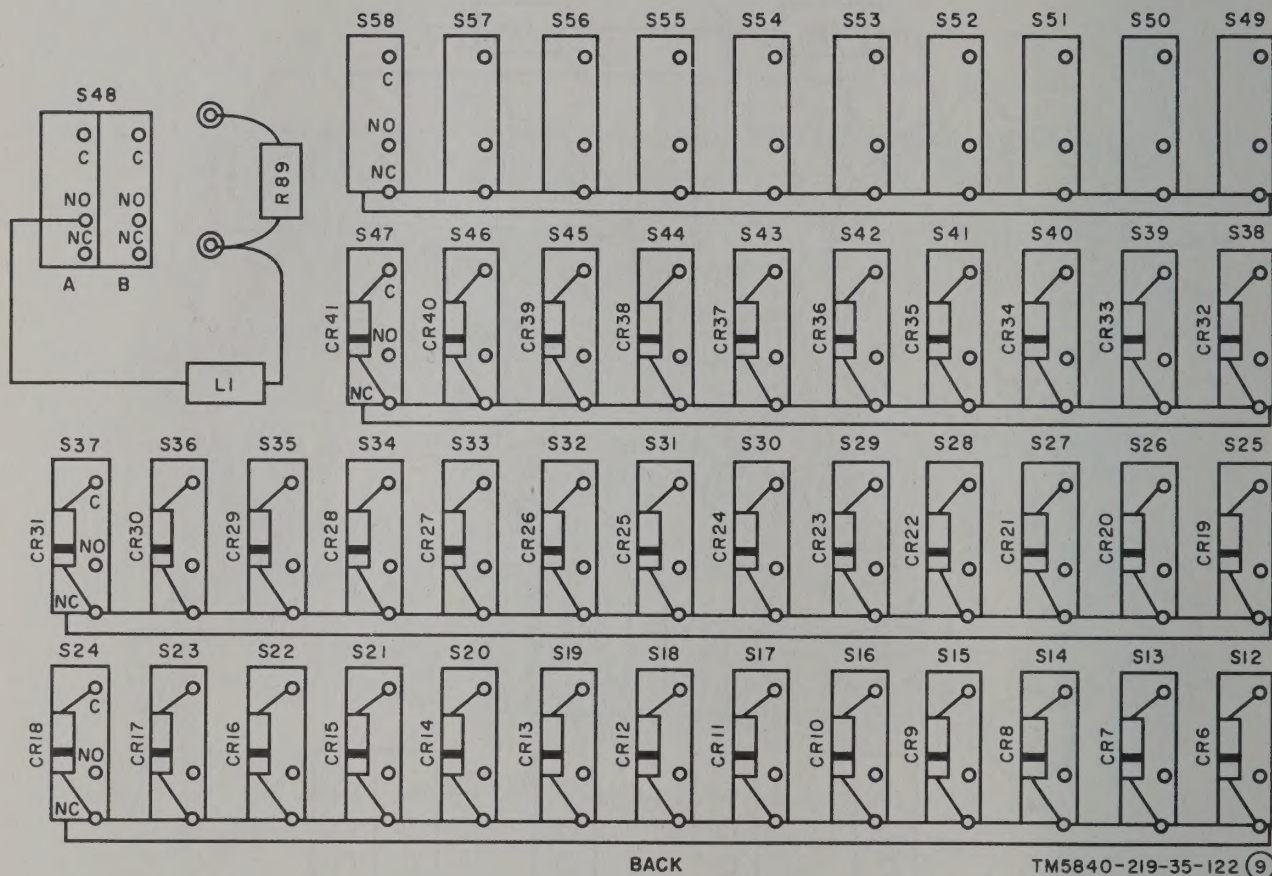


Parts location

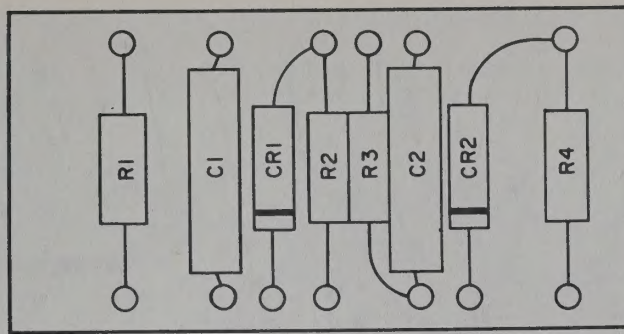
Figure 140—Continued.



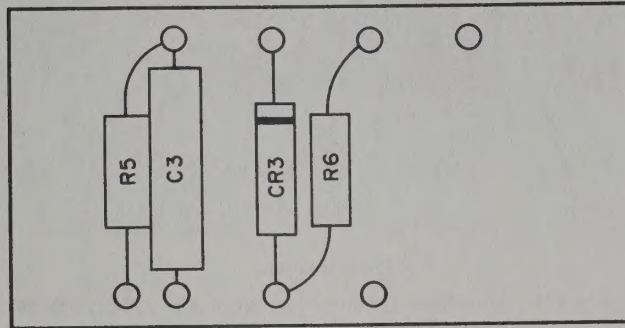
Parts location
Figure 140—Continued.



Parts location
Figure 140—Continued.



LEFT



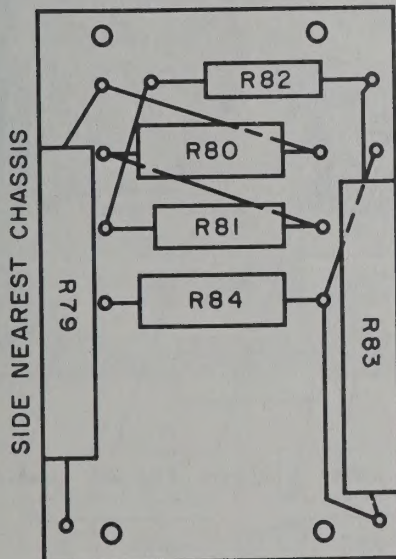
RIGHT

CMB-A

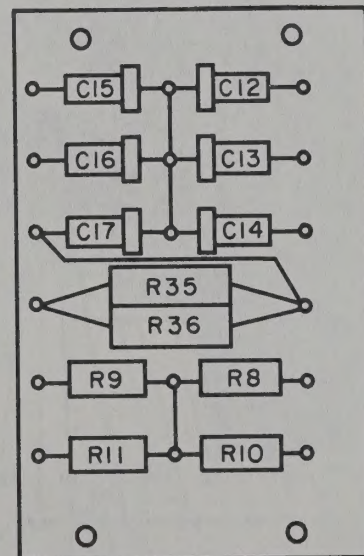
TM5840-219-35-122 (10)

Component boards

Figure 140—Continued.



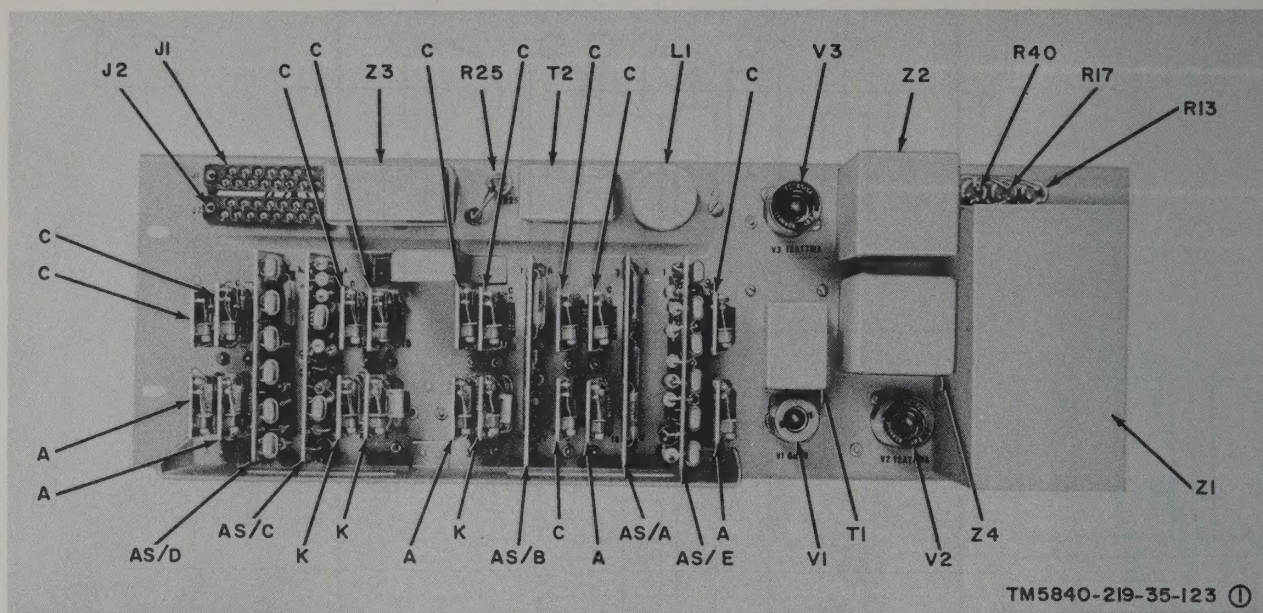
CMB-B



TM 5840 - 219 - 35 - 122 (11)

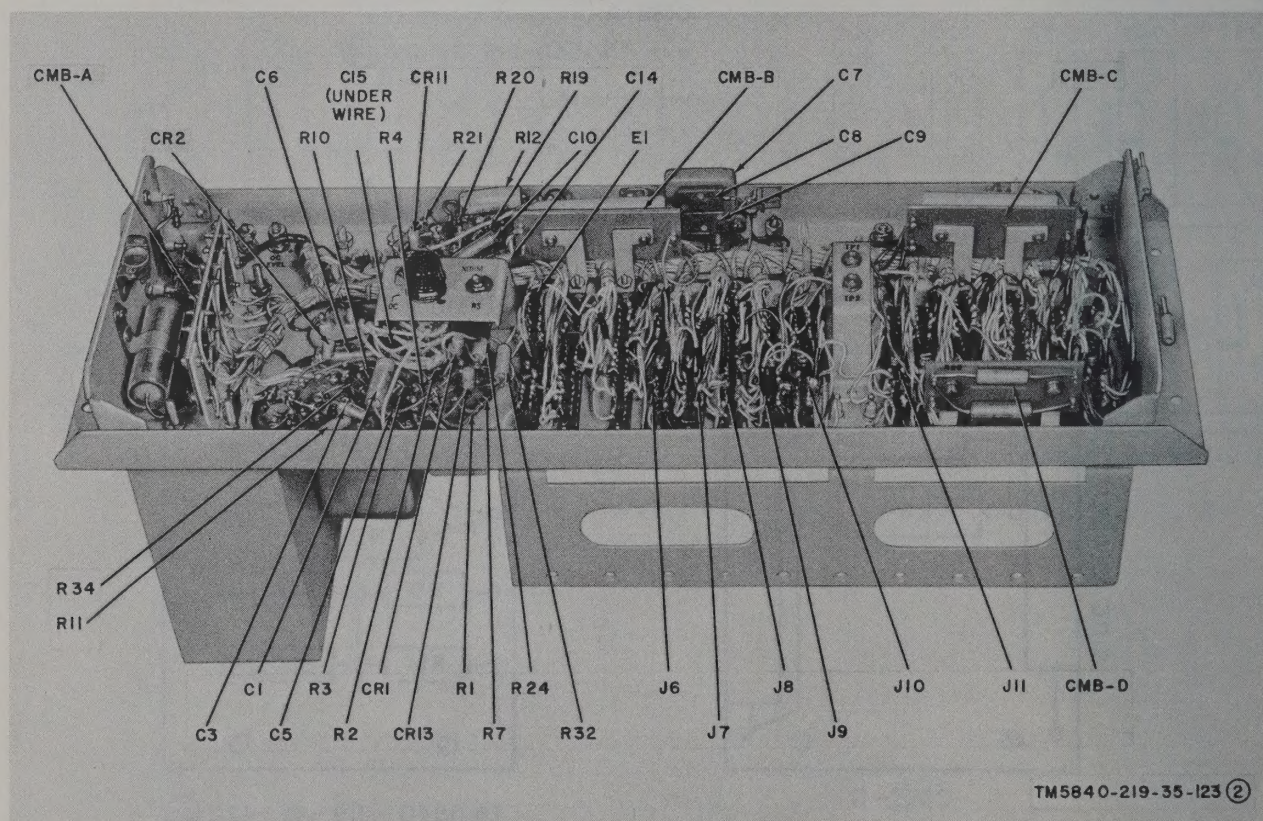
Component boards

Figure 140—Continued.



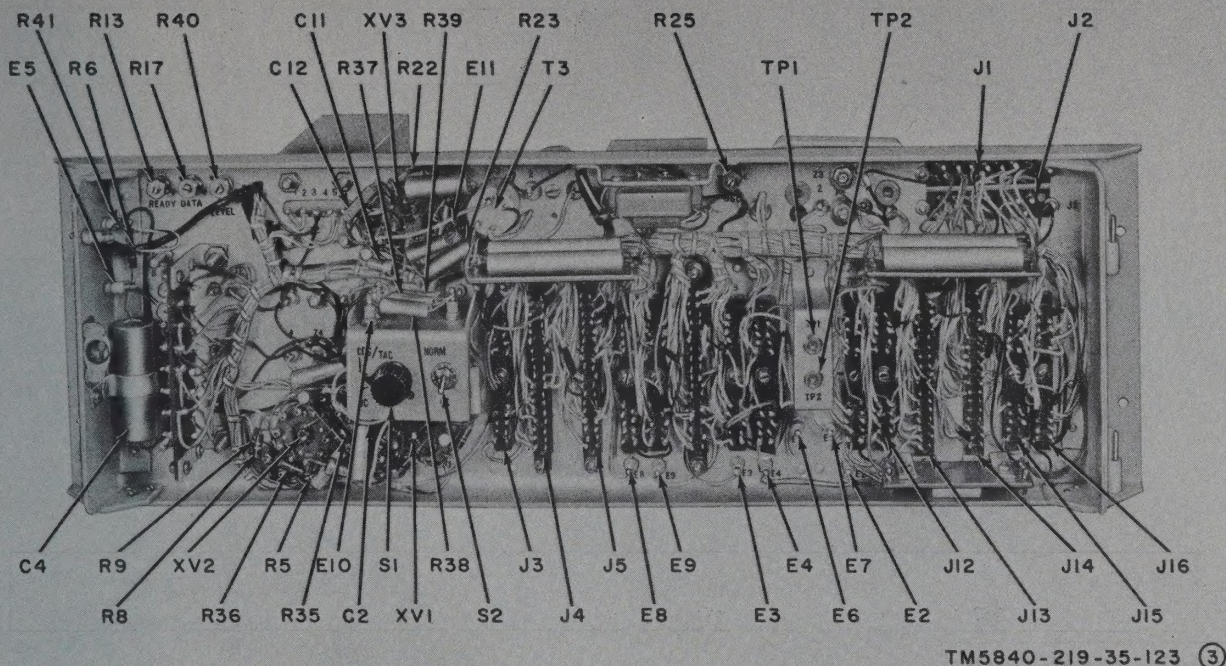
Parts location

Figure 141. Amplifier-synchronizer unit AM-2126/TSQ-36.



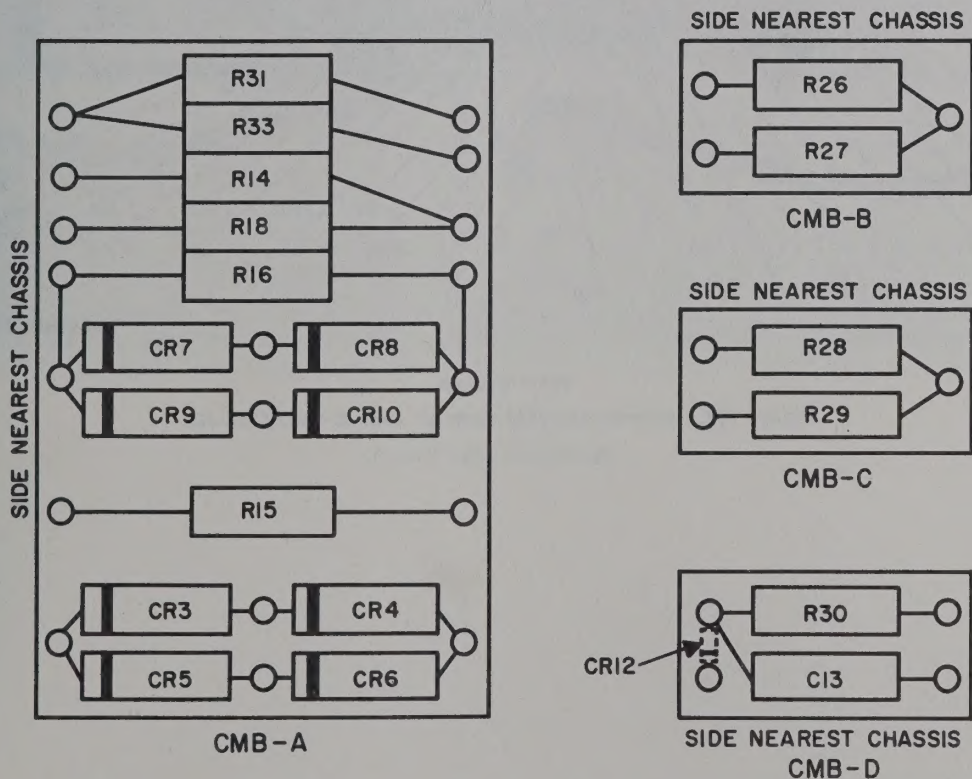
Parts location

Figure 141—Continued.



Parts location

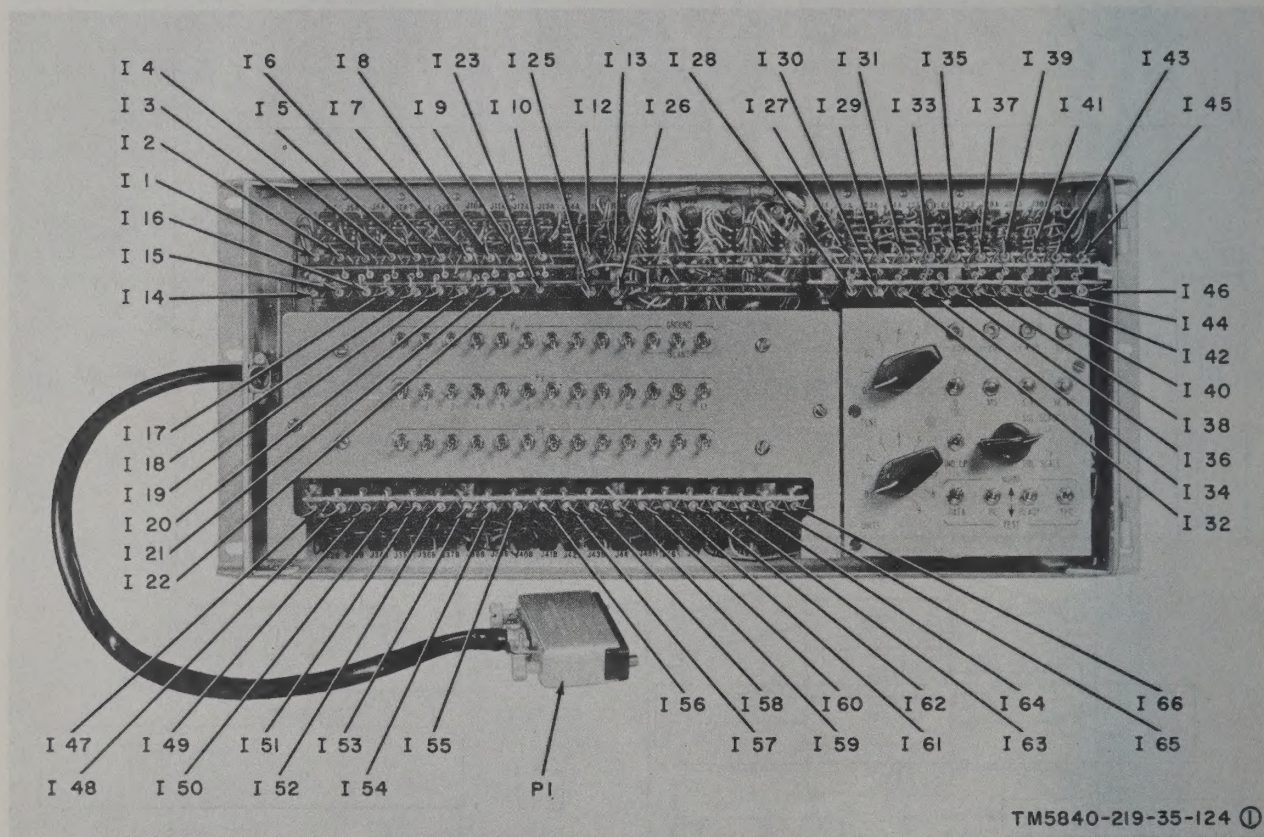
Figure 141—Continued.

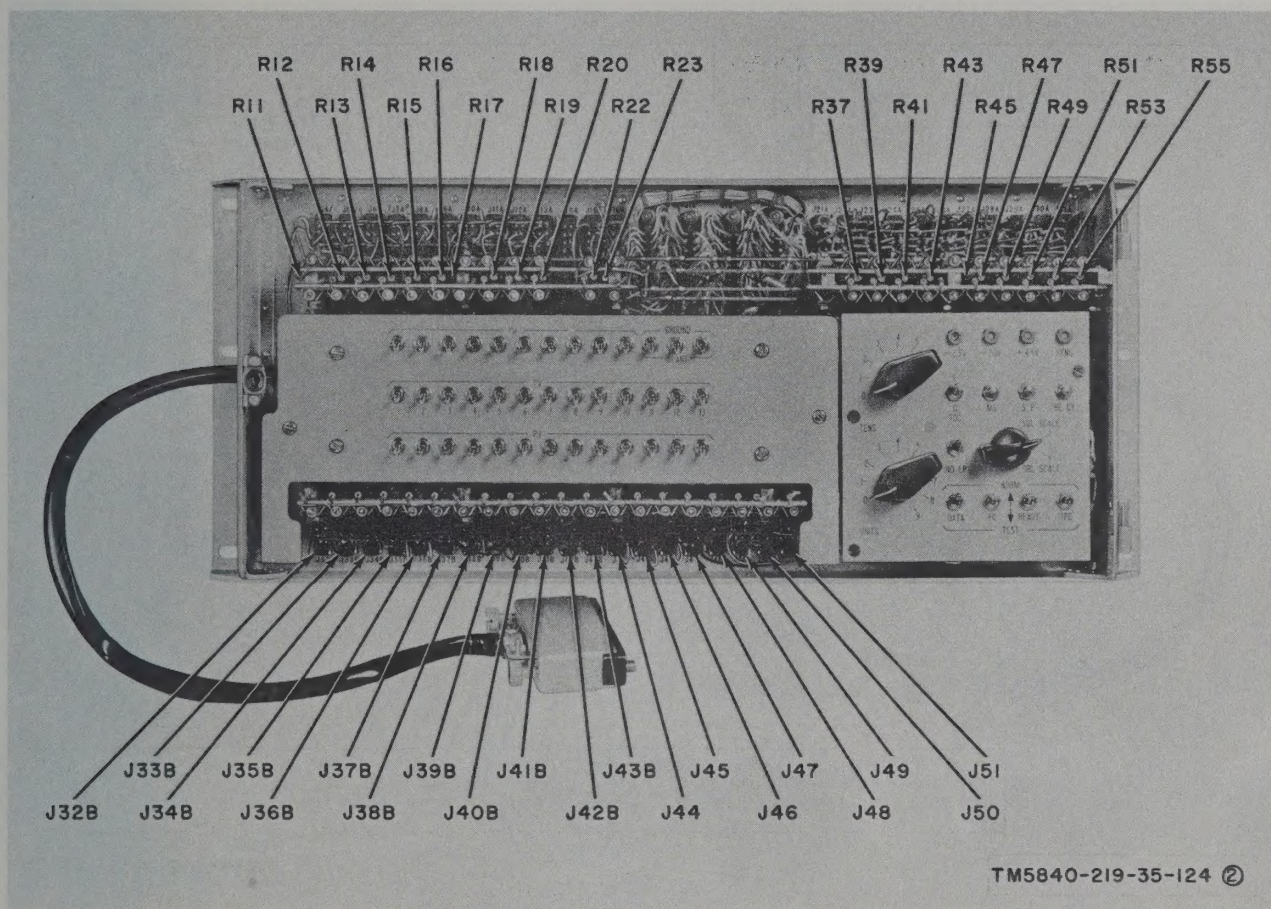


TM5840-219-35-123 ④

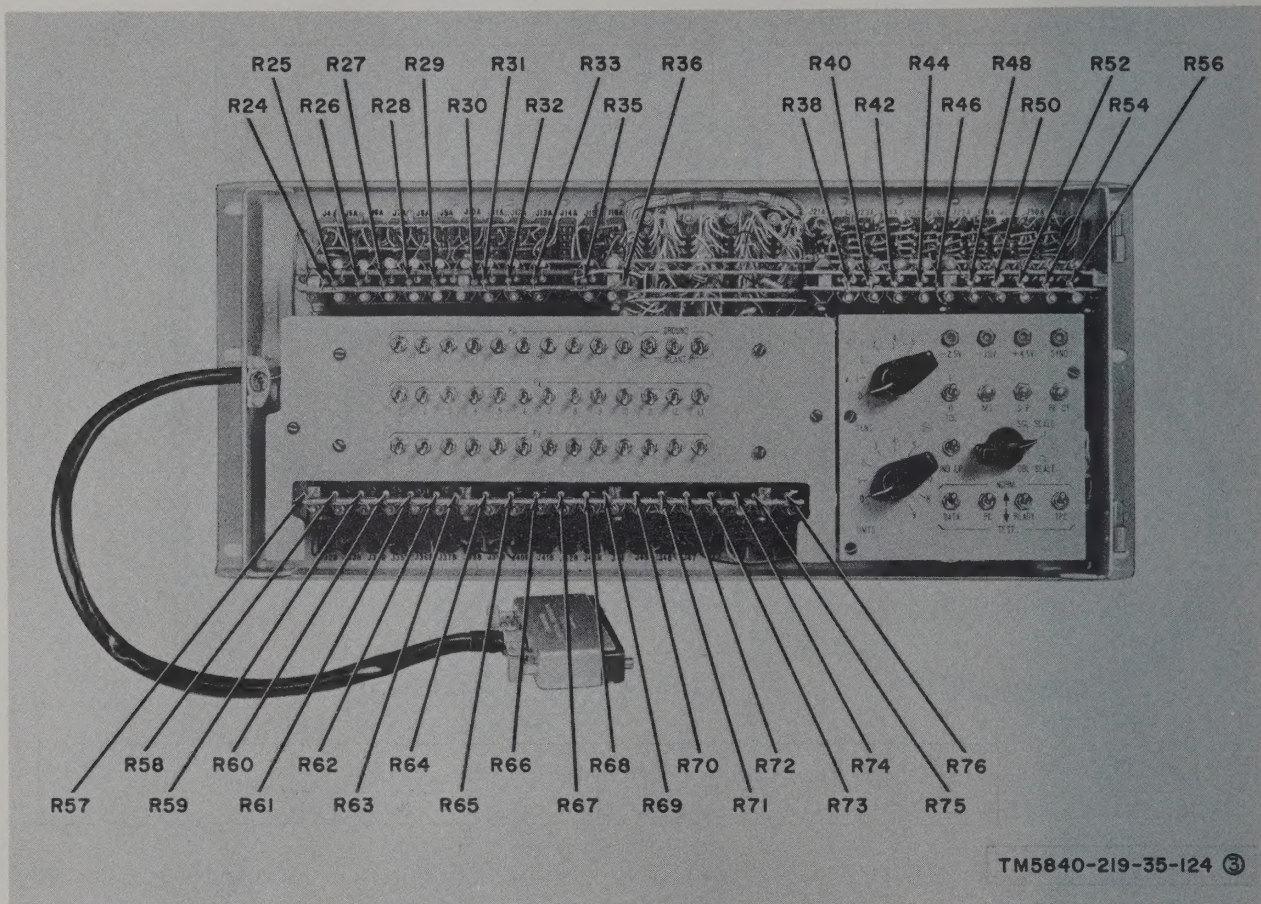
Component boards

Figure 141—Continued.

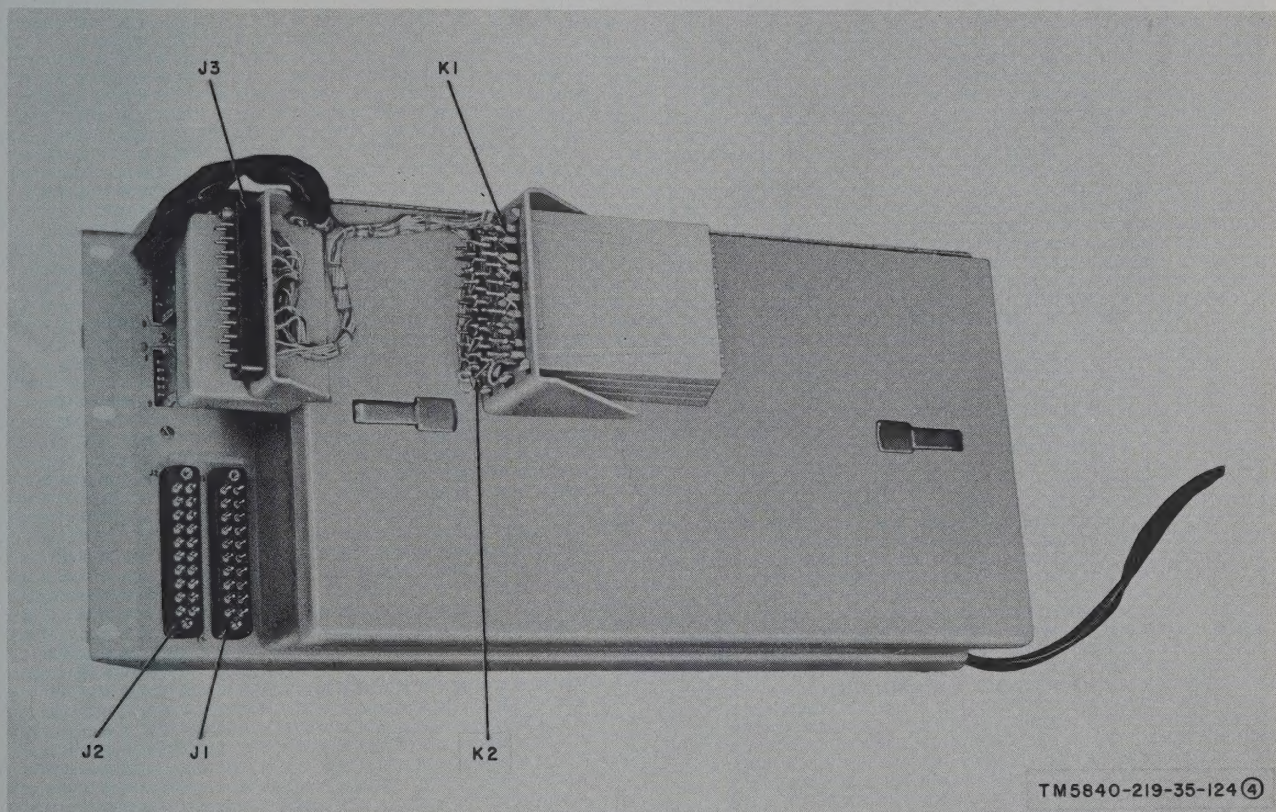




Parts location
 Figure 142—Continued.

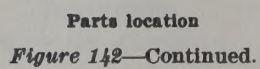


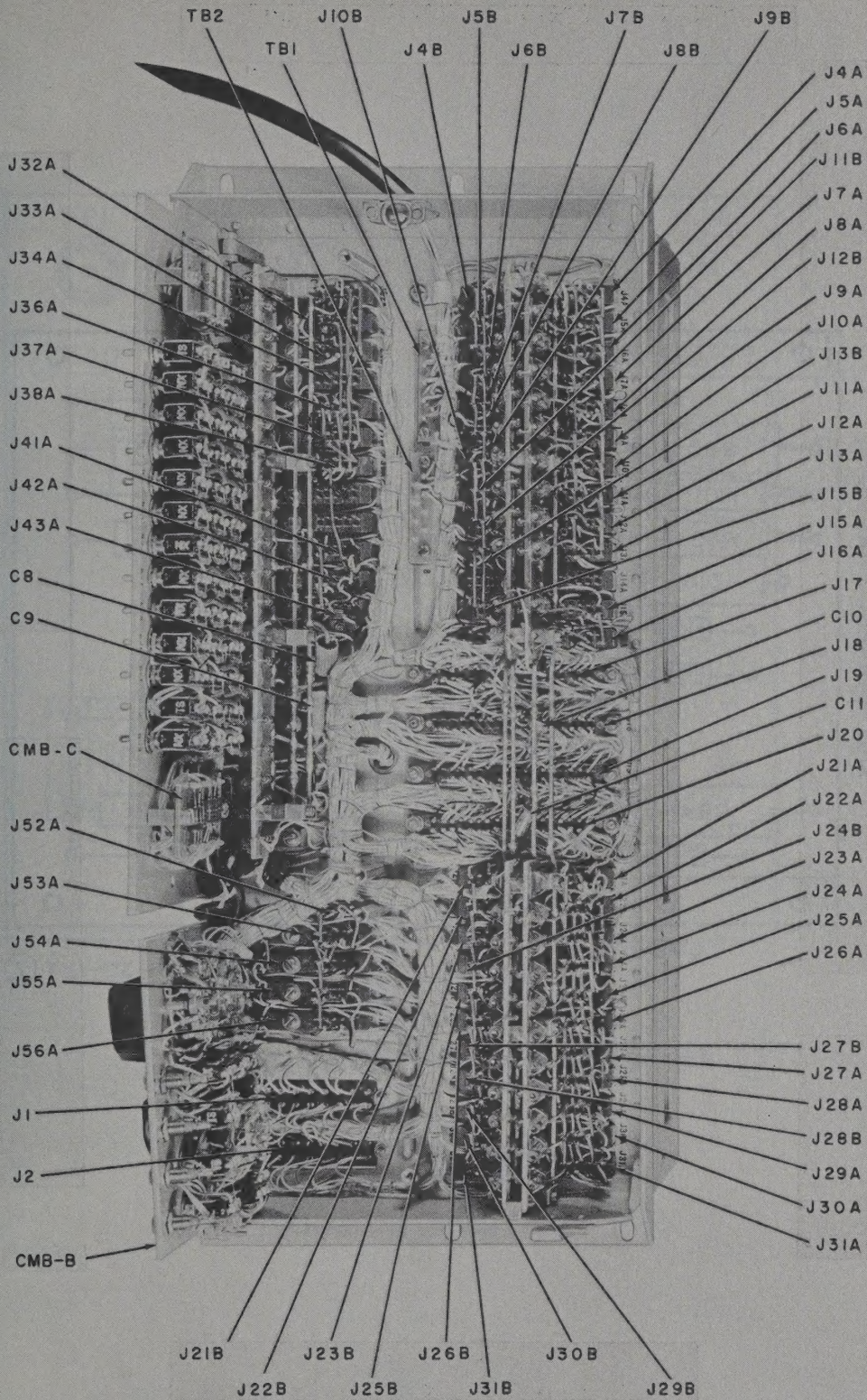
Parts location
Figure 142—Continued.



TM 5840-219-35-124 (4)

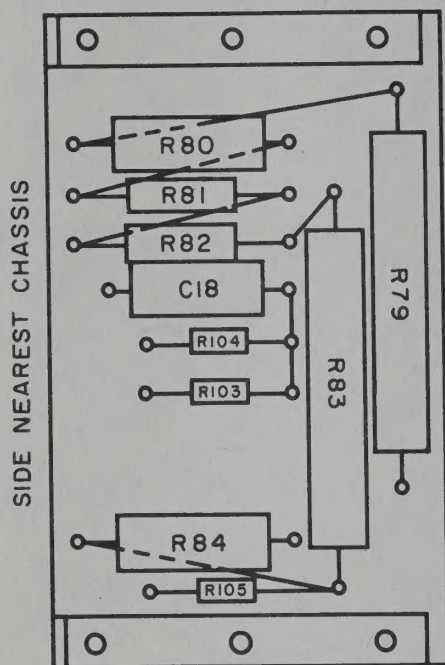
Parts location
Figure 142—Continued.



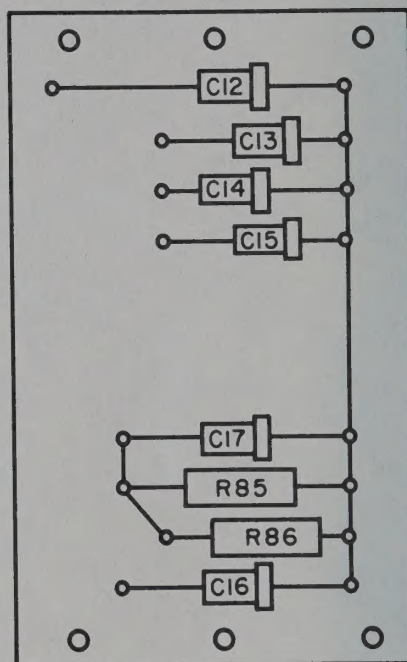


TM5840-219-35-124 (6)

Parts location
Figure 142—Continued.

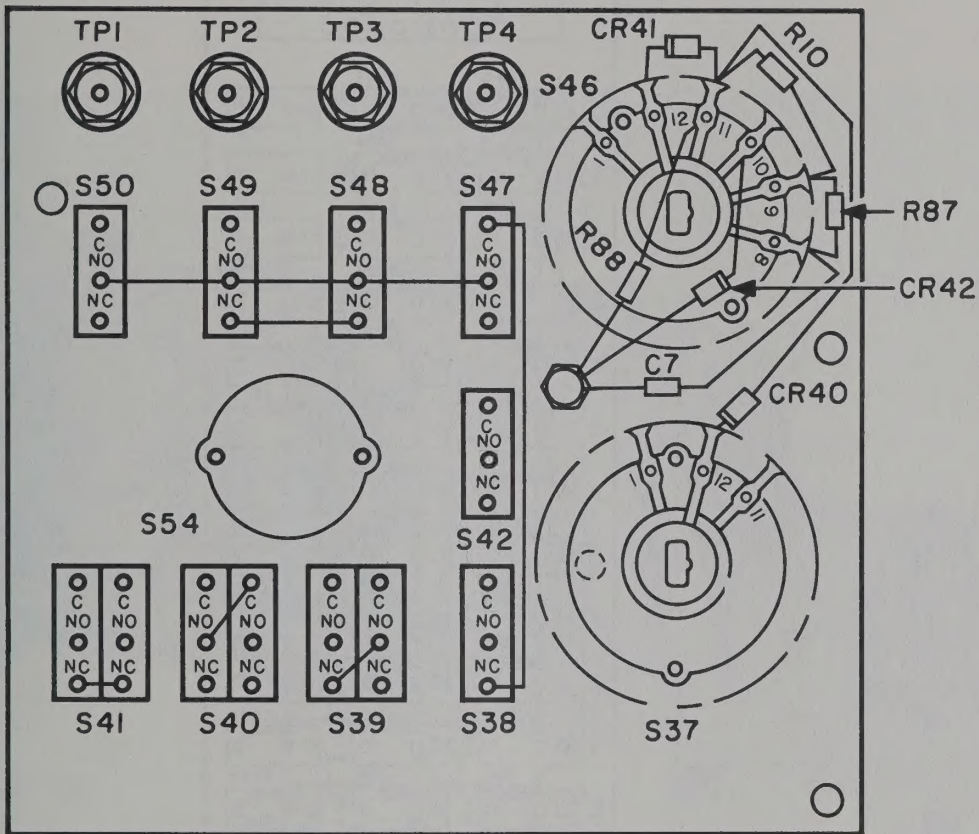


CMB-A



TM 5840-219-35-124 (7)

Component boards
Figure 142—Continued.

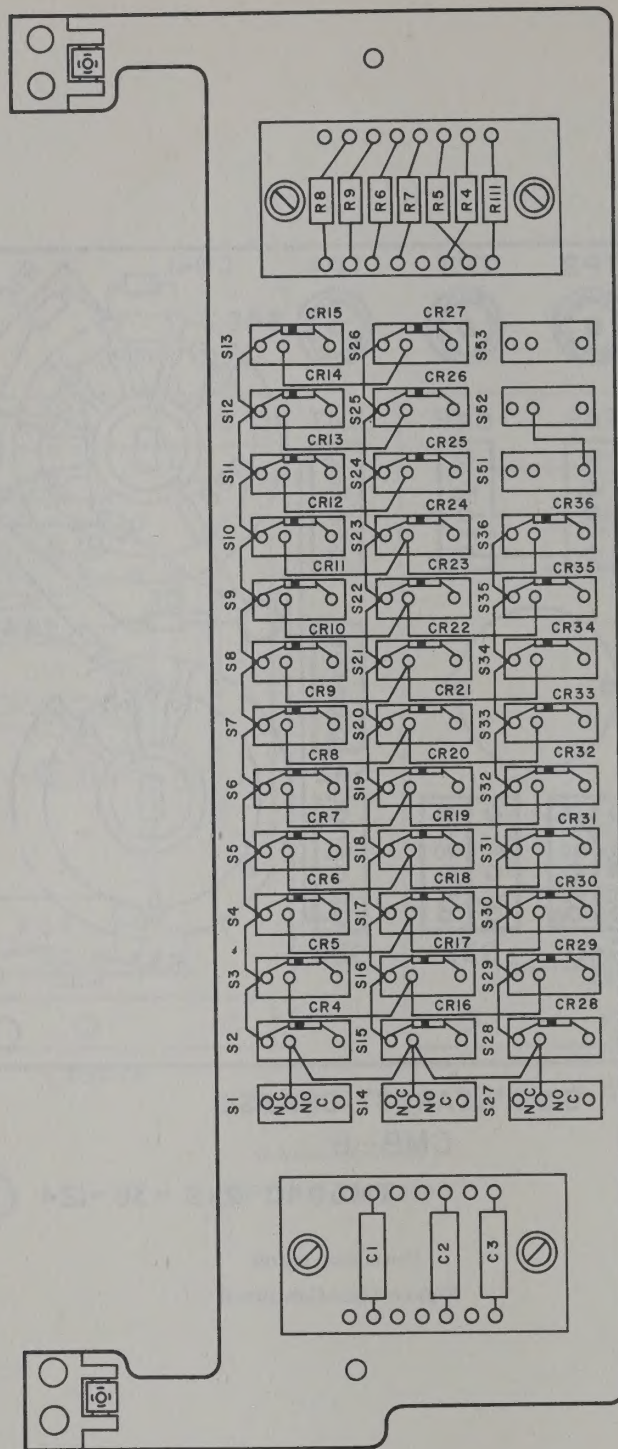


SIDE NEAREST CHASSIS
CMB-B

TM5840-219 -35 -124 (8)

Component boards

Figure 142—Continued.

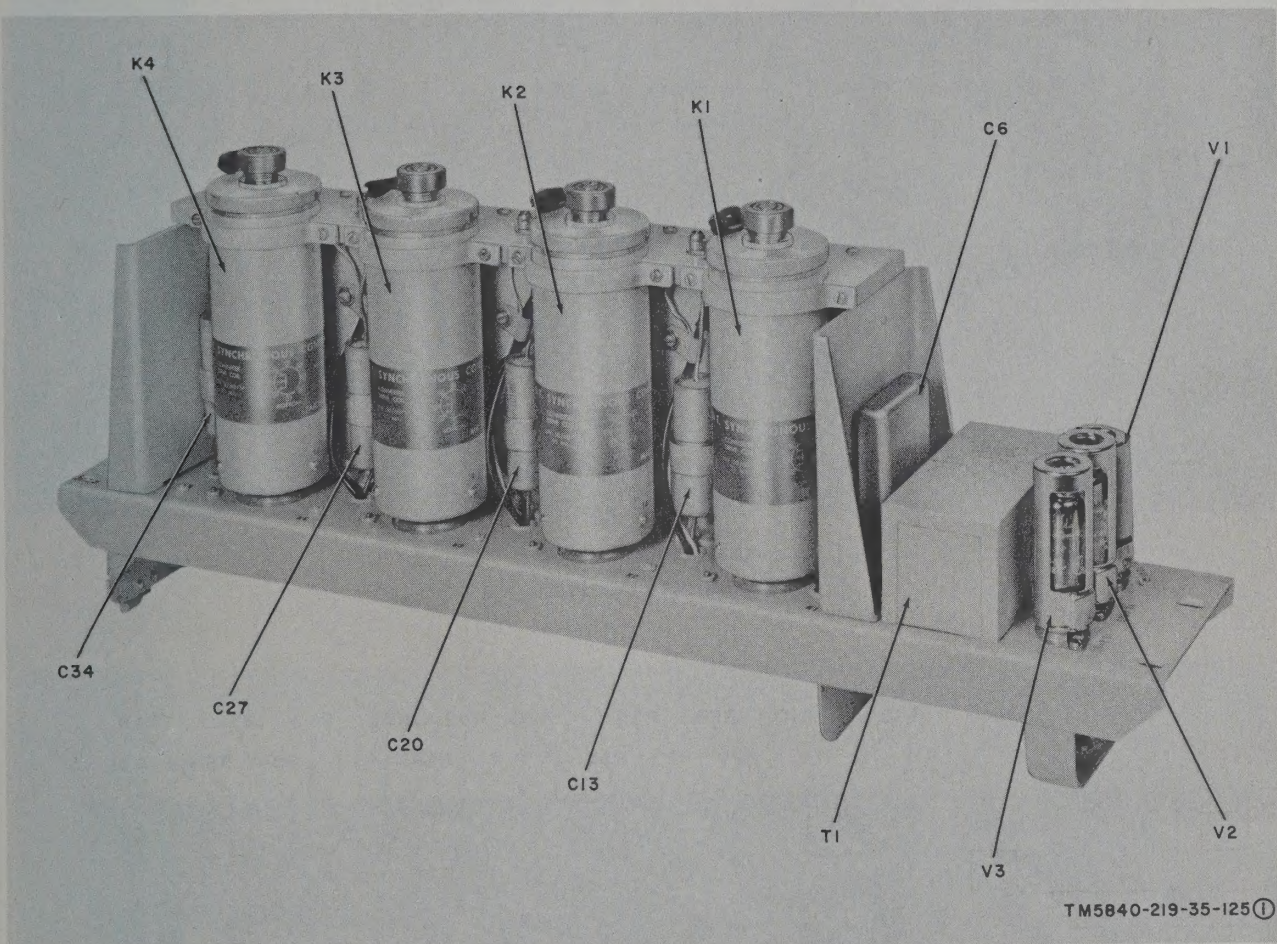


CMB-C

TM5840-219-35-124 (9)

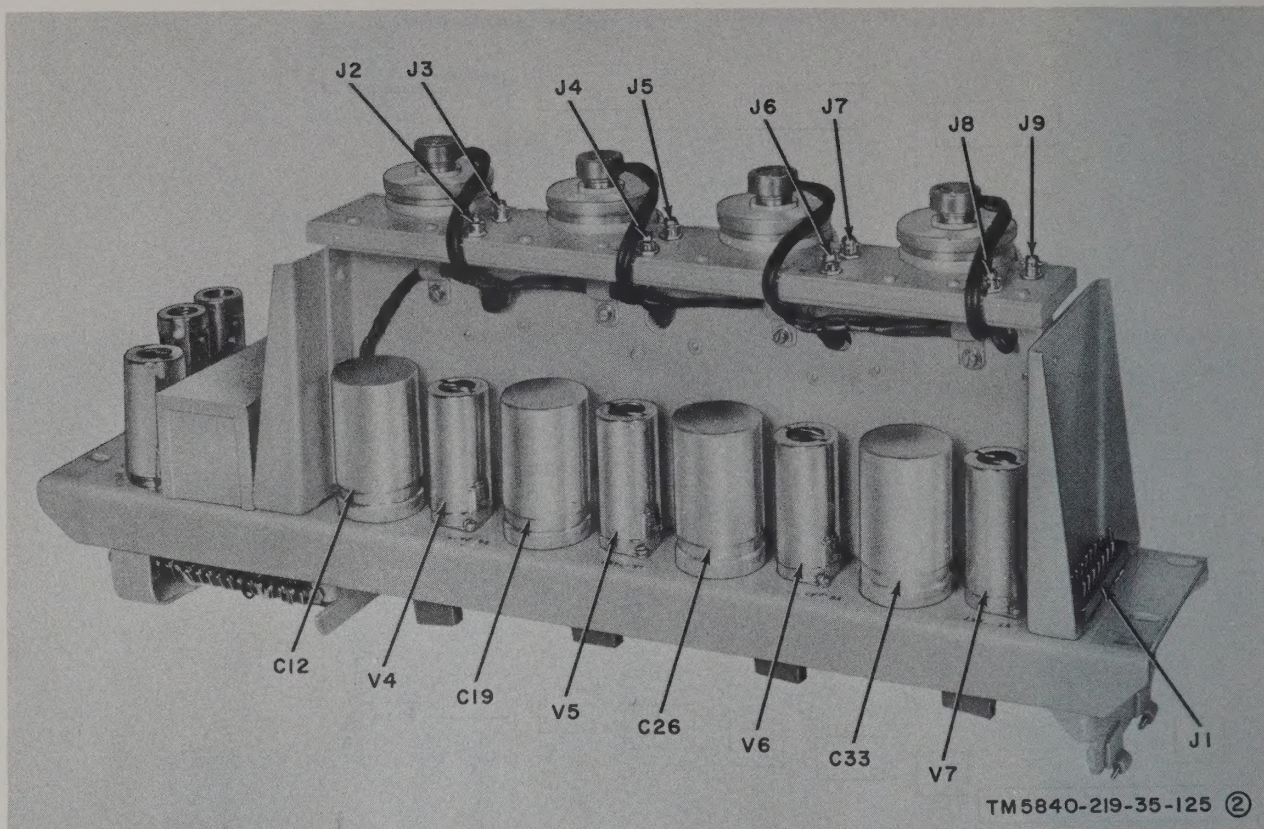
Component boards

Figure 142—Continued.

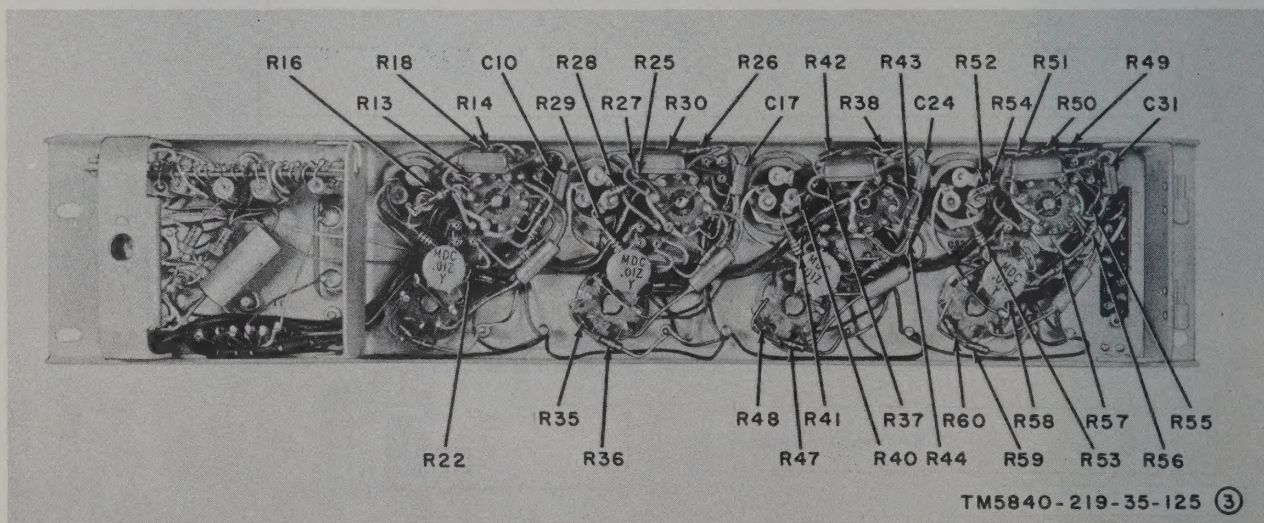


Parts location

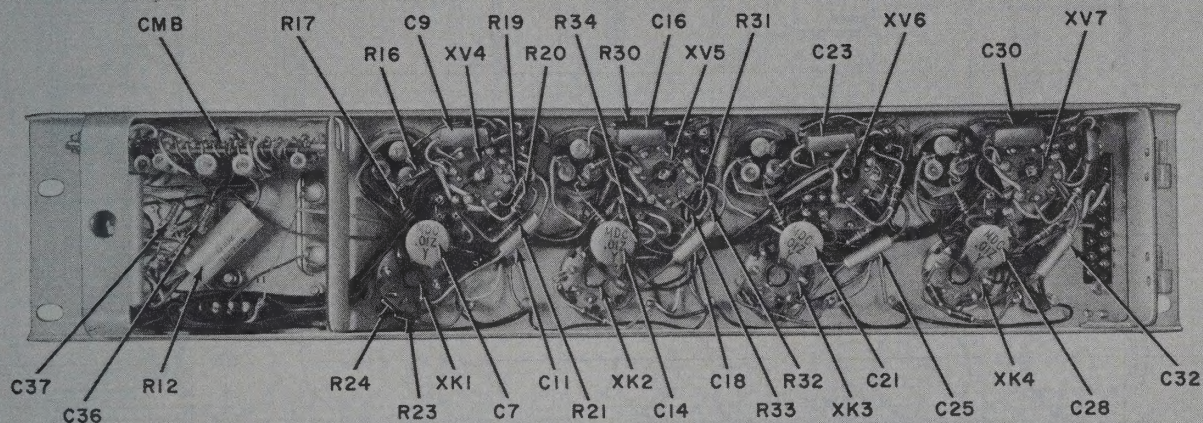
Figure 143. Direct current amplifier AM-2125/TSQ-36.



Parts location
Figure 143—Continued.



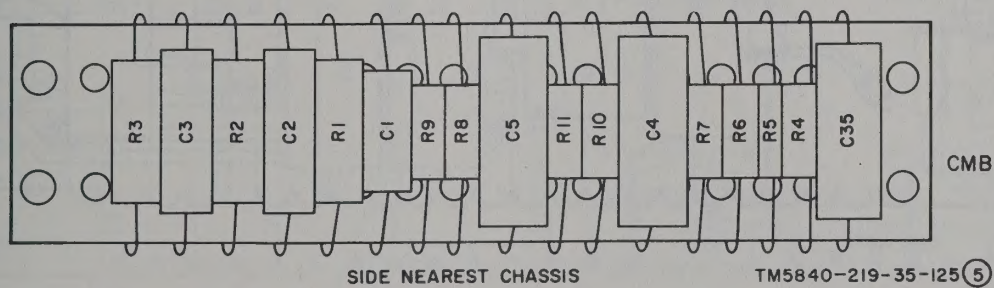
Parts location
Figure 143—Continued.



TM5840-219-35-125 (4)

Parts location

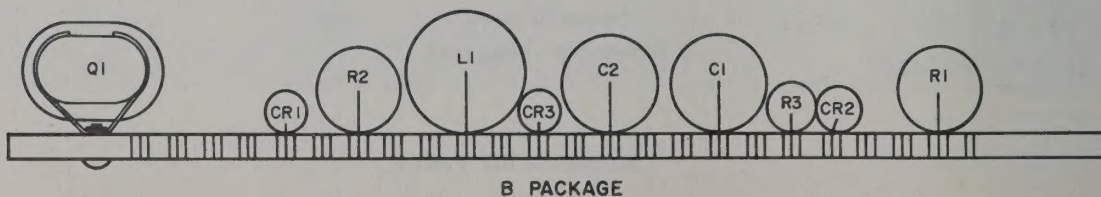
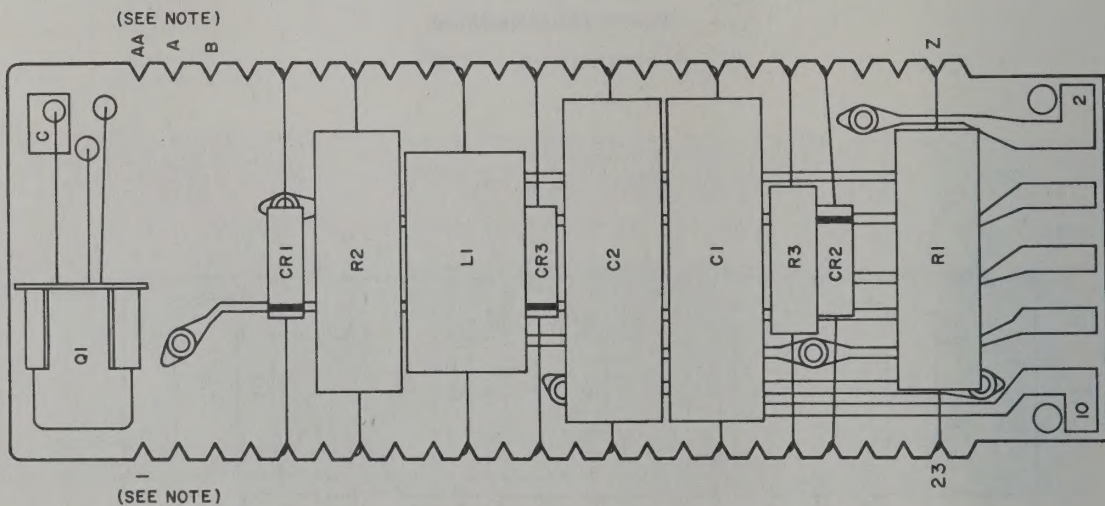
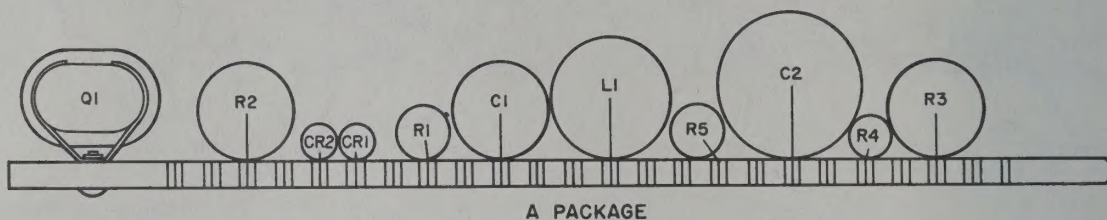
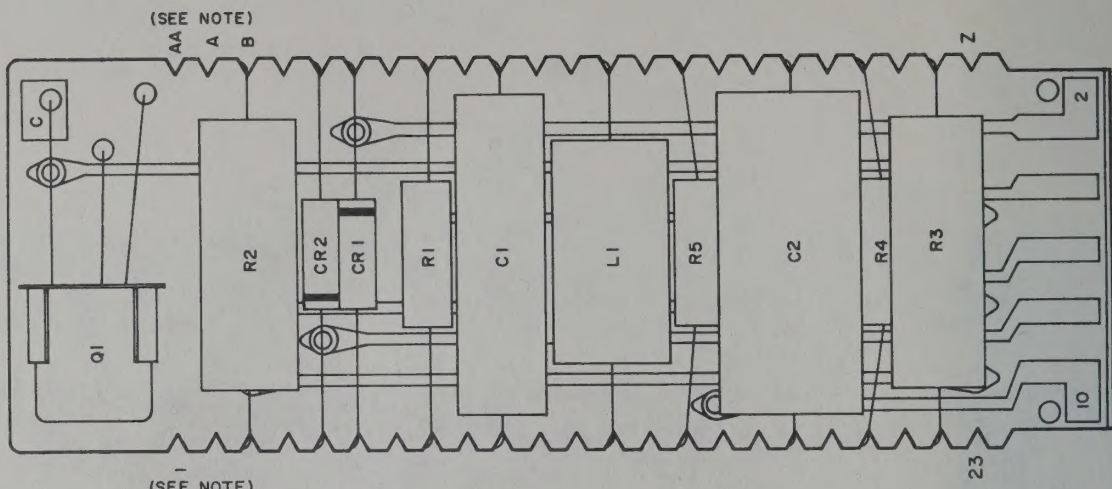
Figure 143—Continued.



TM5840-219-35-125 (5)

Component boards

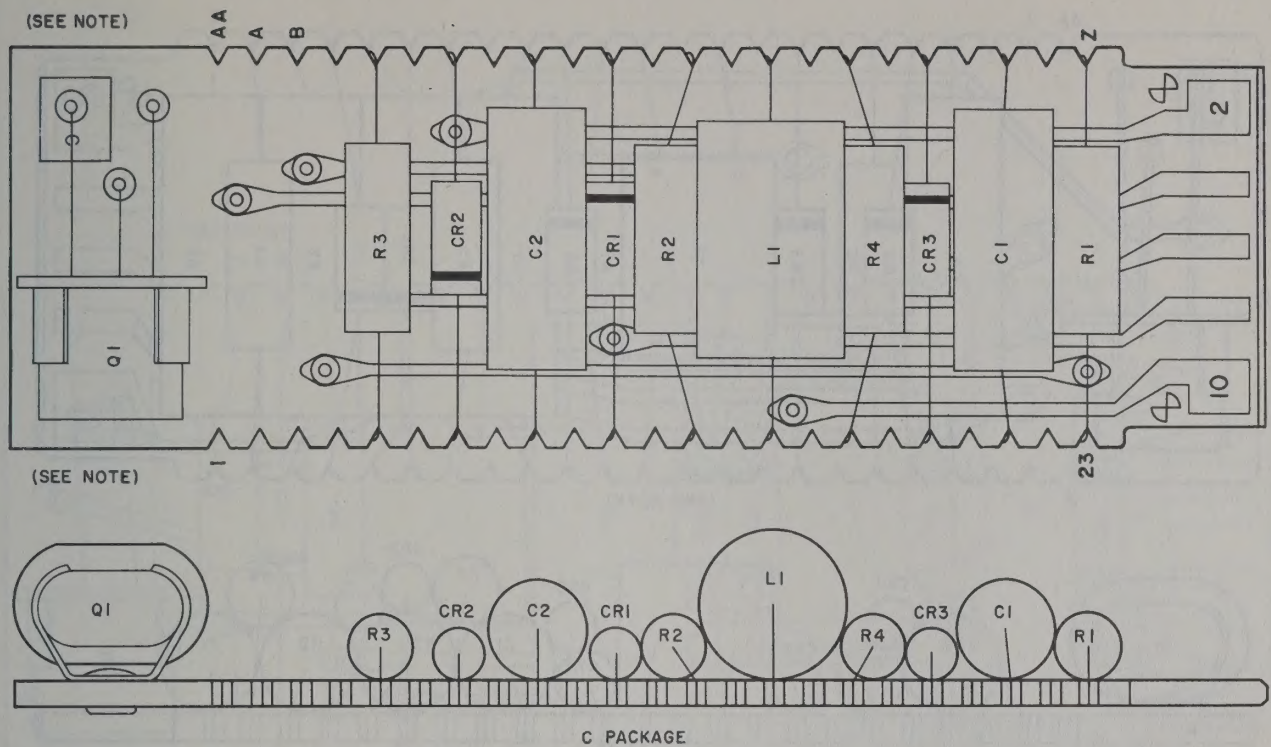
Figure 143—Continued.



NOTE:
LETTERS AND NUMBERS ARE FOR REFERENCE ONLY.
TERMINAL DESIGNATIONS I, Q, AND X ARE NOT USED.

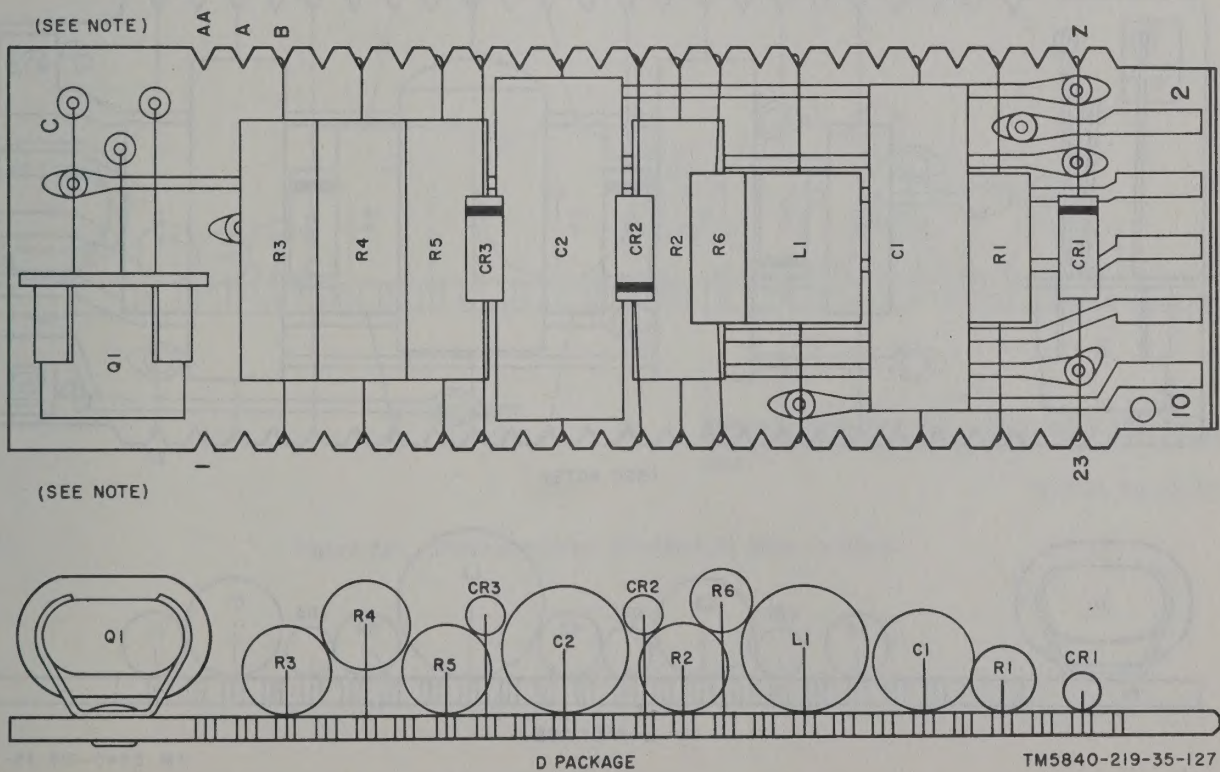
TM 5840-219-35-126

Figure 144. Gated flip-flop TD-210A/G and gated flip-flop TD-212A/G, parts location.



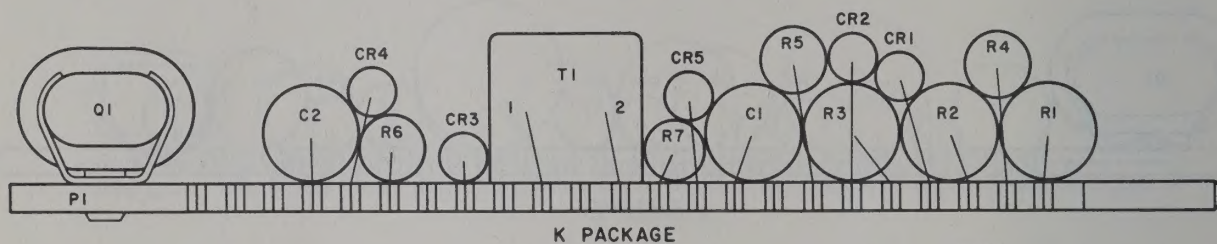
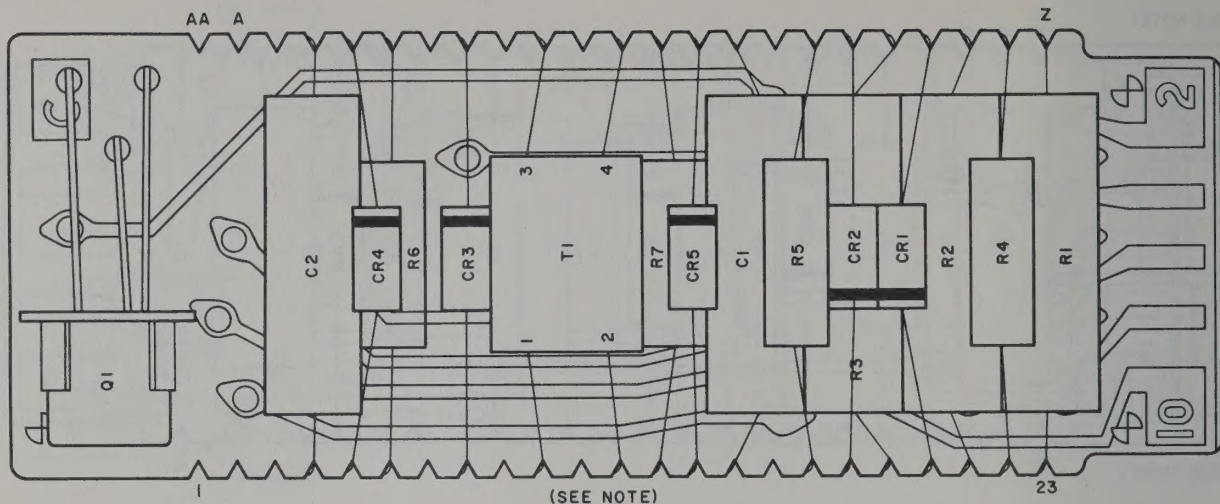
NOTE:

TERMINAL DESIGNATION I, O, Q AND X ARE NOT USED.
LETTERS AND NUMBERS ARE FOR REFERENCE ONLY.



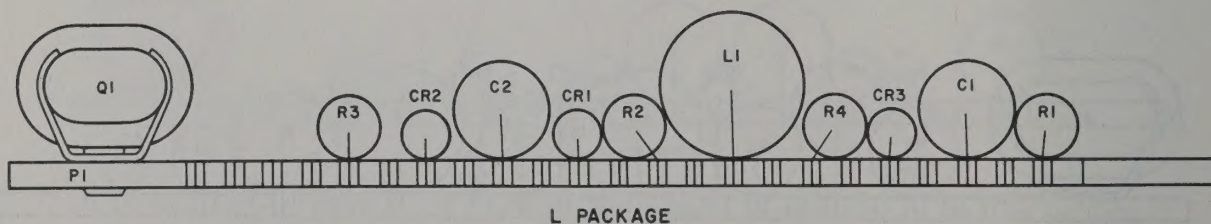
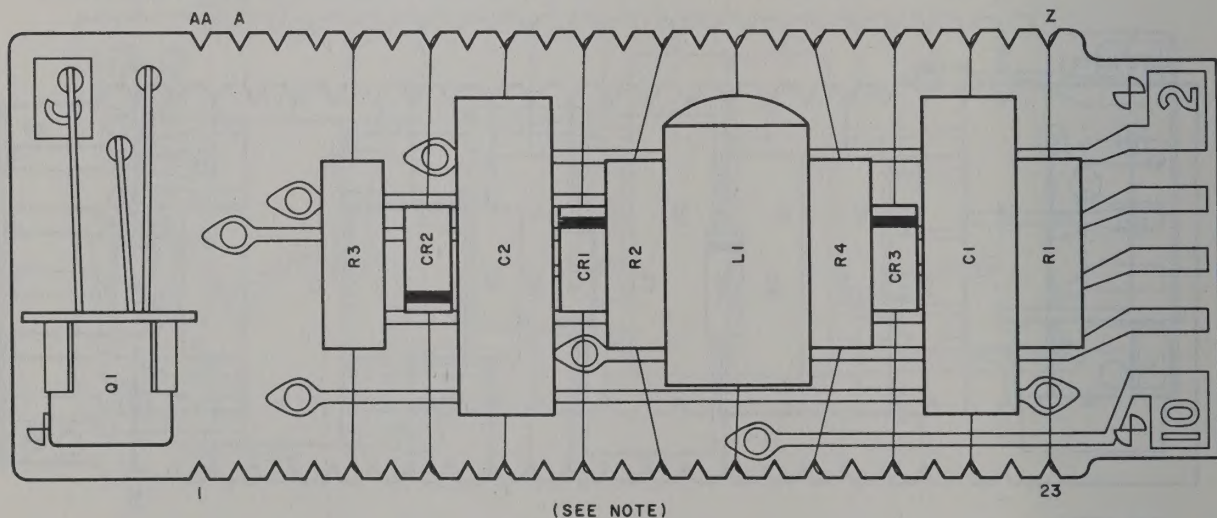
TM5840-219-35-127

Figure 145. Pulse generator SG-257A/G and gated flip-flop TD-211A/G, parts location.



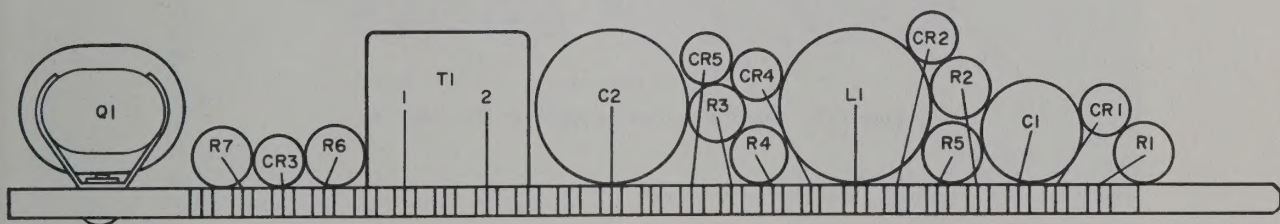
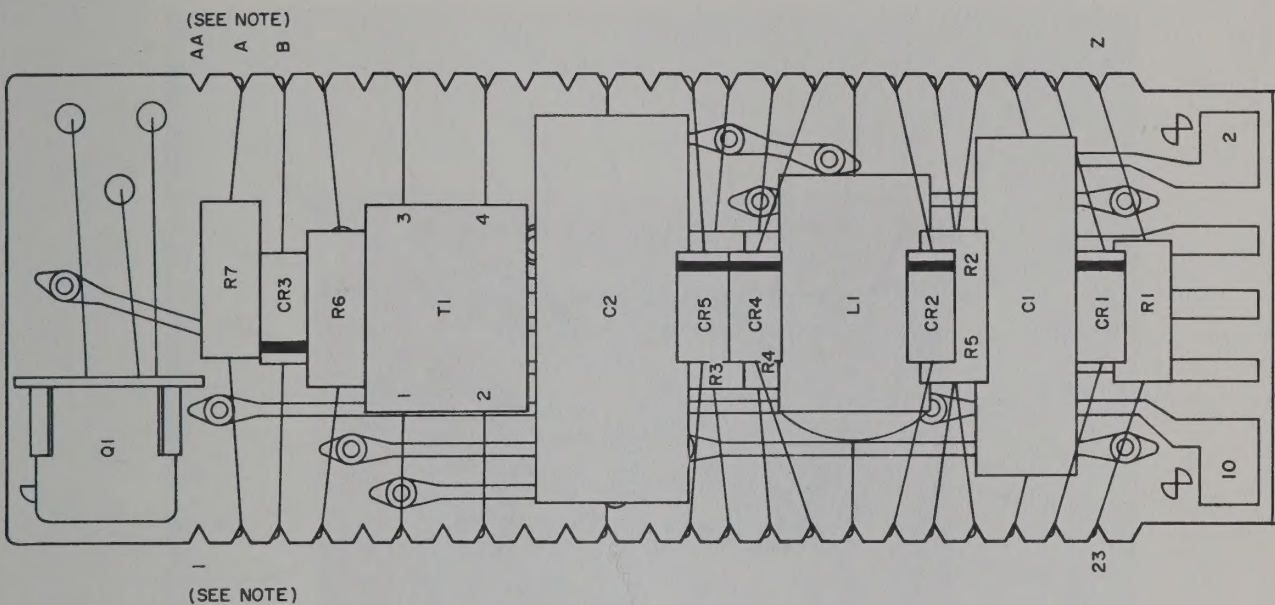
NOTE:

TERMINAL DESIGNATIONS I, O, Q, AND X ARE NOT USED. LETTERS AND NUMBERS ARE FOR REFERENCE ONLY.



TM 5840-219-35-128

Figure 146. Gated flip-flop TD-213A/G and pulse generator SG-259A/G, parts location.

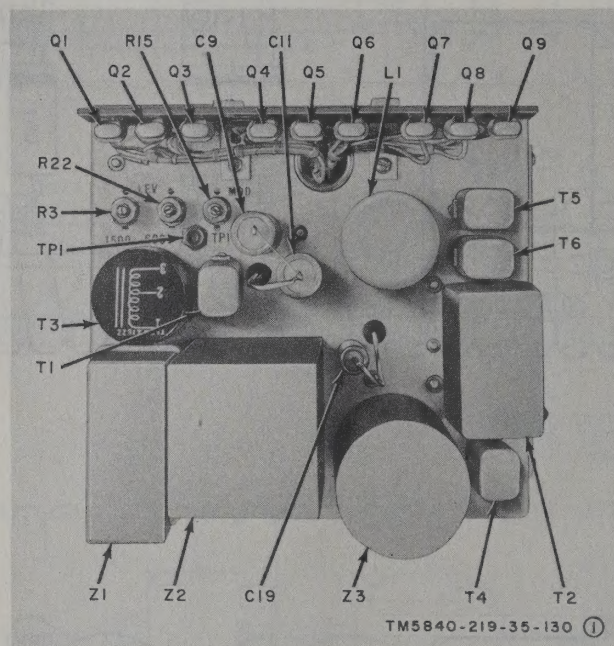


M PACKAGE

NOTE:
TERMINAL DESIGNATIONS I, O, Q, AND X ARE NOT
USED. LETTERS AND NUMBERS ARE FOR REFERENCE
ONLY.

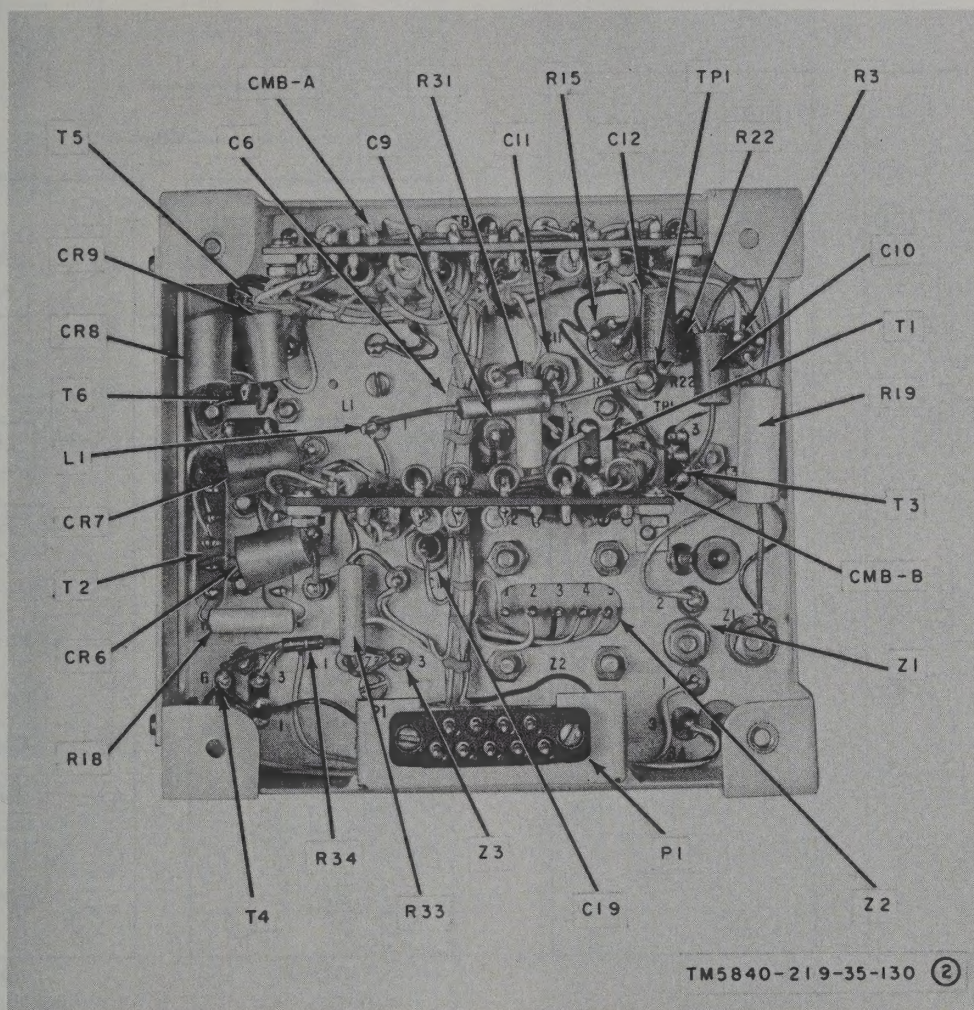
TM5840-219-35-129

Figure 147. Pulse generator SG-260A/G, parts location.



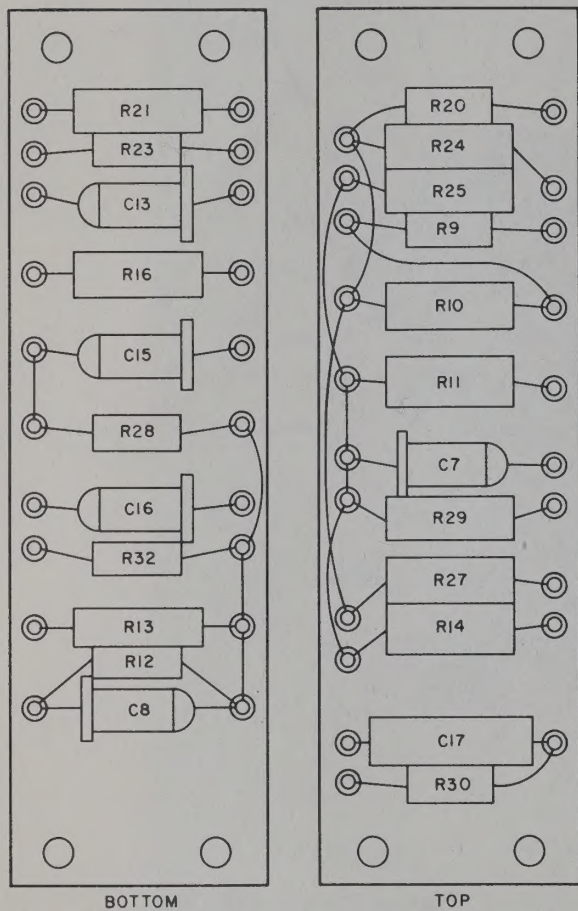
Parts location

Figure 148. Coordinate data modulator MD-323A/G.

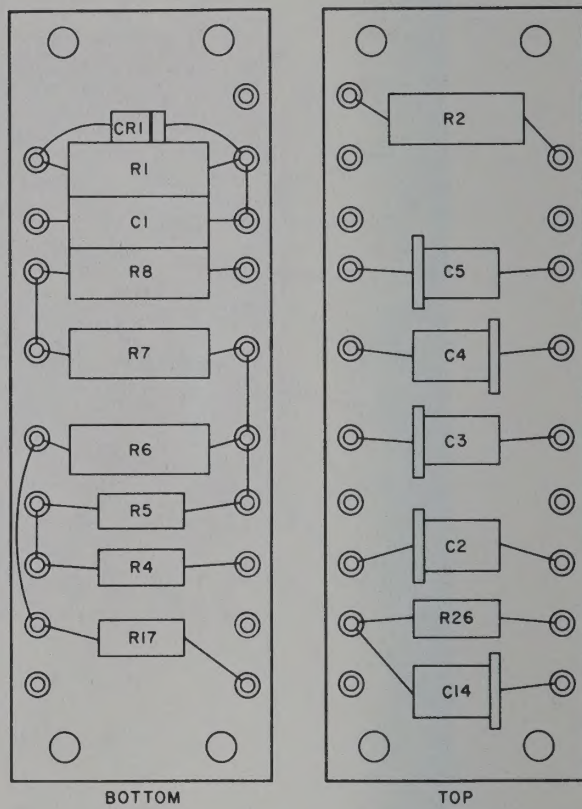


Parts location
 Figure 148—Continued.

CMB-A

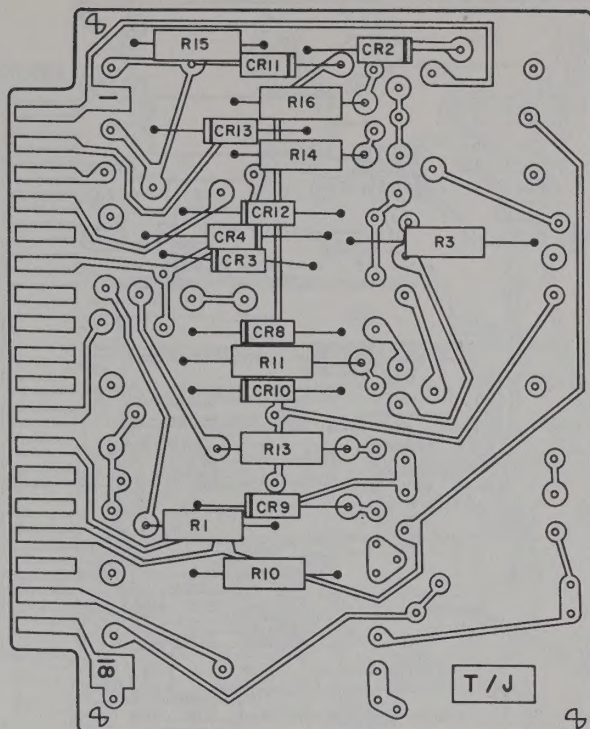
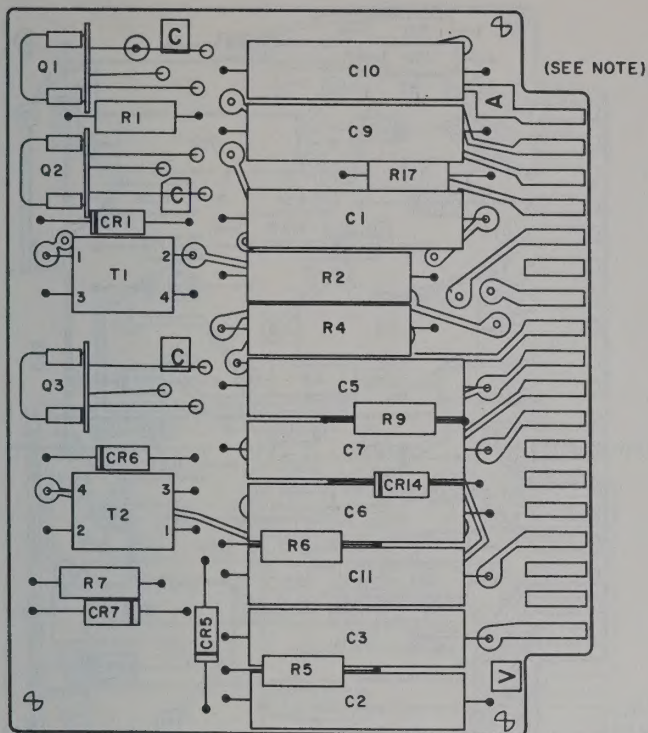


CMB-B



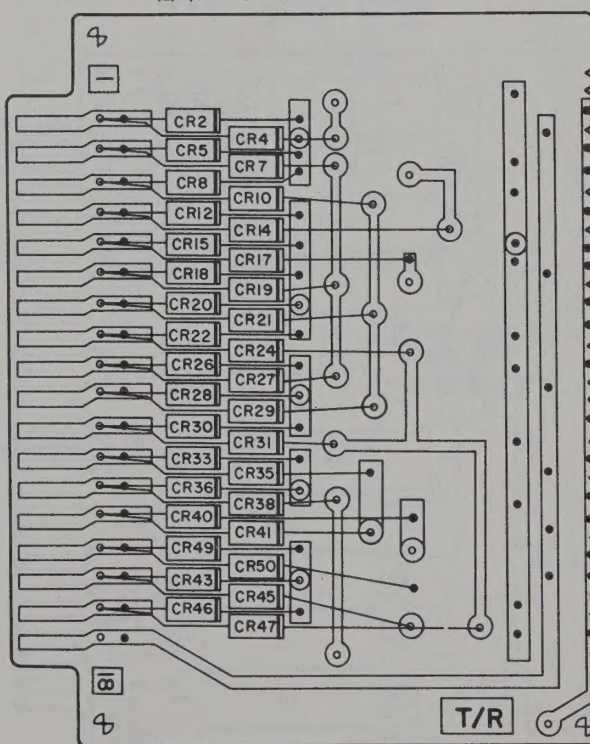
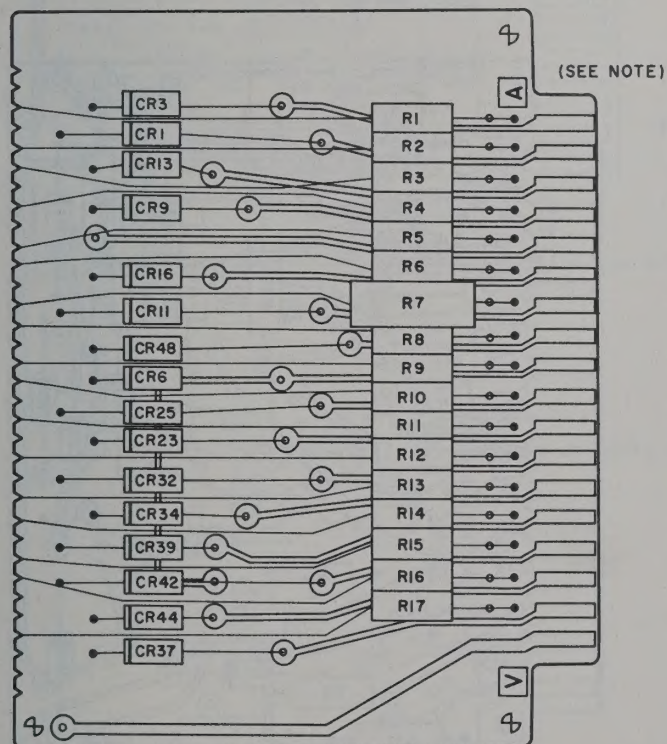
TM5840-219-35-130 (3)

Component boards
 Figure 148—Continued.



T/J PACKAGE

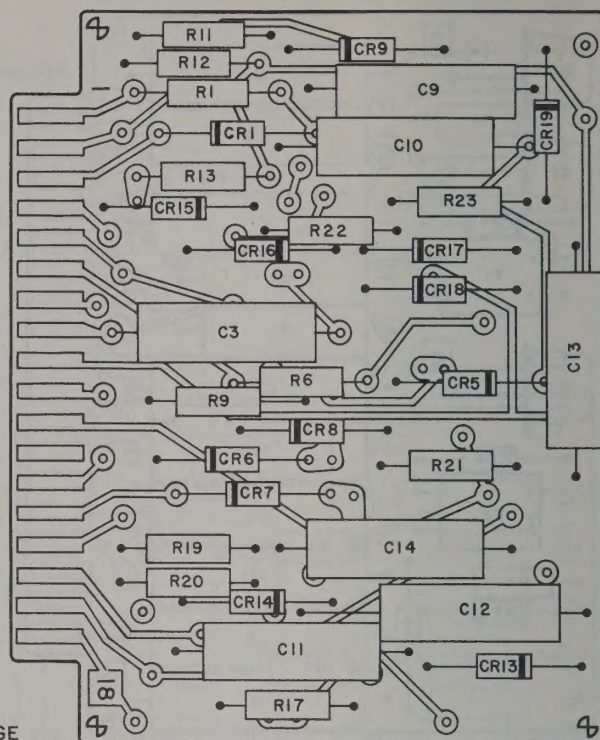
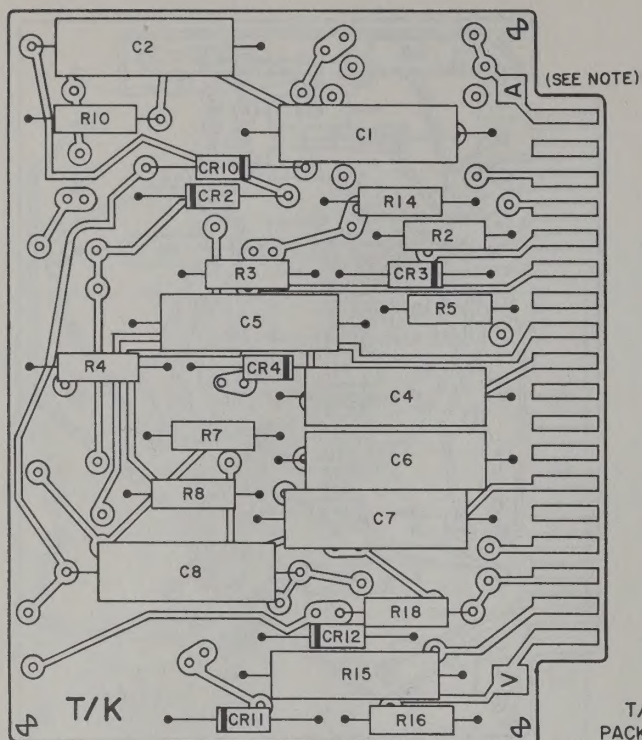
NOTE:
TERMINAL DESIGNATION
G, I, O, AND Q ARE NOT USED.



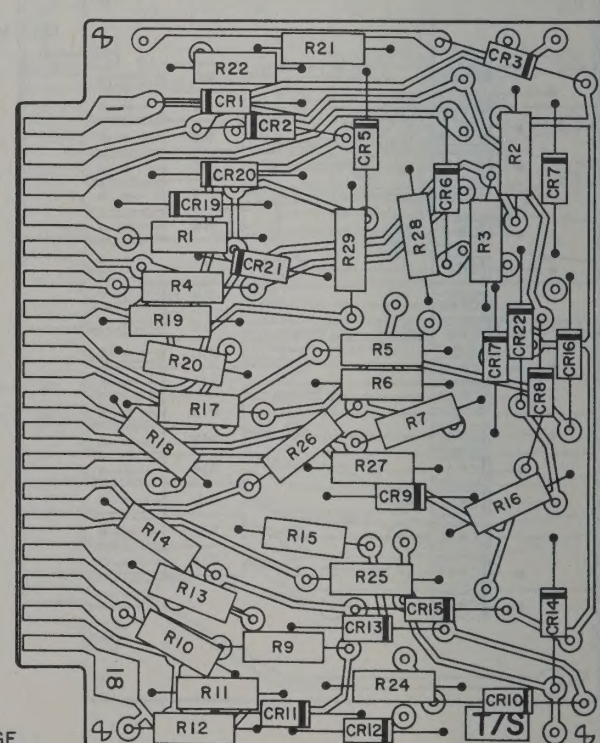
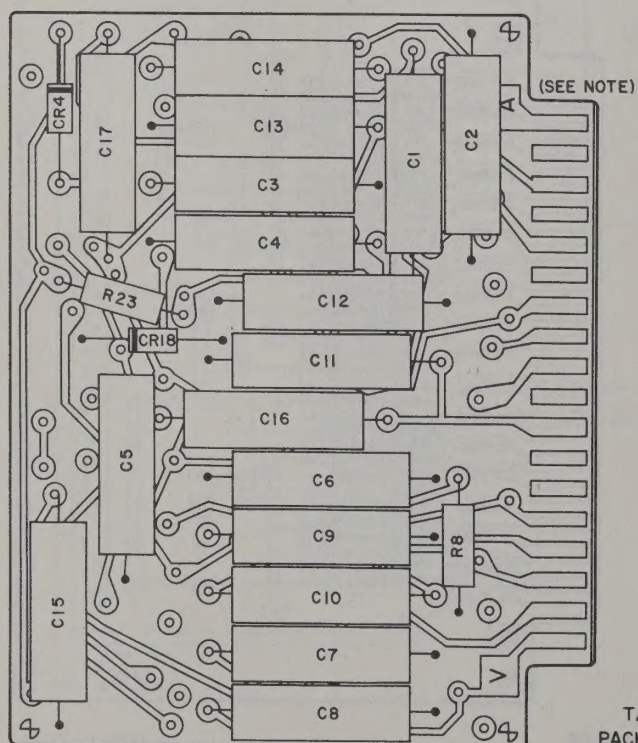
T/R PACKAGE

TM 5840-219-35-131

Figure 149. Transmitter unit subassemblies MX-2341A/G and MX-2688/G, parts location.

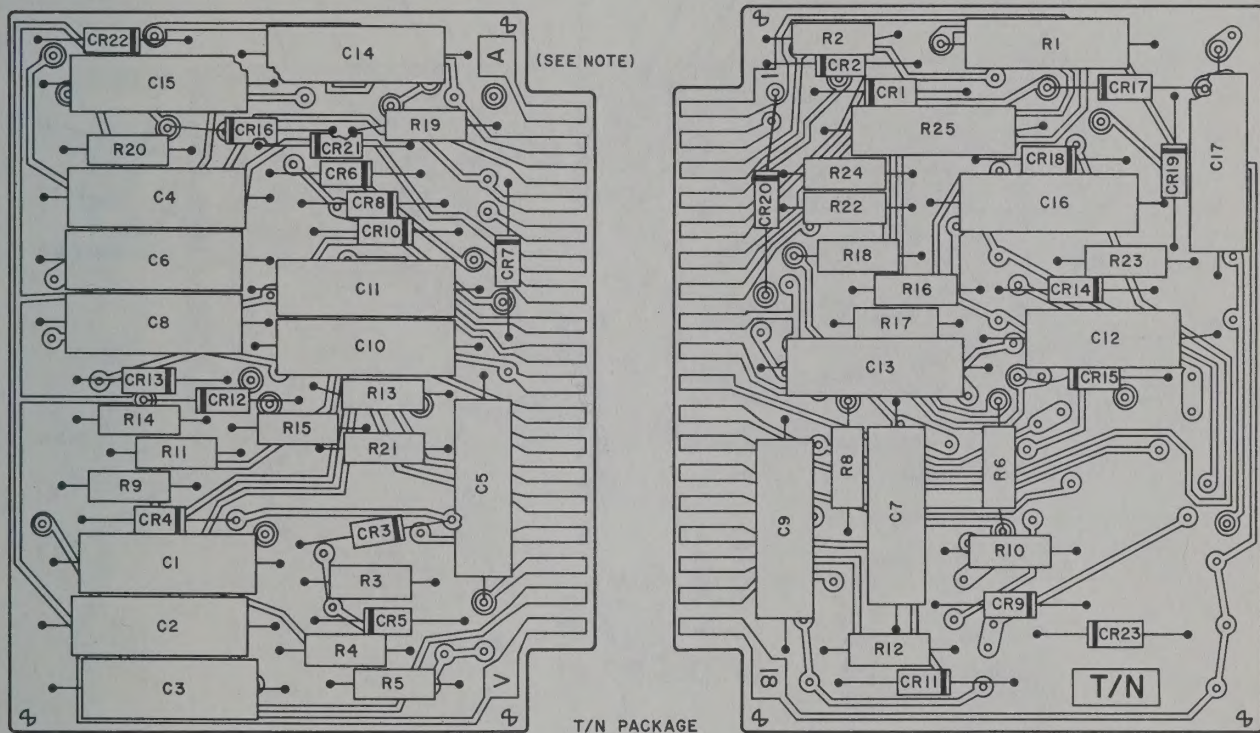


NOTE:
TERMINAL DESIGNATIONS G, I, O, AND Q
ARE NOT USED.



TM 5840-219-35-132

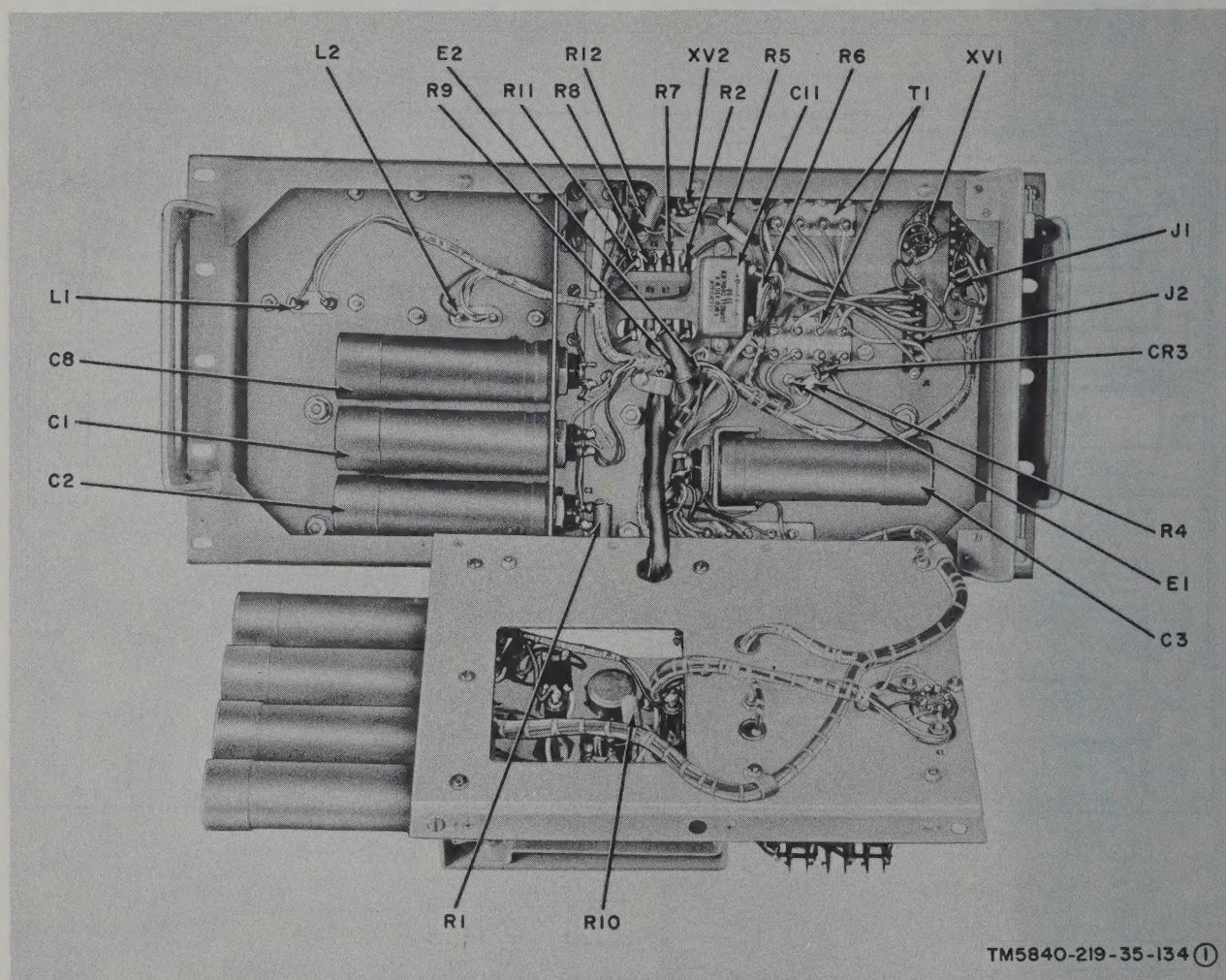
Figure 150. Transmitter unit subassemblies MX-2342A/G and MX-2689/G, parts location.



NOTE:
 TERMINAL DESIGNATIONS G, I, O,
 AND Q ARE NOT USED.

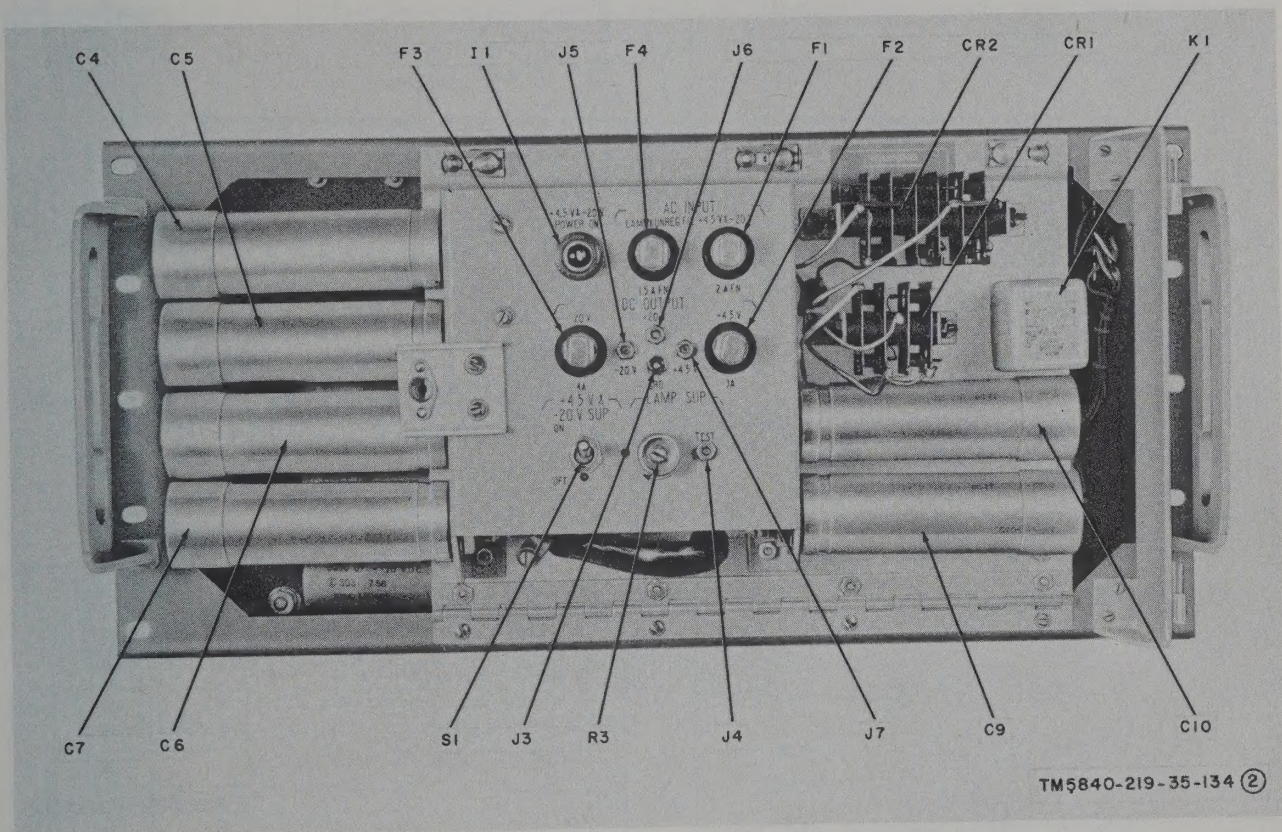
TM 5840-219-35-133

Figure 151. Transmitter unit subassembly MX-2689A/G, parts location.



Parts location

Figure 152. Power supply PP-2235/G.



Parts location

Figure 152—Continued.

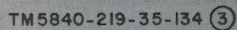
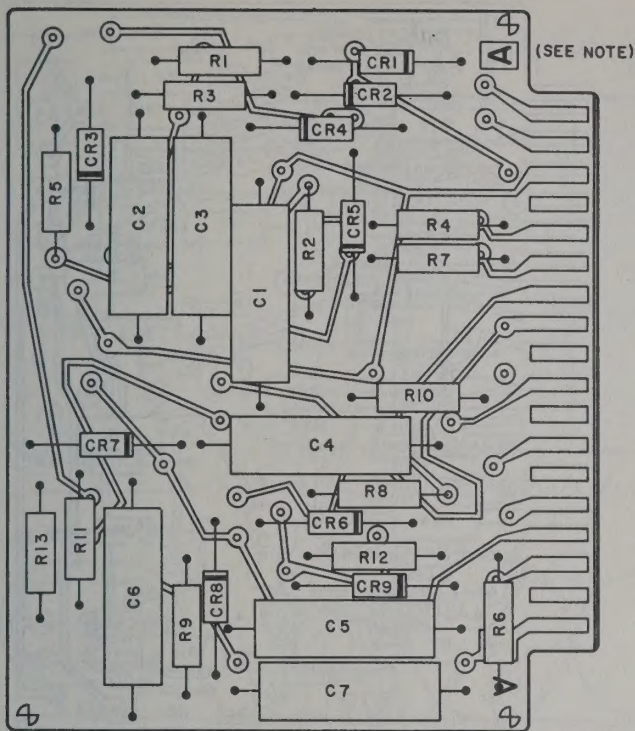
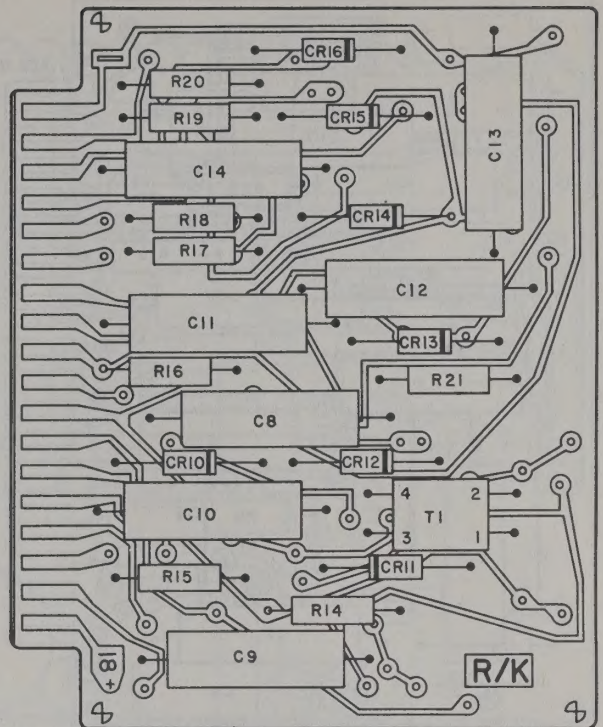


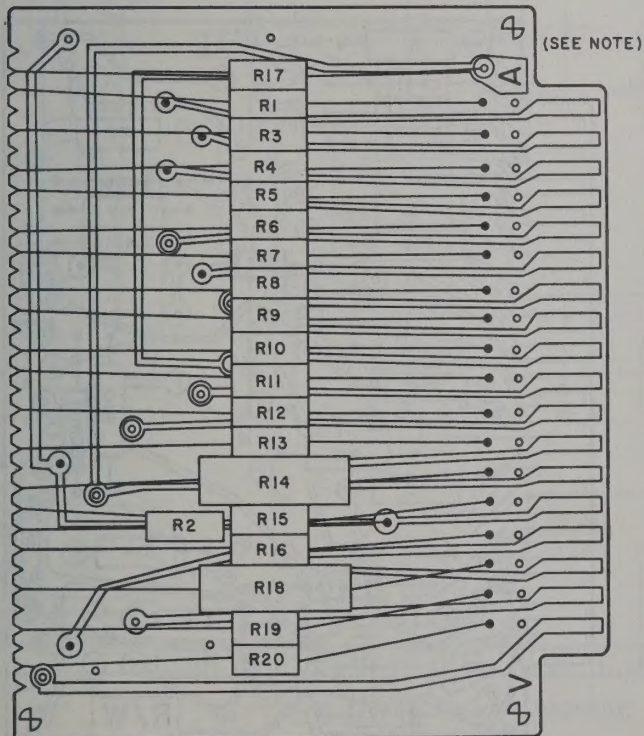
Figure 152—Continued.



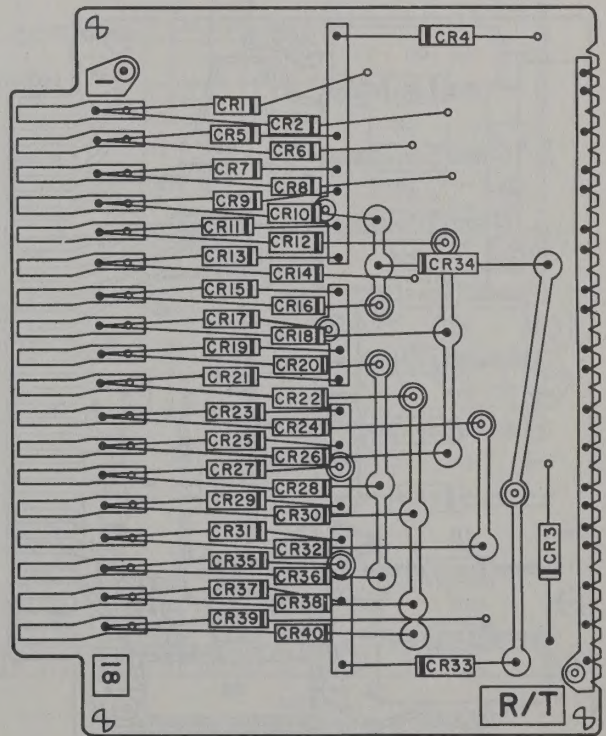
R/K PACKAGE



NOTE:
TERMINAL DESIGNATIONS G, I, O, AND Q
ARE NOT USED.

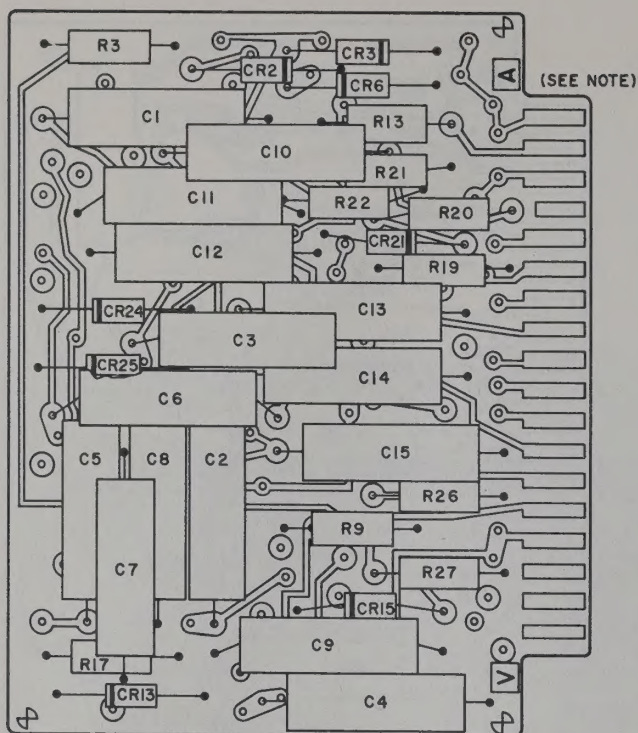


R/T PACKAGE

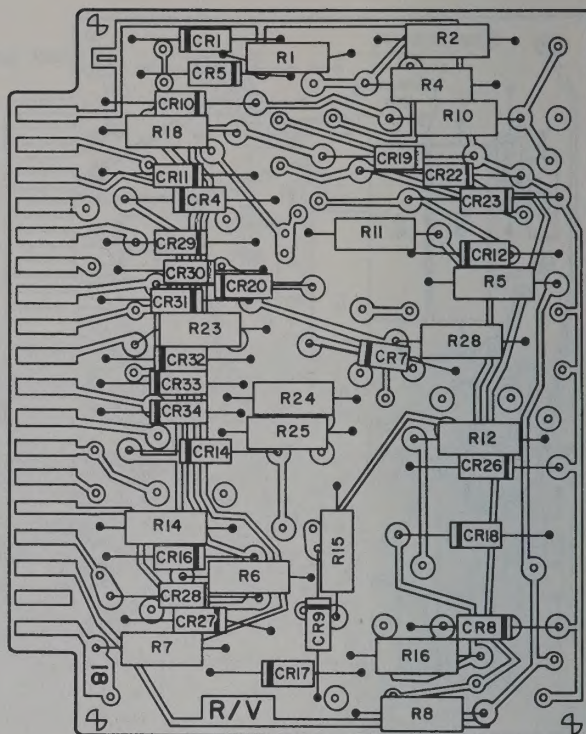


TM 5840-219-35-135

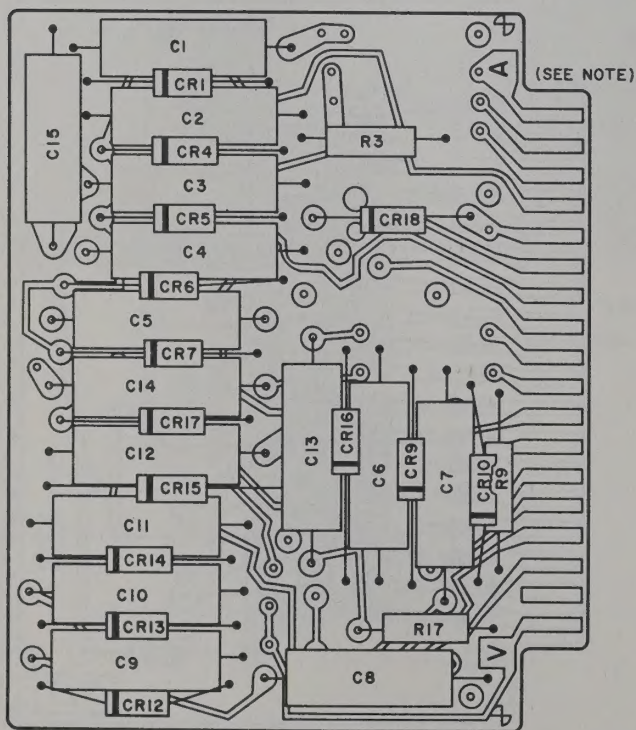
Figure 153. Receiver unit subassemblies MX-2351A/G and MX-2685/G, parts location.



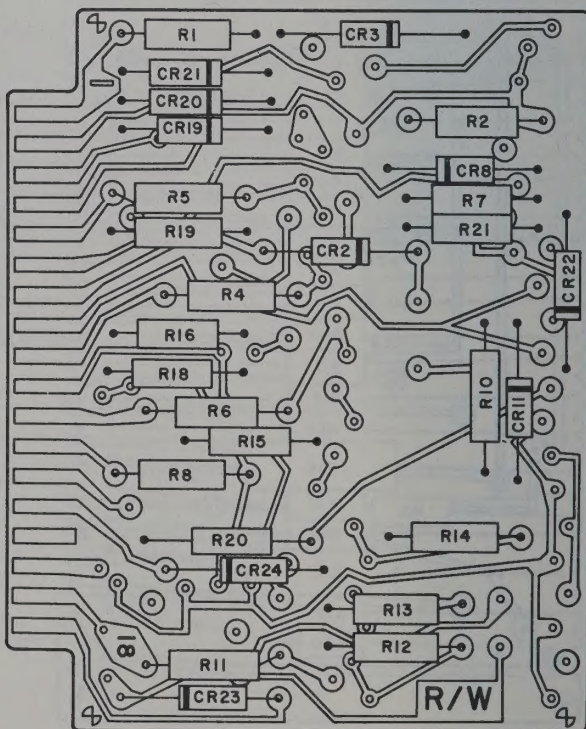
R/V PACKAGE



NOTE:
TERMINAL DESIGNATIONS G, I, O,
AND Q, ARE NOT USED.



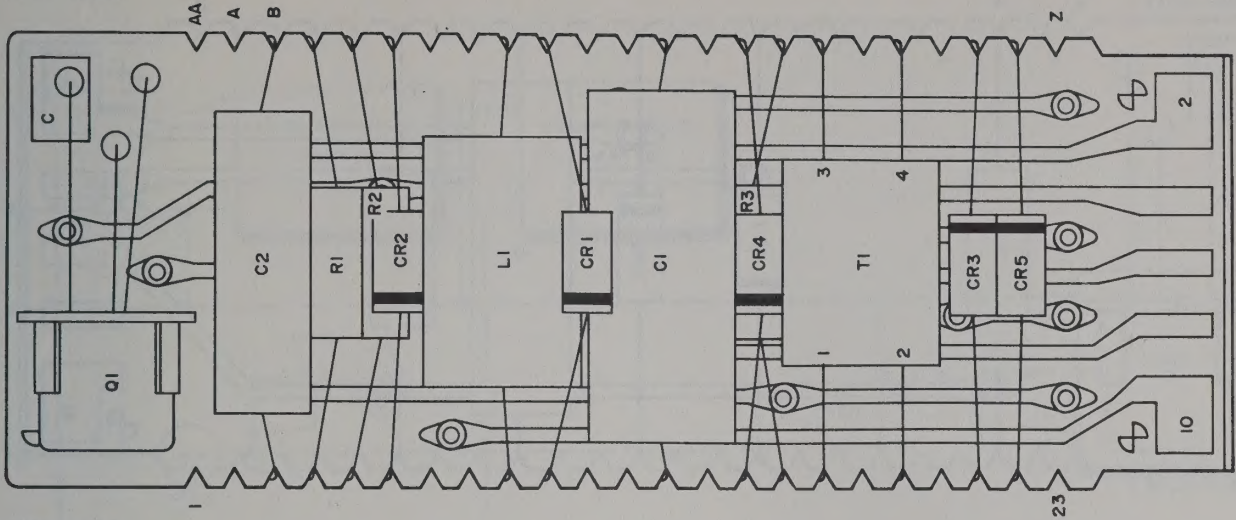
R/W PACKAGE



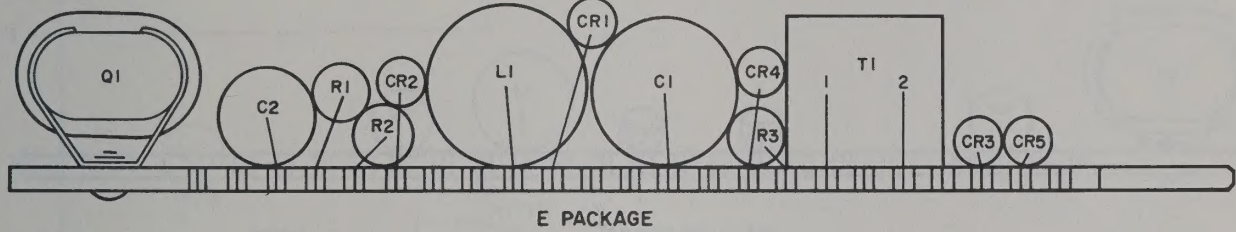
TM 5840-219-35-136

Figure 154. Receiver unit subassemblies MX-2686/G and MX-2687/G, parts location.

(SEE NOTE)

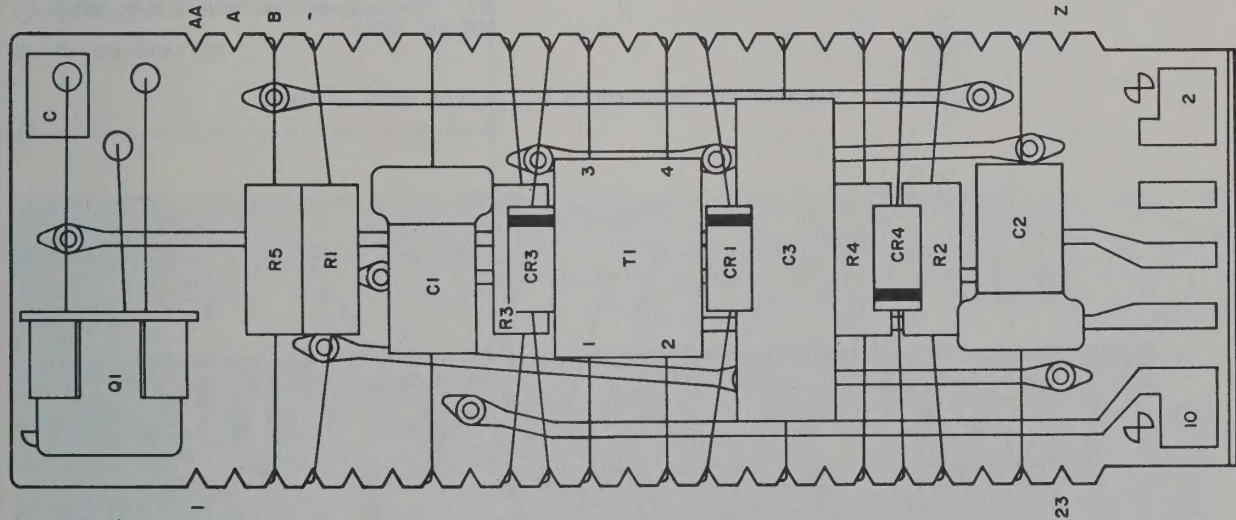


(SEE NOTE)

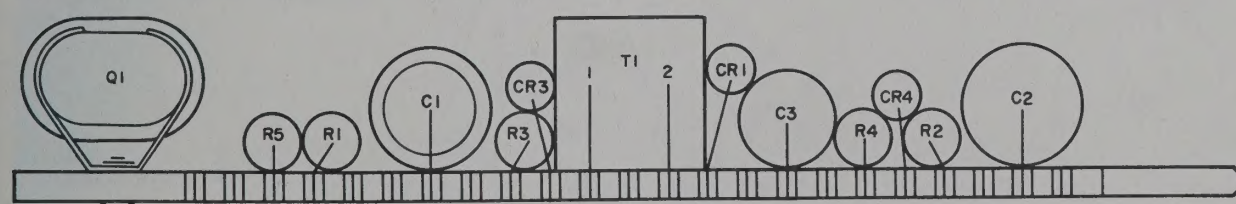


E PACKAGE

(SEE NOTE)



(SEE NOTE)

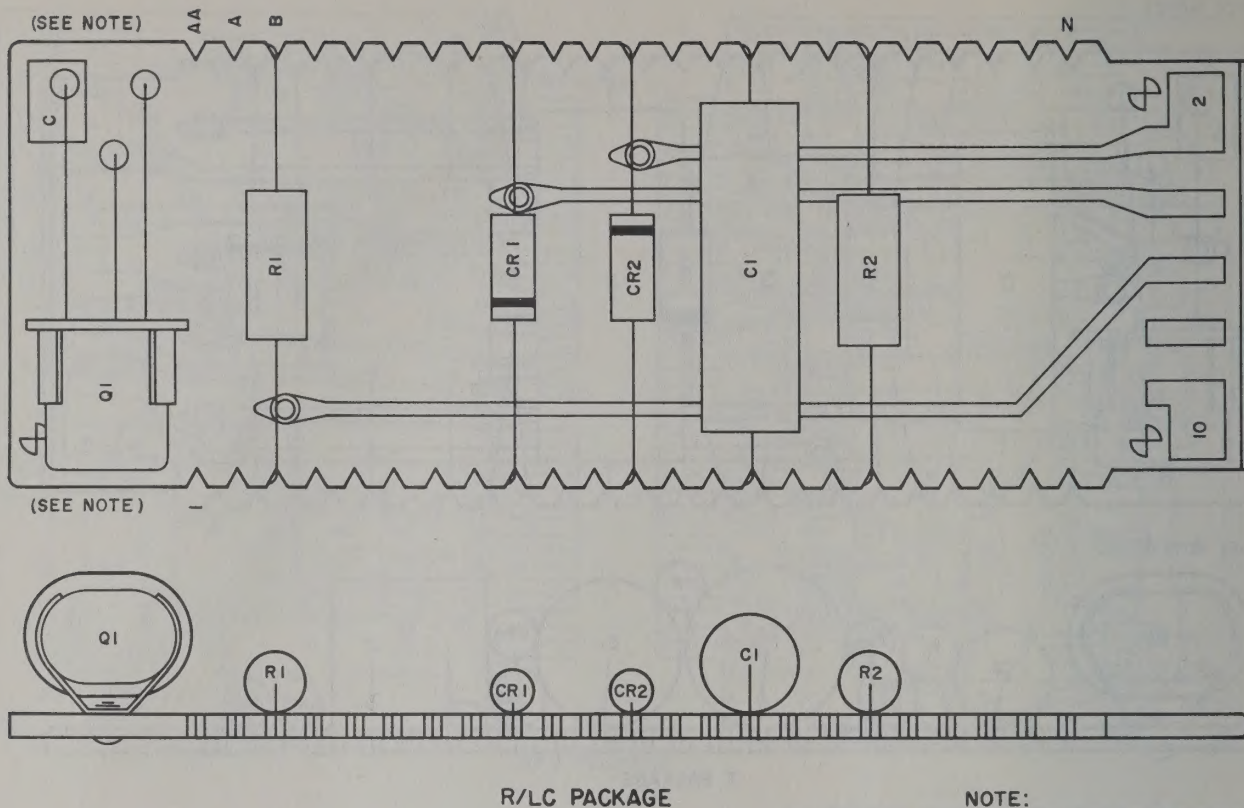


J PACKAGE

NOTE:
TERMINAL DESIGNATIONS I, O, Q, AND X
ARE NOT USED. LETTERS AND NUMBERS
ARE FOR REFERENCE ONLY.

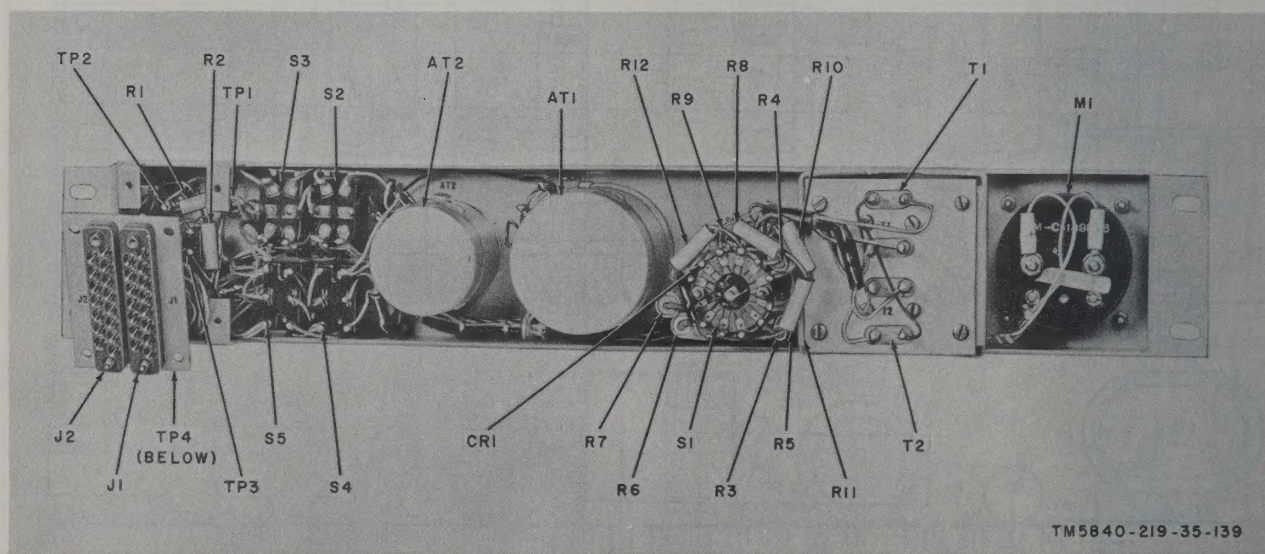
TM5840-219-35-137

Figure 155. Pulse generators SG-261A/G and SG-258A/G, parts location.



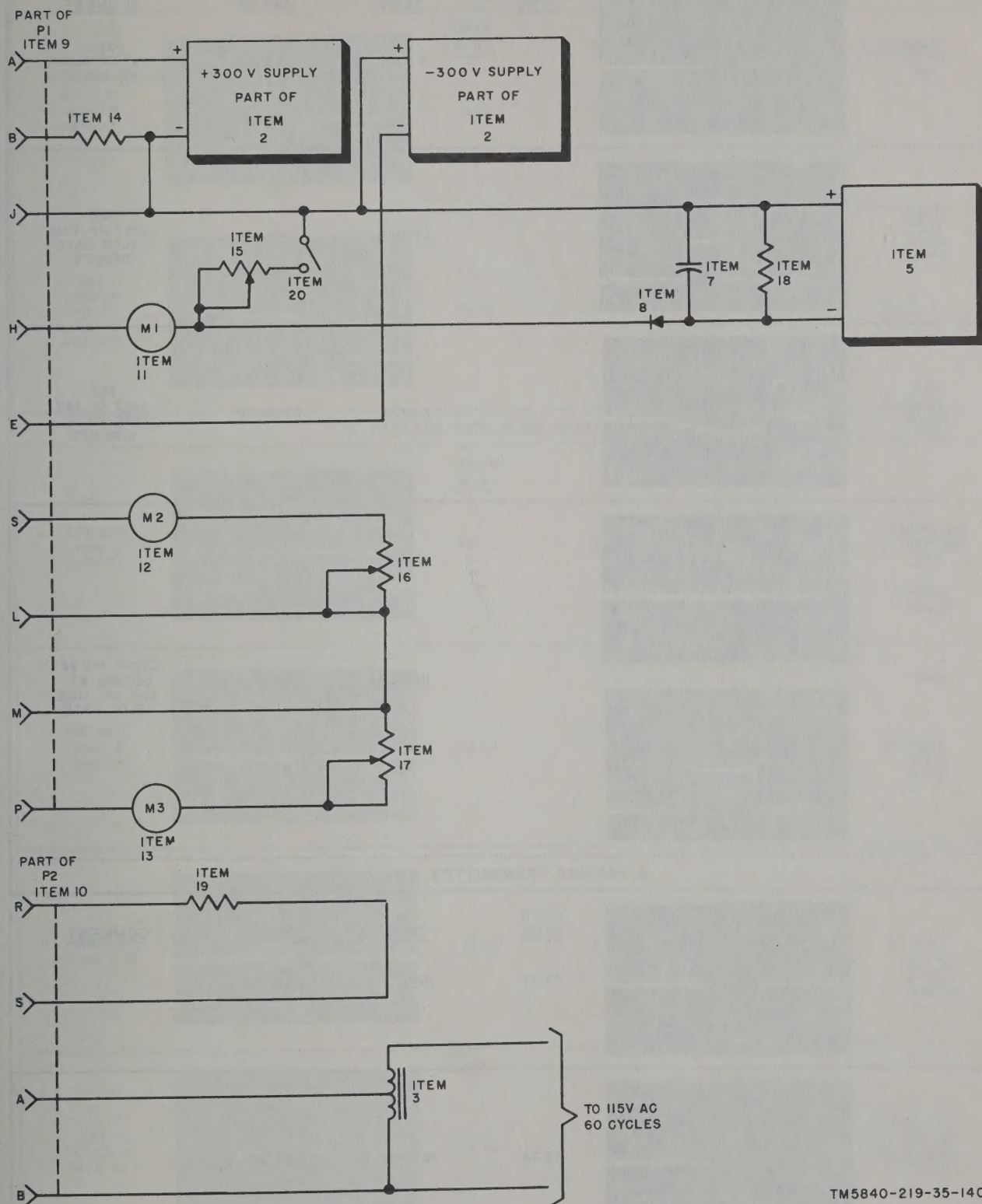
TM 5840-219-35-138

Figure 156. Receiver unit subassembly MX-2684/G, parts location.



TM5840-219-35-139

Figure 157. Electrical test panel SB-976/TSQ-36, parts location.



TM5840-219-35-140

Figure 158. Test set for low voltage power supply.

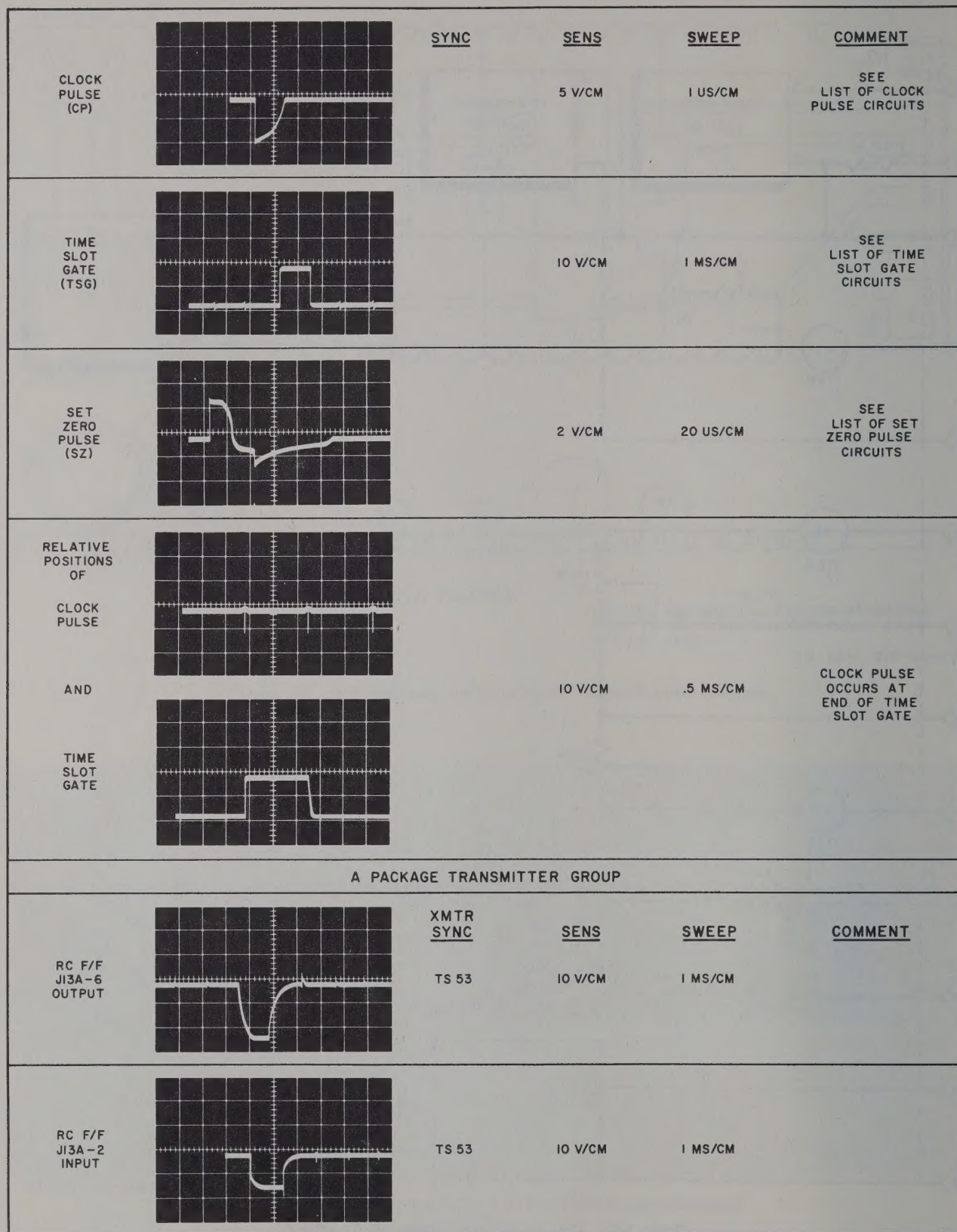
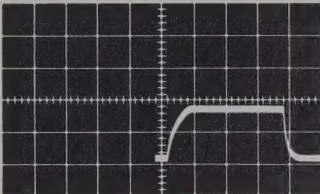
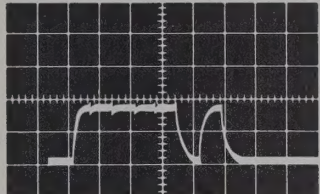
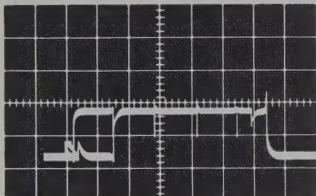
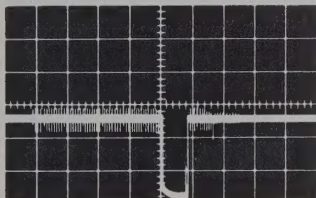
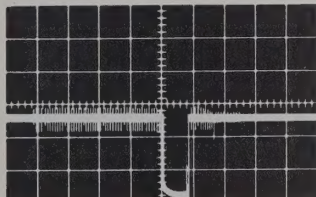
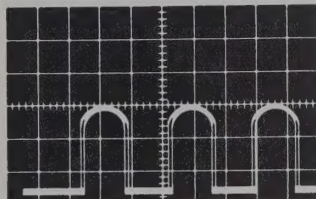


Figure 159. Waveforms.

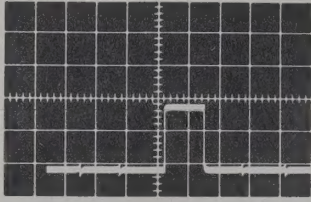
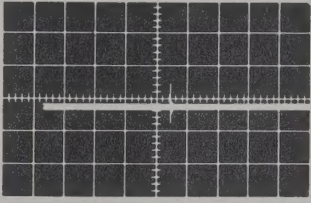
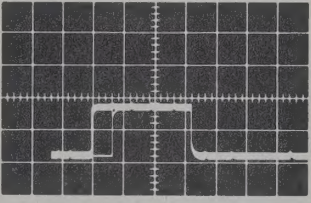
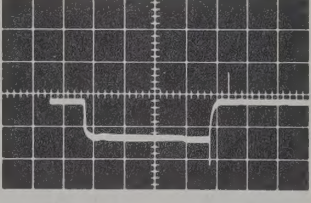
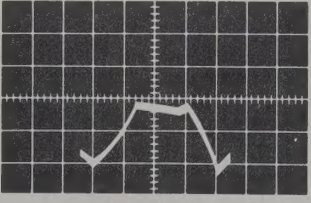
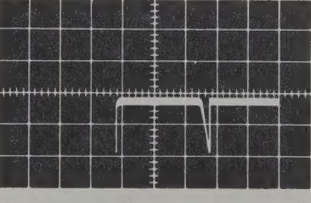
TM 5840-219-35-141 (1)

A PACKAGE TRANSMITTER GROUP (CONT)					
	<u>XMTR SYNC</u>	<u>SENS</u>	<u>SWEEP</u>	<u>COMMENT</u>	
RTC F/F J24A-3 OUTPUT		TS 53	10 V/CM	1 MS/CM	
SR2 J45B-5 INPUT J45B-6 OUTPUT		TS 53	10 V/CM	2 MS/CM	SYNC WORD
A PACKAGE AMPLIFIER SYNCHRONIZER					
	<u>RCVR SYNC</u>				
F/F NO.2 J15B-2 INPUT		TS 58	10 V/CM	1 MS/CM	JITTER
F/F NO.3 J10B-2 INPUT		TS 58	5 V/CM	2 MS/CM	JITTER
J10B-3 F/F NO.3 IN		TS 58	5 V/CM	2 MS/CM	JITTER
J16B-5 F/F NO.5 DATA IN		TS 12	5 V/CM	1 MS/CM	H PARALLAX ALTERNATE ONES AND ZEROS

TM 5840-219-35-141 (2)

Figure 159—Continued.

A PACKAGE AMPLIFIER SYNCHRONIZER (CONT)

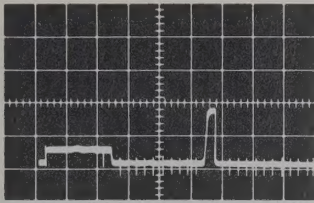
		RCVR SYNC	SENS	SWEEP	COMMENT
J16B-3 F/F NO. 5 DATA OUT		TS 0	10 V/CM	1 MS/CM	AUX NO. 4
J3B-2 F/F NO. 6 IN		TS 47	10 V/CM	.2 MS/CM	JITTER
A PACKAGE RECEIVER GROUP					
J24B-5 RC 1 F/F IN		TS 46	10 V/CM	2 MS/CM	SYNC WORD JITTER
J25B-2 RC 2 F/F IN		TS 46	10 V/CM	2 MS/CM	
J32B-6 PSR OUT		TS 10	5 V/CM	1 MS/CM	NO. 5 H PARALLAX
J16A-6 SPD F/F OUT		TS 10	10 V/CM	1 MS/CM	

TM 5840-219-35-141 (3)

Figure 159—Continued.

A PACKAGE RECEIVER GROUP (CONT)

J15A-5
CS F/F IN



RCVR
SYNC

TS 46

SENS

10 V/CM

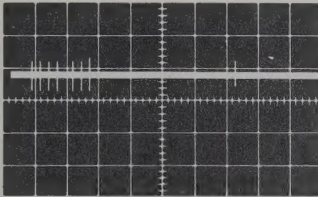
SWEEP

5 MS/CM

COMMENT

NO. 2 H
PARALLAX

J45-7
SR 13 IN



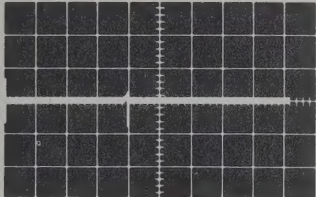
TS 0

5 V/CM

5 MS/CM

B PACKAGE TRANSMITTER GROUP

J68-3
UR O IN



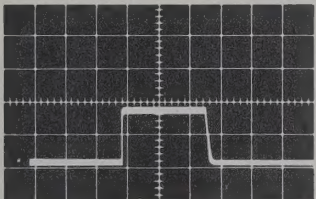
XMTR
SYNC

TS 56

10 V/CM

.2 MS/CM

J6B-5
UR O OUT



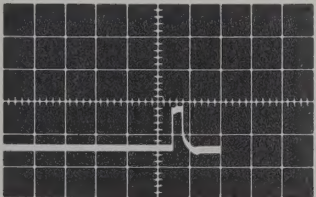
TS 56

10 V/CM

.5 MS/CM

C PACKAGE TRANSMITTER GROUP

J14A-4
PFD F/O OUT

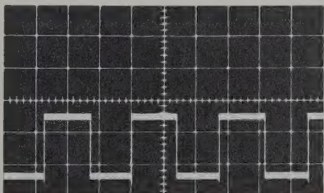


TS 7

10 V/CM

.1 MS/CM

J14A-6
PFD F/O IN



INT-

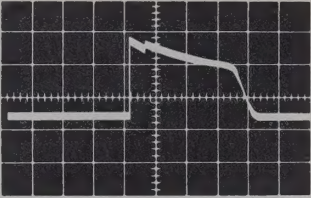
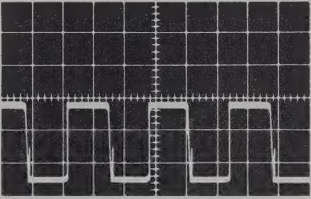
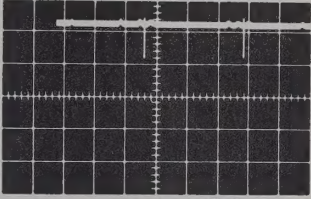
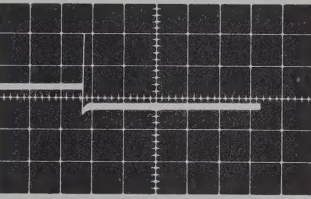
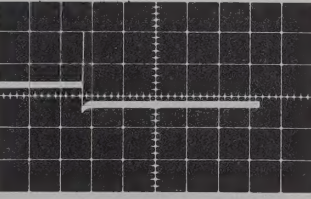
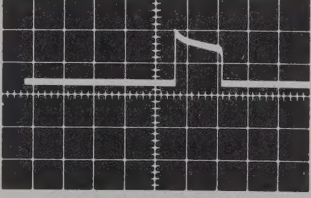
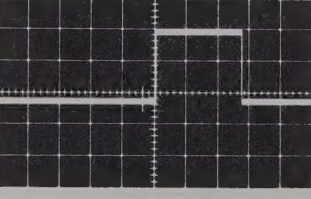
5 V/CM

.5 MS/CM

TM 5840-219-35-141 (4)

Figure 159—Continued.

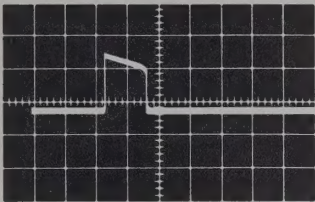
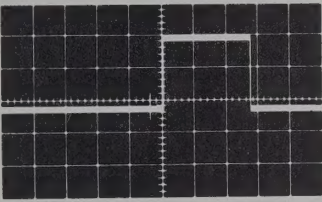
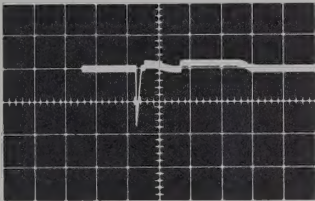
C PACKAGE TRANSMITTER GROUP (CONT)

		<u>XMTR SYNC</u>	<u>SENS</u>	<u>SWEEP</u>	<u>COMMENT</u>
J14A-3 PFD F/O OUT		TS 7	5 V/CM	10 MS/CM	
J14A-2 PFD F/O IN		TS 7	5 V/CM	.5 MS/CM	
J16A-8 ESP F/O IN		TS 7	2 V/CM	5 MS/CM	
J16A-3 ESP F/O OUT		TS 5	10 V/CM	.5 MS/CM	
J18A-3 ERP F/O OUT		TS 14	10 V/CM	.5 MS/CM	
J24B-3 RTC F/O OUT		TS 0	10 V/CM	20 US/CM	
J43-2 BC 13 F/O IN		TS 0	5 V/CM	.5 MS/CM	

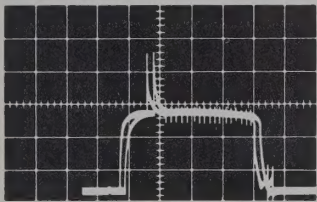
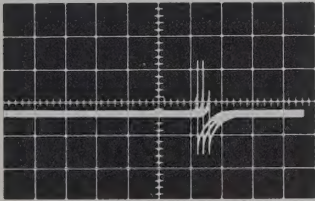
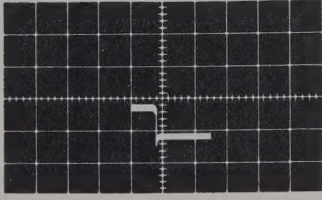
TM 5840-219-35-141 (5)

Figure 159—Continued.

C PACKAGE TRANSMITTER GROUP (CONT)

		<u>XMTR SYNC</u>	<u>SENS</u>	<u>SWEEP</u>	<u>COMMENT</u>
J43-3 BC 13 F/O OUT		TS 0	10 V/CM	20 US/CM	
J43-6 BC 13 F/O IN		TS 0	5 V/CM	.5 MS/CM	
J43-8 BC 13 F/O IN		TS 0	5 V/CM	20 US/CM	

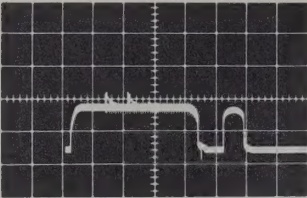
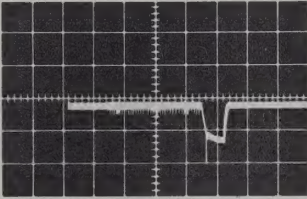
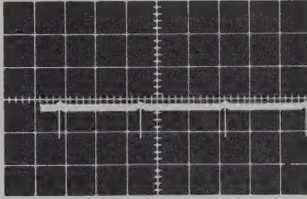
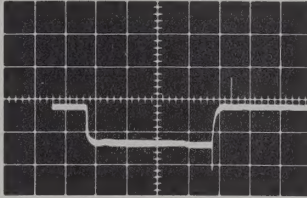
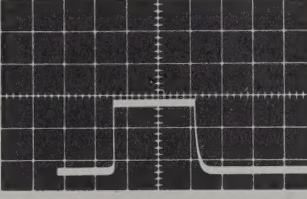
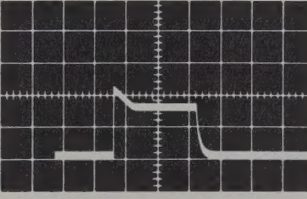
C PACKAGE AMPLIFIER SYNCHRONIZER

		<u>RCVR SYNC</u>			
J12A-2 F/O NO. 1 IN		TS 58	5 V/CM	1 MS/CM	JITTER
J12A-3 F/O NO. 1 OUT		TS 58	10 V/CM	1 MS/CM	JITTER
J15A-2 F/O NO. 2 IN		TS 45	10 V/CM	1 MS/CM	JITTER

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Figure 159—Continued.

C PACKAGE AMPLIFIER SYNCHRONIZER (CONT)

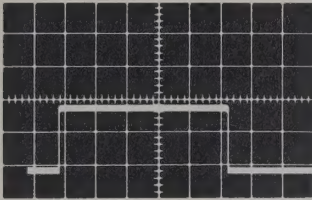
		RCVR SYNC	SENS	SWEEP	COMMENT
J10A-2 F/O NO. 3 IN		TS 46	10 V/CM	2 MS/CM	SYNC WORD
J3A-2 F/O NO. 6 IN		TS 46	10 V/CM	2 MS/CM	
J6A-2 F/O NO. 7 IN		TS 46	10 V/CM	.5 MS/CM	
C PACKAGE RECEIVER GROUP					
J53A-2 RC I F/O IN		TS 46	10 V/CM	2 MS/CM	
D PACKAGE TRANSMITTER GROUP					
J27A-3 HRLU F/F OUT		XMTR SYNC	TS 0	10 V/CM	5 MS/CM
J27A-6 HRLU F/F OUT		TS 48	10 V/CM	5 MS/CM	

TM 5840-219-35-141 ⑦

Figure 159—Continued.

D PACKAGE RECEIVER GROUP

J47-3
SLU HG OUT



RCVR
SYNC

SENS

SWEEP

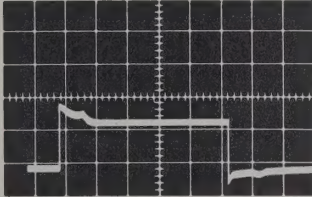
COMMENT

TS 18

10 V/CM

2 MS/CM

J47-6
SLU HG OUT

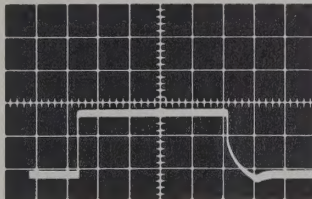


TS 18

10 V/CM

2 MS/CM

J46-3
SLU HF OUT

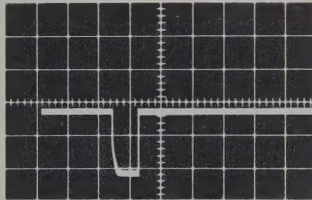


TS 18

10 V/CM

2 MS/CM

J53B-5
FLU IN



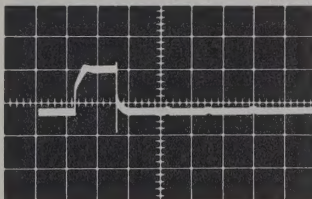
TS 30

10 V/CM

5 MS/CM

E PACKAGE TRANSMITTER GROUP

J28B-7
SRC F/O



XMTR
SYNC

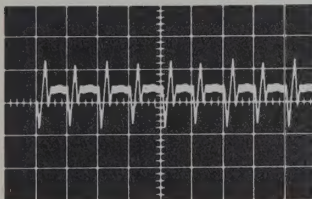
TS 26

5 V/CM

1 MS/CM

K PACKAGE TRANSMITTER GROUP

J44A-4
BC I F/F IN



INT +

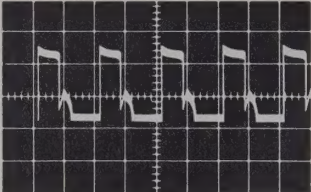
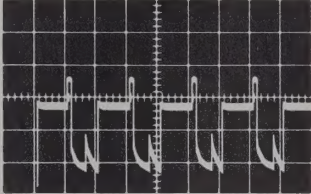
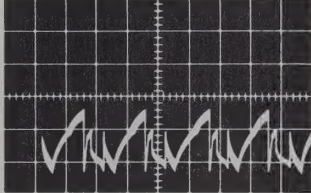
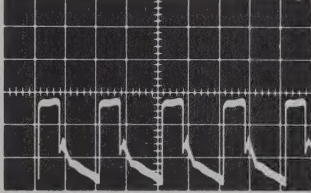
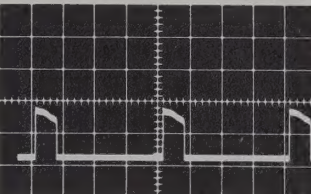
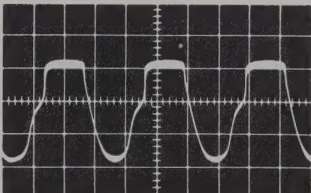
10 V/CM

10 MS/CM

Figure 159—Continued.

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K PACKAGE TRANSMITTER GROUP (CONT)

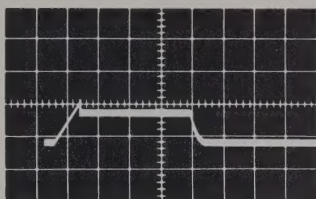
		<u>XMTR SYNC</u>	<u>SENS</u>	<u>SWEEP</u>	<u>COMMENT</u>
J44A-5 BC 1 F/F IN		INT +	5 V/CM	10 US/CM	
J44A-6 BC 1 F/F OUT		INT +	5 V/CM	10 US/CM	
J44A-2 BC 1 F/F OUT		INT +	5 V/CM	10 US/CM	
J45A-8 BC 2 F/F IN		INT +	5 V/CM	10 US/CM	
L PACKAGE TRANSMITTER GROUP					
J32-3 BC 2 F/O OUT		TS 52	5 V/CM	10 US/CM	
AMPLIFIER SYNCHRONIZER					
E1 1,500-CYCLE OSCILLATOR		<u>RCVR SYNC</u> INT -	5 V/CM	.2 MS/CM	

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Figure 159—Continued.

AMPLIFIER SYNCHRONIZER (CONT)

E2
EMITTER
DELAY F/F



RCVR
SYNC

SENS

SWEEP

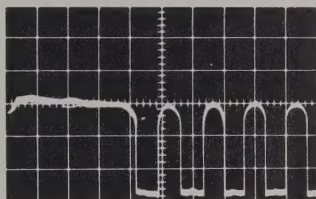
COMMENT

TS 0

10 V/CM

1 MS/CM

E3
DATA SLICER
OUTPUT



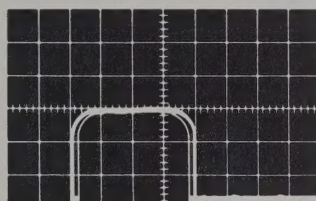
TS 0

5 V/CM

2 MS/CM

SYNC WORD
AND DATA

E4
READY SLICER
OUTPUT



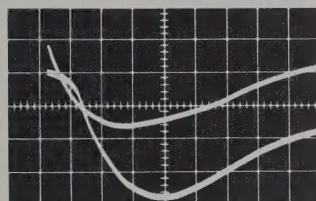
TS 0

5 V/CM

1 MS/CM

ENCODER

E1
E2
START AND
RESET PULSES



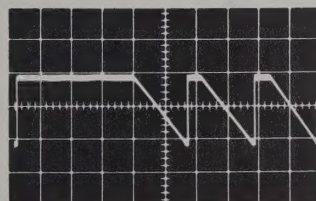
XMTR
SYNC

EXT -

20 V/CM

2 US/CM

TP1
RAMP VOLTAGE



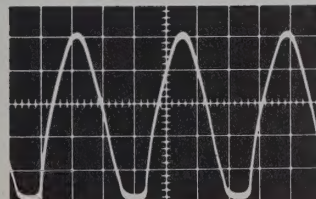
TS 0

50 V/CM

ONE FRAME

MODULATOR

TP1
1,500-CYCLE
OSCILLATOR



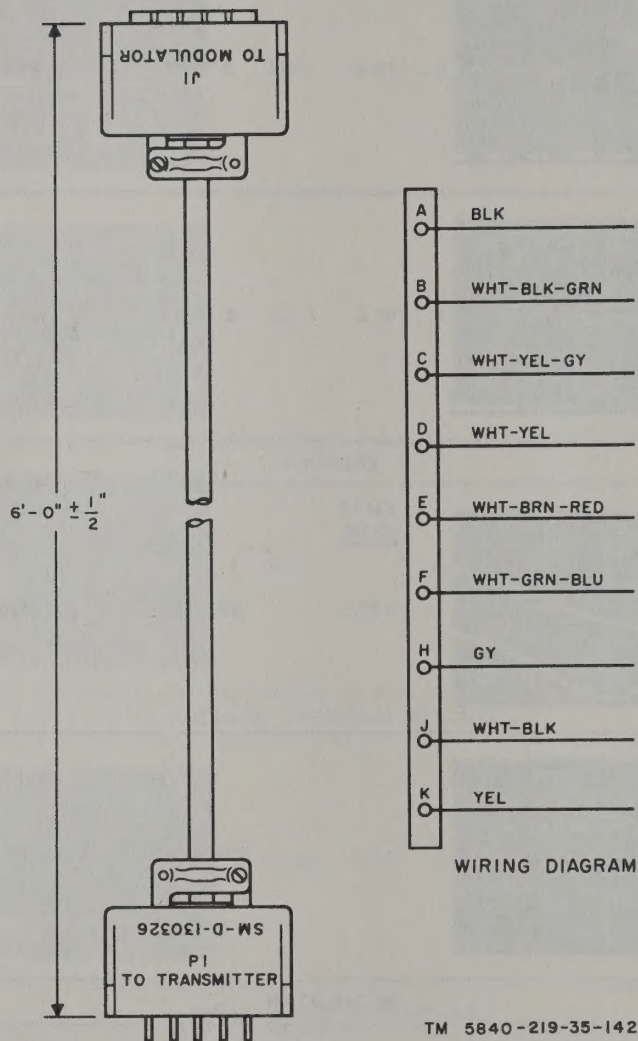
INT -

5 V/CM

.2 MS/CM

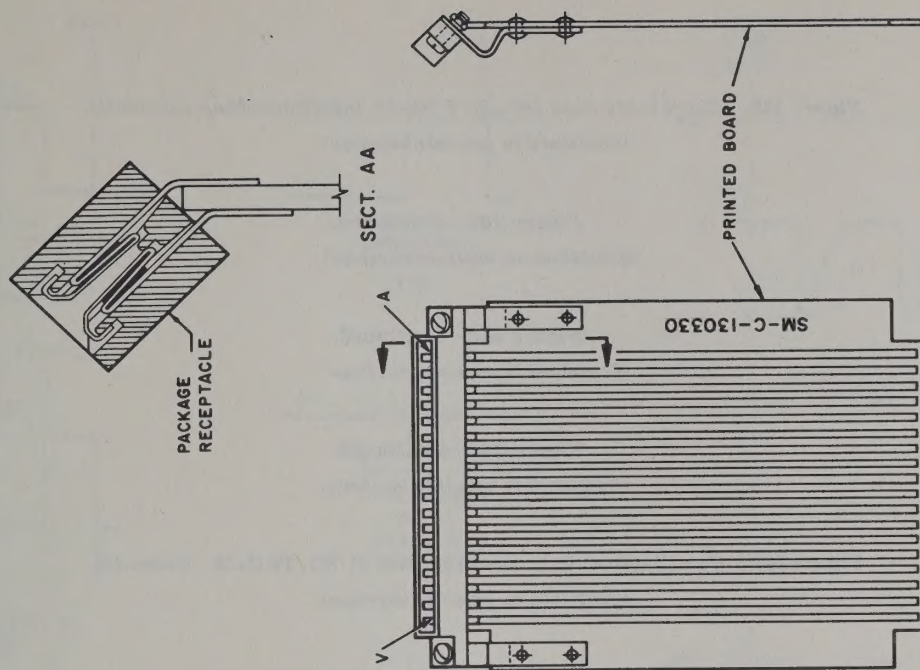
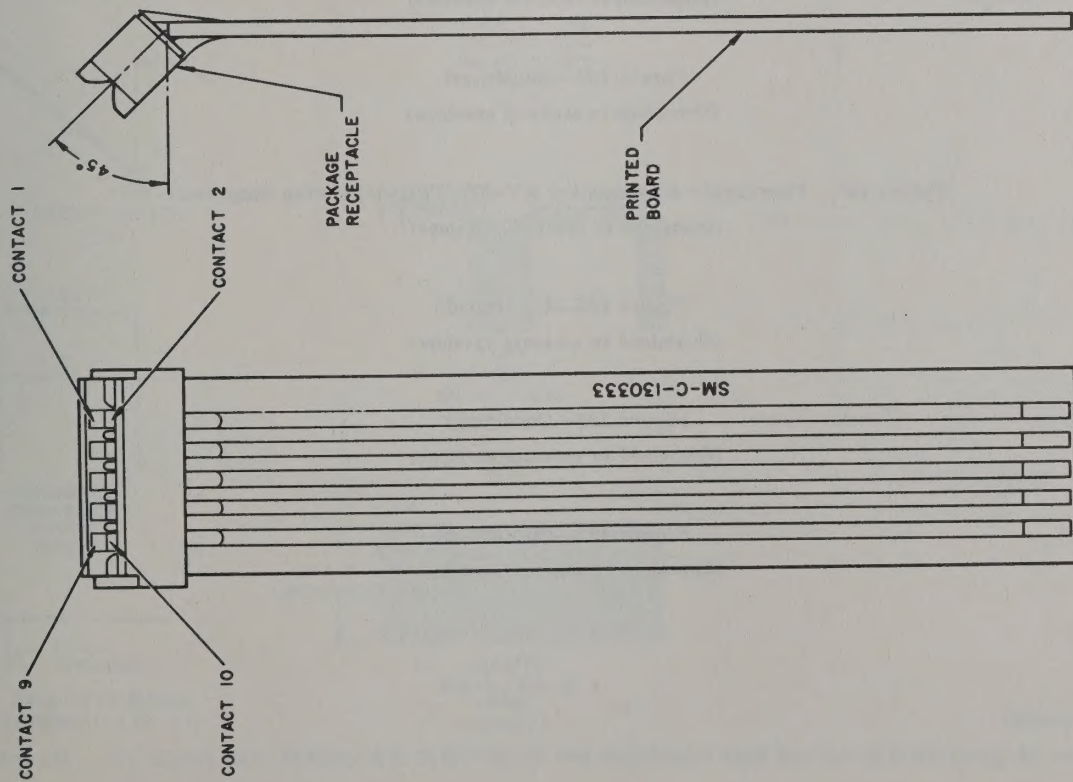
TM 5840-219-35-141 (10)

Figure 159—Continued.



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Figure 160. Special purpose electrical cable assembly.



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Figure 161. SM-C-130333 electrical test adapter and SM-C-130330 electrical test adapter.

Figure 162. Coordinate data set AN/TSQ-36, interconnecting schematic.

(Contained in separate envelope)

Figure 162—Continued.

(Contained in separate envelope)

Figure 162—Continued.

(Contained in separate envelope)

Figure 162—Continued.

(Contained in separate envelope)

Figure 163. Coordinate data transmitter unit T-721/TSQ-36, schematic.

(Contained in separate envelope)

Figure 163—Continued.

(Contained in separate envelope)

Figure 163—Continued.

(Contained in separate envelope)

Figure 164. Coordinate data encoder KY-728/TSQ-36, schematic.

(Contained in separate envelope)

Figure 164—Continued

(Contained in separate envelope)

Figure 165. Coordinate data encoder KY-278/TSQ-36, wiring diagram.

(Contained in separate envelope)

Figure 165—Continued.

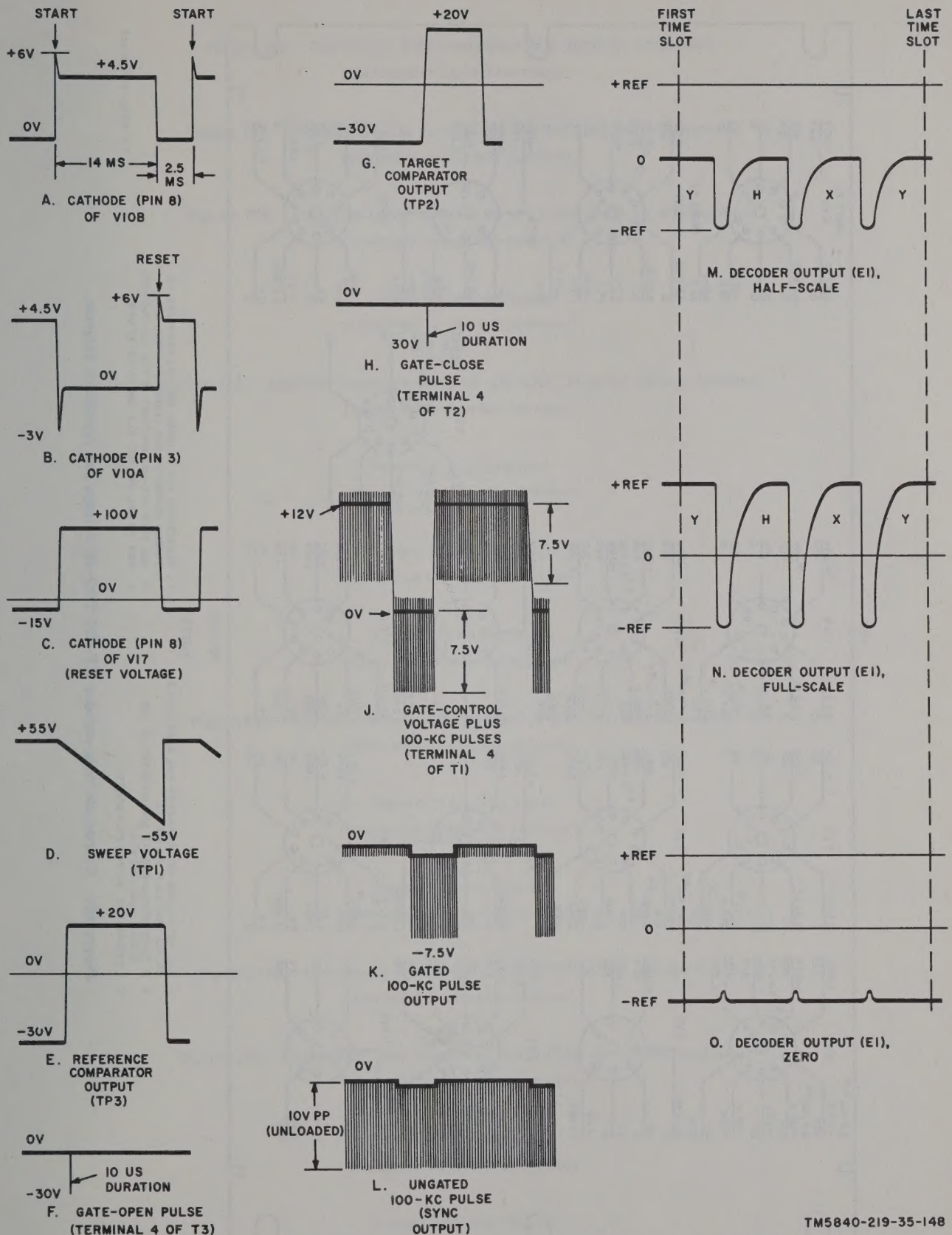
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Figure 165—Continued.

(Contained in separate envelope)

Figure 165—Continued.

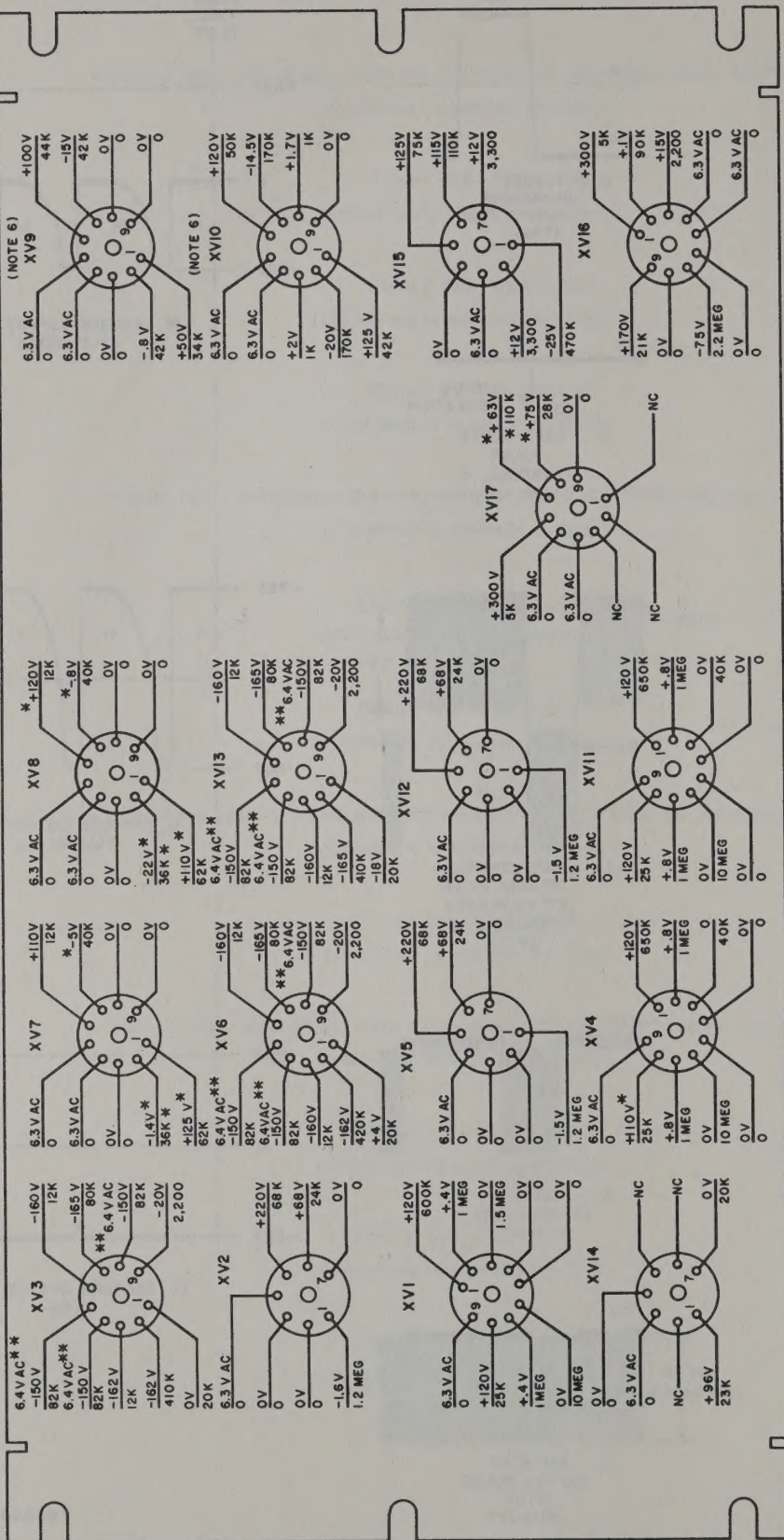
(Contained in separate envelope)



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Figure 166. Coordinate data encoder KY-278/TSQ-36 and coordinate data decoder KY-277/TSQ-36, waveforms.

TOP



- NOTES:**
1. ALL DC VOLTAGE MEASUREMENTS ARE MADE WITH A 20000 OHM/VOLT VOLTMETER.
 2. * THESE MEASUREMENTS ARE AFFECTED BY THE CIRCUIT ADJUSTMENTS.
 3. ** MEASURED ACROSS FILAMENTS.
 4. RESISTANCES ARE IN OHMS AND ARE MEASURED TO CHASSIS GROUND UNLESS OTHERWISE SPECIFIED.
 5. ALL FOUR OPR-ADJ SWITCHES IN THE ADJ POSITION.
 6. FOR V9 AND V10, SET ALL SWITCHES AT OPR.

Figure 167. Coordinate data encoder KY-278/TSQ-36, voltage and resistance diagram.

Figure 168. Coordinate data modulator MD-323A/G, schematic.

(Contained in separate envelope)

Figure 169. Coordinate data modulator MD-323A/G, wiring diagram.

(Contained in separate envelope)

Figure 170. Amplifier-synchronizer unit AM-2126/TSQ-36, schematic.

(Contained in separate envelope)

Figure 170—Continued.

(Contained in separate envelope)

Figure 171. Amplifier-synchronizer unit AM-2126/TSQ-36, wiring diagram.

(Contained in separate envelope)

Figure 171—Continued.

(Contained in separate envelope)

Figure 171—Continued.

(Contained in separate envelope)

Figure 171—Continued.

(Contained in separate envelope)

Figure 172. Coordinate data receiver unit R-930/TSQ-36, schematic.

(Contained in separate envelope)

Figure 172—Continued.

(Contained in separate envelope)

Figure 172—Continued.

(Contained in separate envelope)

Figure 173. Coordinate data decoder KY-277/TSQ-36, schematic.

(Contained in separate envelope)

Figure 174. Coordinate data decoder KY-277/TSQ-36, wiring diagram.

(Contained in separate envelope)

Figure 174—Continued.

(Contained in separate envelope)

Figure 174—Continued.

(Contained in separate envelope)



NOTES:

1. VOLTAGE MEASUREMENTS ARE MADE WITH 20,000 OHMS PER VOLT METER.
2. RESISTANCES ARE IN OHMS AND ARE MEASURED TO CHASSIS GROUND UNLESS OTHERWISE SPECIFIED.
3. * MEASURED TO PIN 9 OF SAME SOCKET.
4. SET IN GROUND LEVEL CODE OF 000 000 001 (NUMBER 10 KEY UP, REST DOWN) FOR H, X, Y OF RECEIVER. TEST PANEL REC LINE ON EXT DEPRESS M5 SWITCH.

Figure 175. Coordinate data decoder KY-277/TSQ-36, voltage and resistance diagram.

Figure 176. Direct current amplifier AM-2125/TSQ-36, schematic.

(Contained in separate envelope)

Figure 177. Direct current amplifier AM-2125/TSQ-36, wiring diagram.

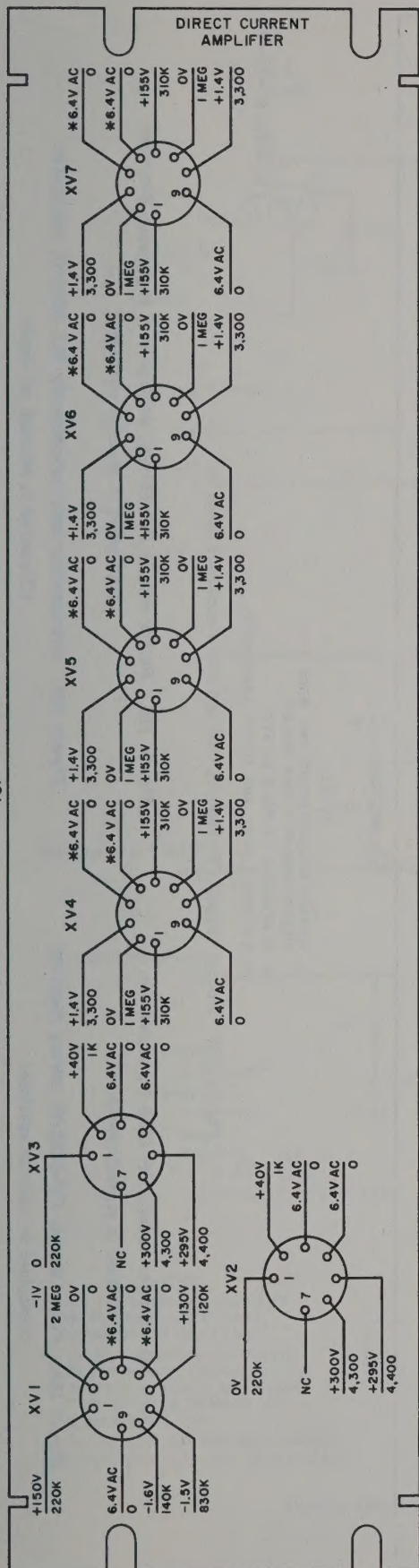
(Contained in separate envelope)

Figure 177—Continued.

(Contained in separate envelope)

Figure 177—Continued.

(Contained in separate envelope)



NOTES:

1. VOLTAGE MEASUREMENTS MADE WITH 20,000 OHMS PER VOLT METER.
2. * MEASURED TO PIN 9 OF SAME SOCKET.
3. RESISTANCES ARE IN OHMS AND ARE MEASURED TO CHASSIS GROUND UNLESS OTHERWISE SPECIFIED.

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Figure 178. Direct current amplifier AM-2125/TSQ-36, voltage and resistance diagram.

Figure 179. Electrical test panel SB-976/TSQ-36, schematic.

(Contained in separate envelope)

Figure 180. Electrical test panel SB-976/TSQ-36, wiring diagram.

(Contained in separate envelope)

Figure 181. Power supply PP-2235/G, schematic.

(Contained in separate envelope)

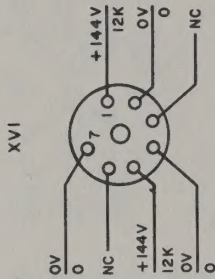
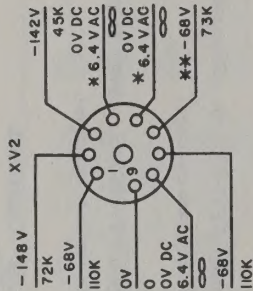
Figure 182. Power supply PP-2235/G, wiring diagram.

(Contained in separate envelope)

Figure 182—Continued.

(Contained in separate envelope)

TOP



POWER
SUPPLY

BOTTOM

NOTES:

1. VOLTAGE MEASUREMENTS ARE MADE WITH 20,000 OHMS PER VOLT METER.
2. * MEASURED TO PIN 8 OF XV2.
3. ** VARIES WITH LAMP SUPPLY ADJUSTMENT.

Figure 183. Power supply PP-2235/G, voltage and resistance diagram.

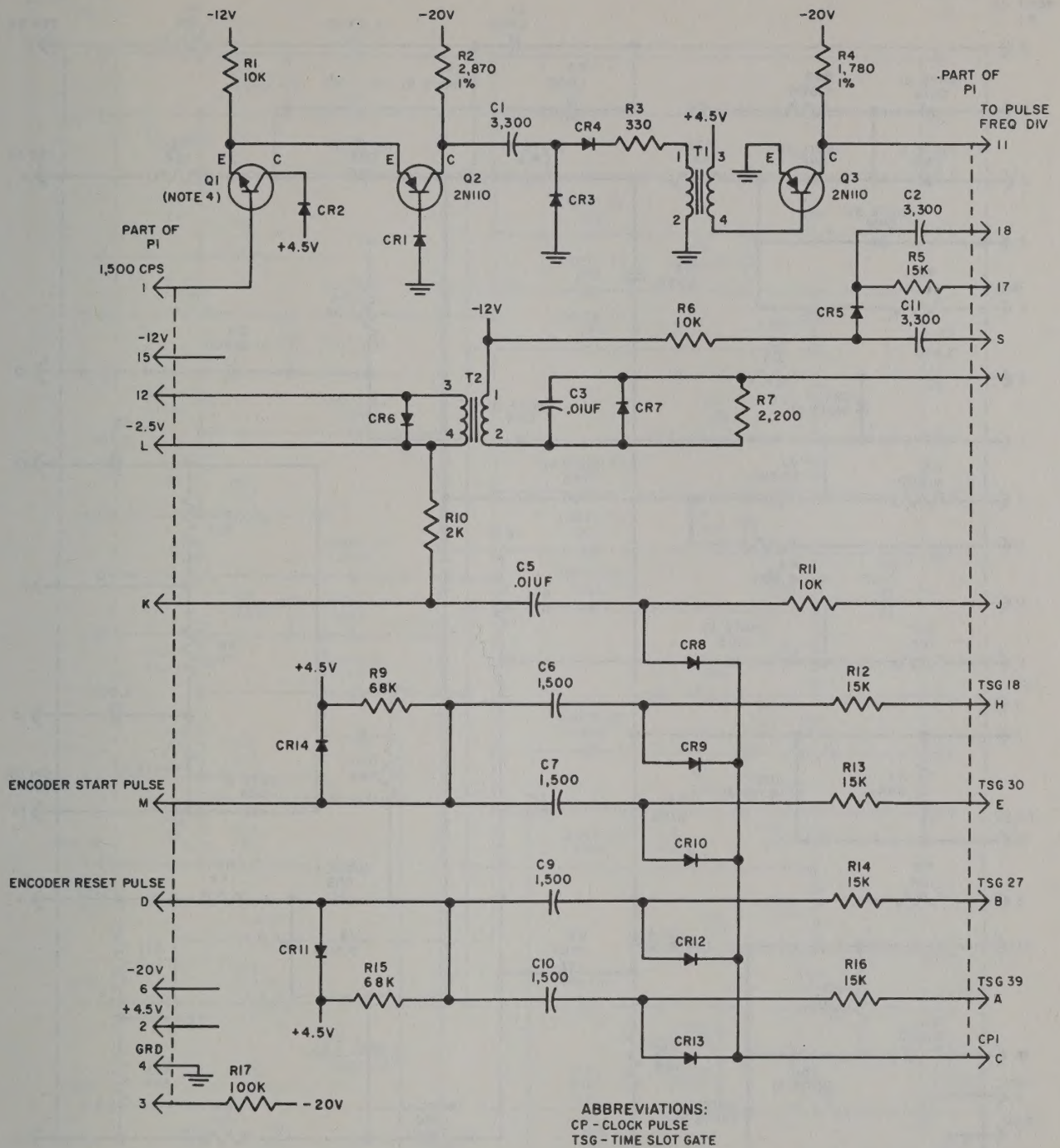
Figure 184. Power supply PP-2236/G, schematic.
(Contained in separate envelope)

Figure 185. Power supply PP-2236/G, wiring diagram.
(Contained in separate envelope)

Figure 186. Power supply PP-2236/G, voltage and resistance diagram.
(Contained in separate envelope)

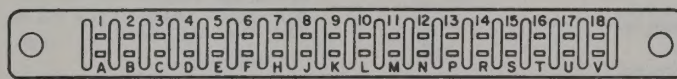
Figure 187. Transmitter unit subassembly MX-2688/G, schematic.
(Contained in separate envelope)

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NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. UNLESS OTHERWISE INDICATED, RESISTORS ARE $\pm 5\%$ TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUES.
3. ALL DIODES ARE PER SM-B-181088
4. TRANSISTOR Q1 IS PER SM-B-182553



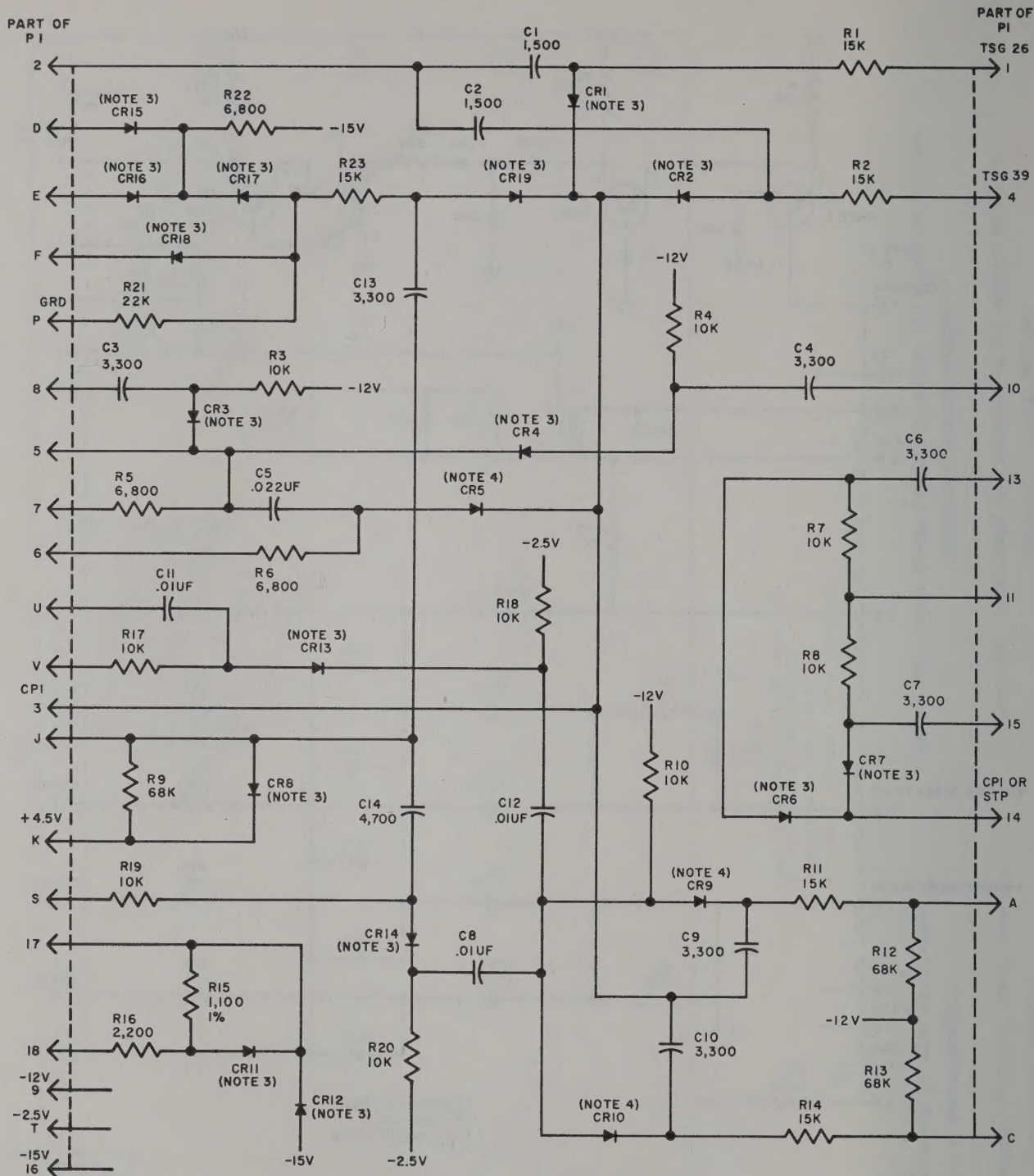
P1
WIRING SIDE

T/J PACKAGE

HIGHEST REFERENCE DESIGNATIONS		
C11	CR14	R17
REFERENCE DESIGNATIONS NOT USED		
C4, C8, R8		

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Figure 188. Transmitter unit subassembly MX-2341A/G, schematic.

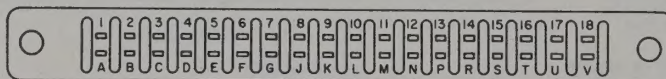


NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. UNLESS OTHERWISE INDICATED, RESISTORS ARE $\pm 5\%$ TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.
3. DIODE PER SM-B-181088.
4. DIODE PER SM-B-181092.

ABBREVIATIONS:

CP - CLOCK PULSE
STP - START TRANSMITTER PULSE
TSG - TIME SLOT GATE



PI
WIRING SIDE

HIGHEST REFERENCE DESIGNATIONS		
C14	CR19	R23

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T/K PACKAGE

Figure 189. Transmitter unit subassembly MX-2342A/G, schematic.

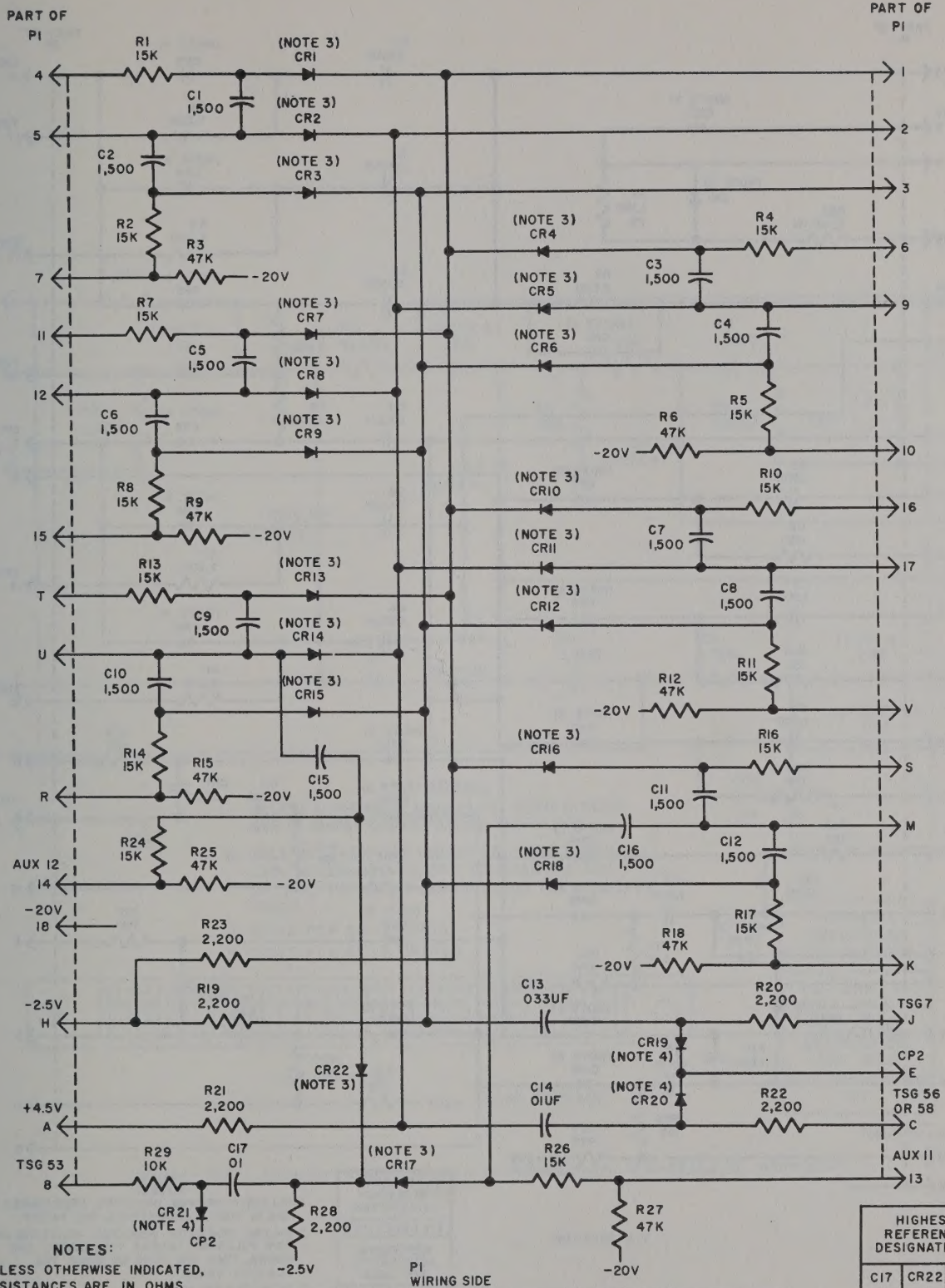


Figure 190. Transmitter unit subassembly MX-2689/G, schematic.

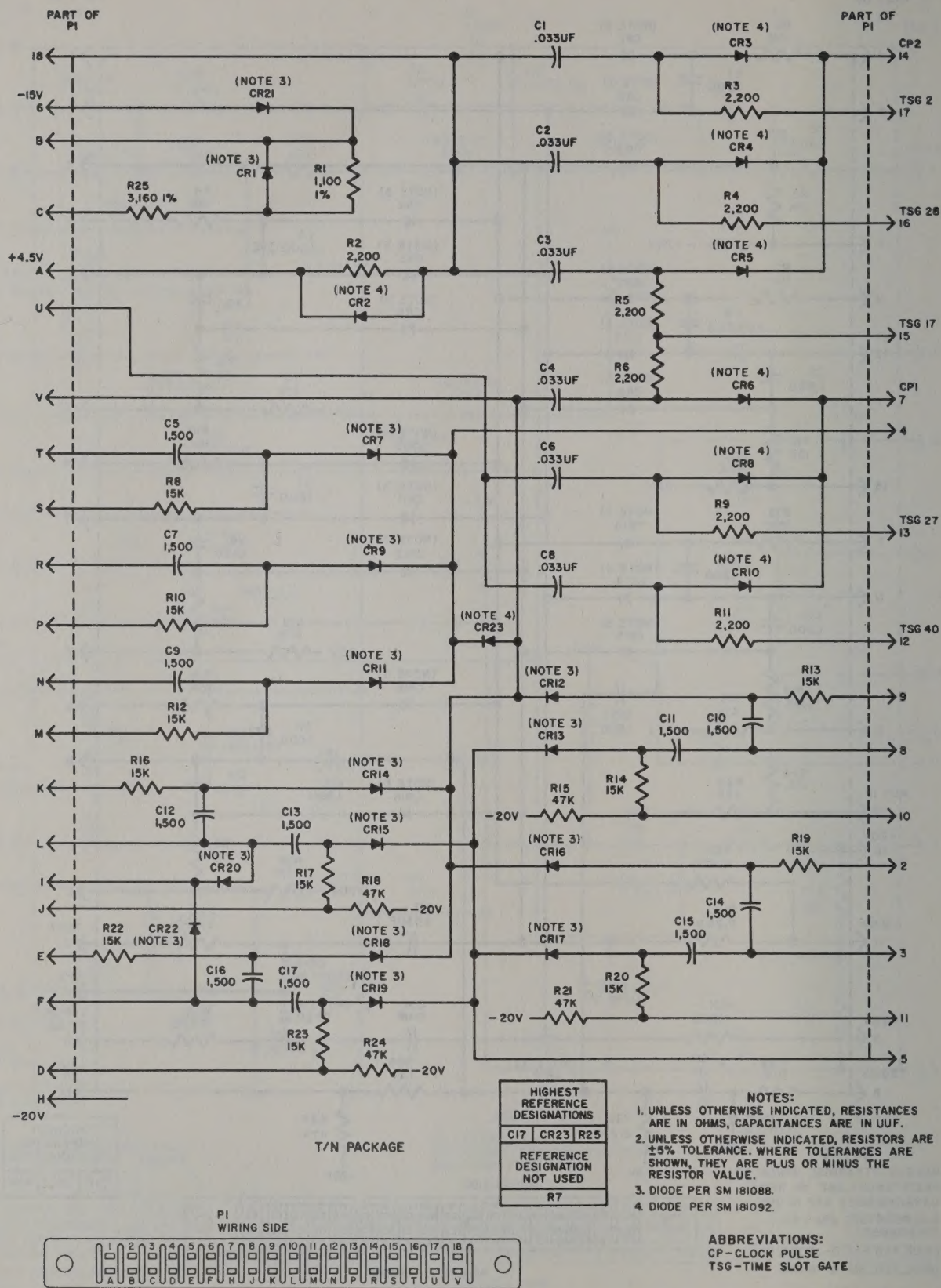
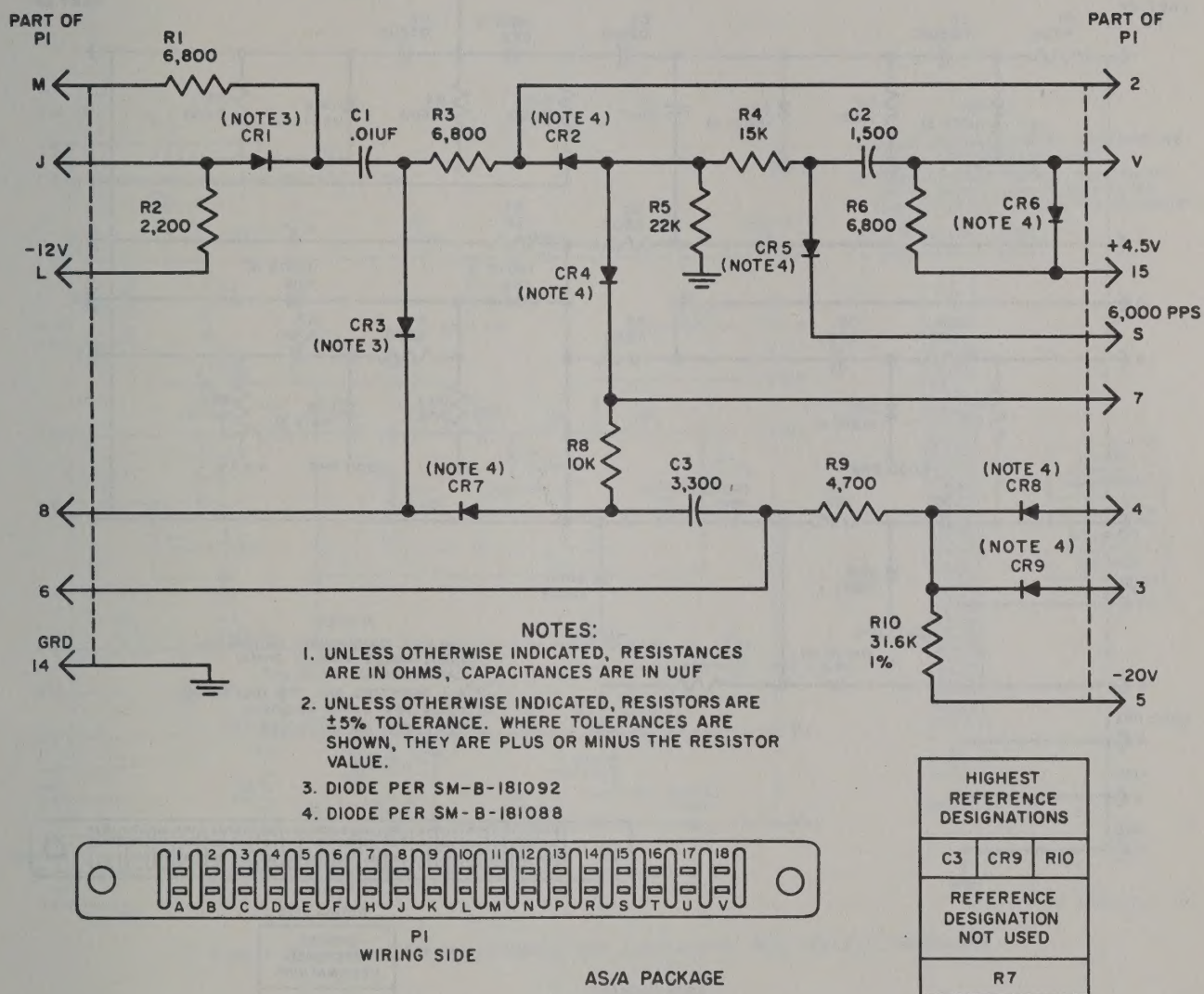


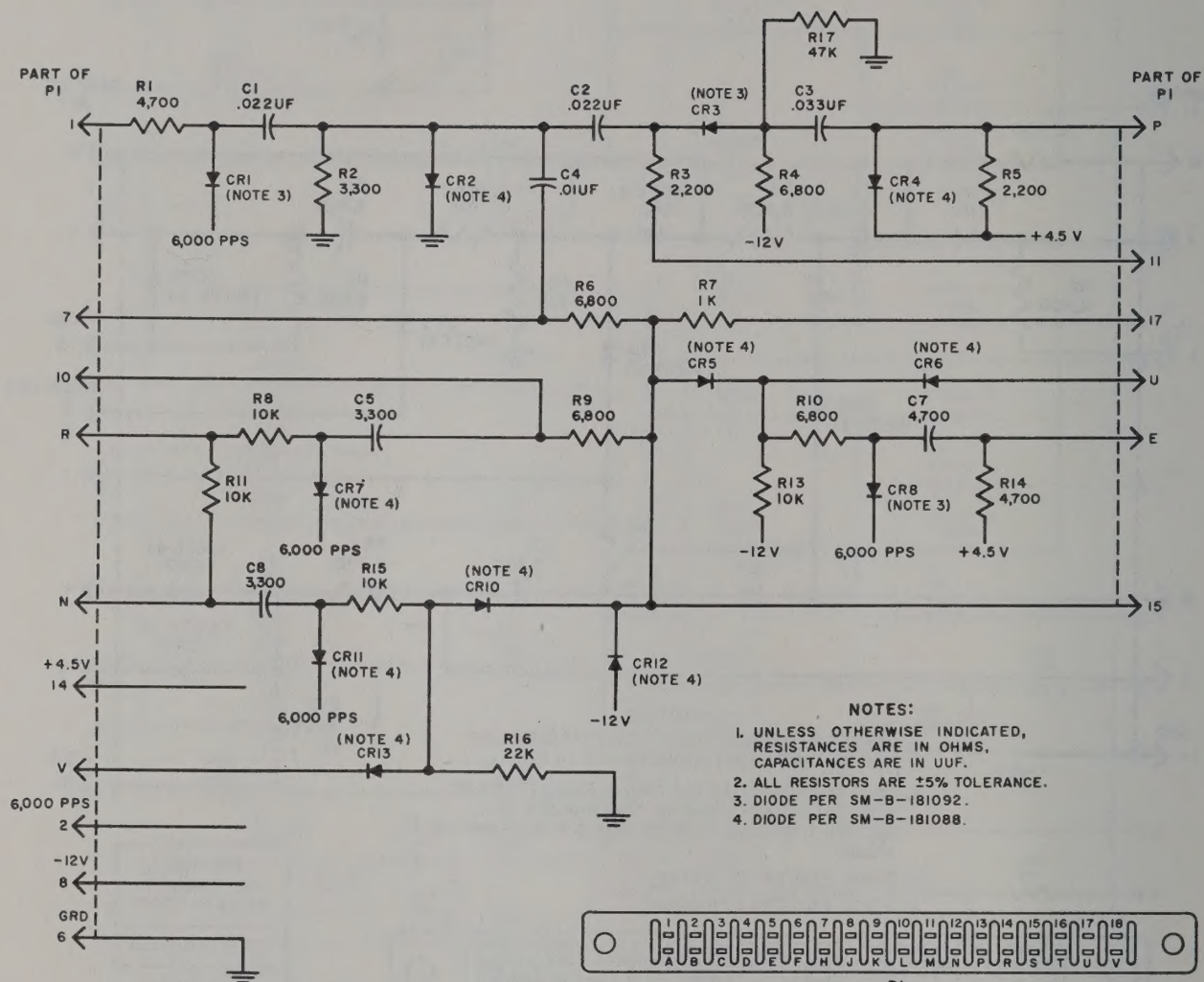
Figure 191. Transmitter unit subassembly MX-2344A/G, schematic.

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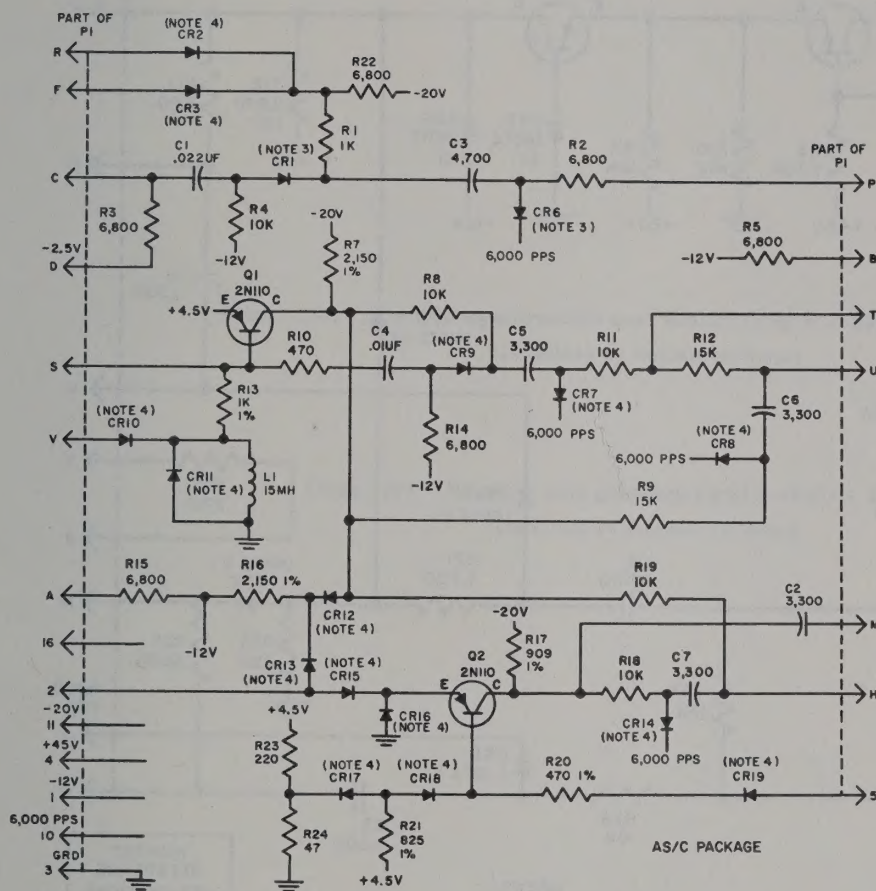
TM5840-219-35-176

Figure 192. Amplifier-synchronizer unit subassembly MX-2345A/G, schematic.

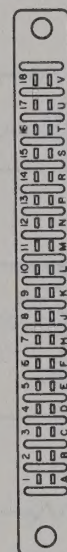


- NOTES:**
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
 2. ALL RESISTORS ARE $\pm 5\%$ TOLERANCE.
 3. DIODE PER SM-B-181092.
 4. DIODE PER SM-B-181088.

Figure 193. Amplifier-synchronizer unit subassembly MX-2346A/G, schematic.



- NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
 2. UNLESS OTHERWISE INDICATED, RESISTORS ARE $\pm 5\%$ TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.
 3. DIODE PER 5M-B-181092
 4. DIODE PER 5M-B-181088



P1
WIRING SIDE

HIGHEST REFERENCE DESIGNATIONS		
C7	CR19	R24
REFERENCE DESIGNATIONS NOT USED		
CR4, CR5, R6		

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Figure 194. Amplifier-synchronizer unit subassembly MX-2347A/G, schematic.

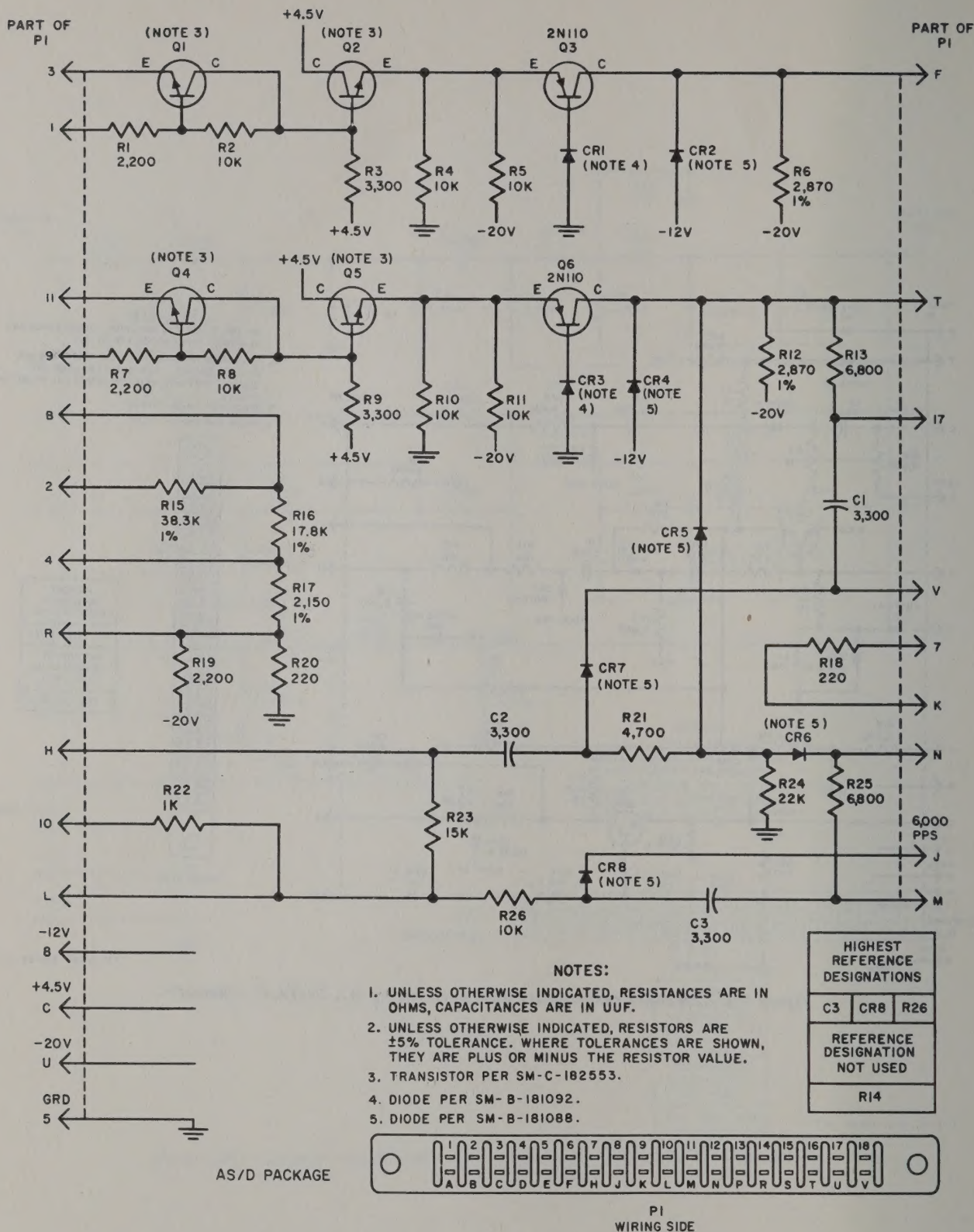


Figure 195. Amplifier-synchronizer unit subassembly MX-2348A/G, schematic.

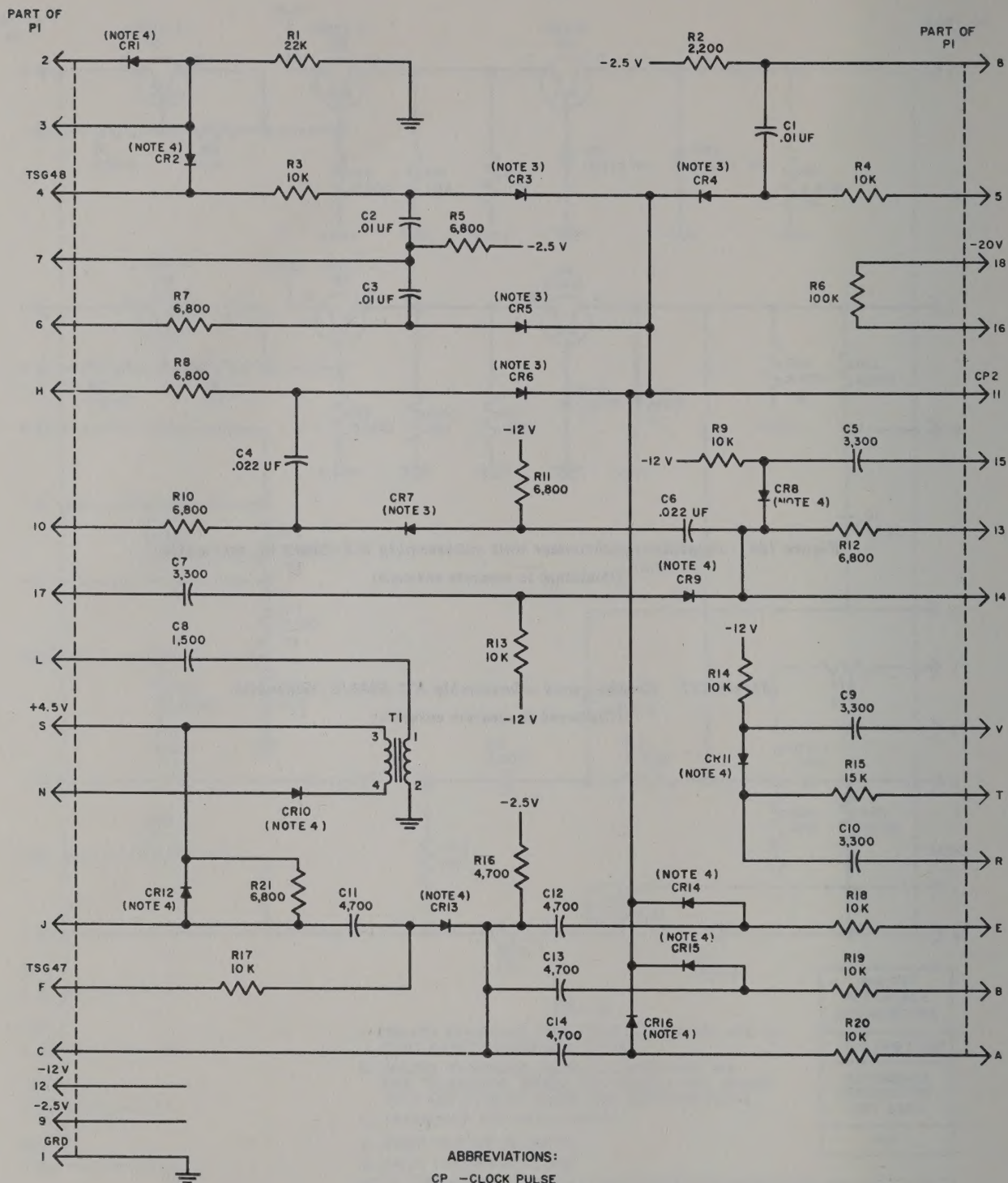
TM 5840-219-35-179

Figure 196. Amplifier-synchronizer unit subassembly MX-2349A/G, schematic.

(Contained in separate envelope)

Figure 197. Receiver unit subassembly MX-2685/G, schematic.

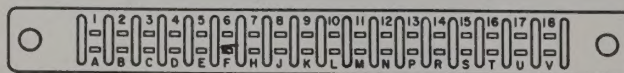
(Contained in separate envelope)



ABBREVIATIONS:
CP - CLOCK PULSE
TSG - TIME SLOT GATE

NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. ALL RESISTORS ARE $\pm 5\%$ TOLERANCE.
3. DIODE PER SM-B-181092
4. DIODE PER SM-B-181088



R/K PACKAGE

PI
WIRING SIDE

HIGHEST REFERENCE DESIGNATION		
C14	CR16	R21

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Figure 198. Receiver unit subassembly MX-2351A/G, schematic.

Figure 199. Receiver unit subassembly MX-2686/G, schematic.

(Contained in separate envelope)

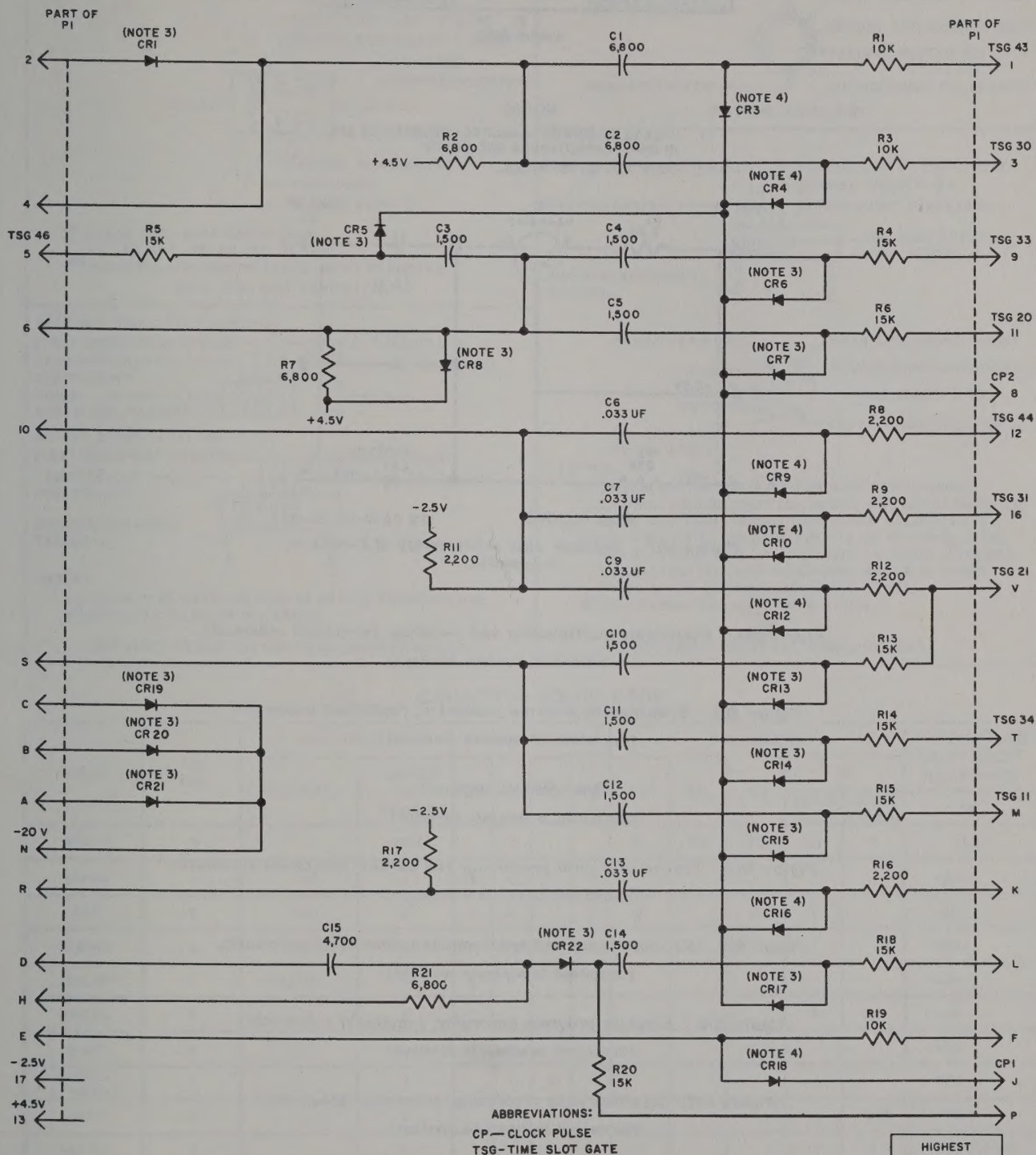
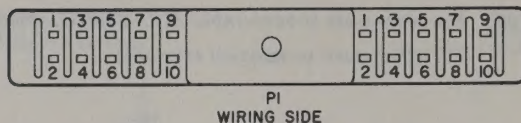


Figure 200. Receiver unit subassembly MX-2687/G, schematic.



NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. DIODE PER SM-B-181088.

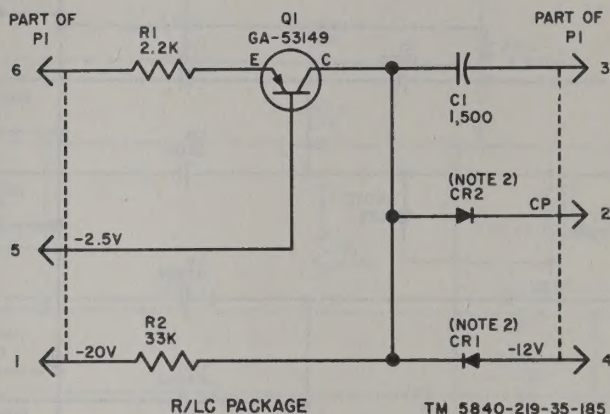


Figure 201. Receiver unit subassembly MX-2684/G, schematic.

Figure 202. Coordinate multiplexing and encoding, functional schematic.

(Contained in separate envelope)

Figure 203. Transmitter program generator, functional schematic.

(Contained in separate envelope)

Figure 203—Continued.

(Contained in separate envelope)

Figure 204. Transmitter data processing and output, functional schematic.

(Contained in separate envelope)

Figure 205. Receiver input and synchronizing, functional schematic.

(Contained in separate envelope)

Figure 206. Receiver program generator, functional schematic.

(Contained in separate envelope)

Figure 207. Receiver data processing, functional schematic.

(Contained in separate envelope)

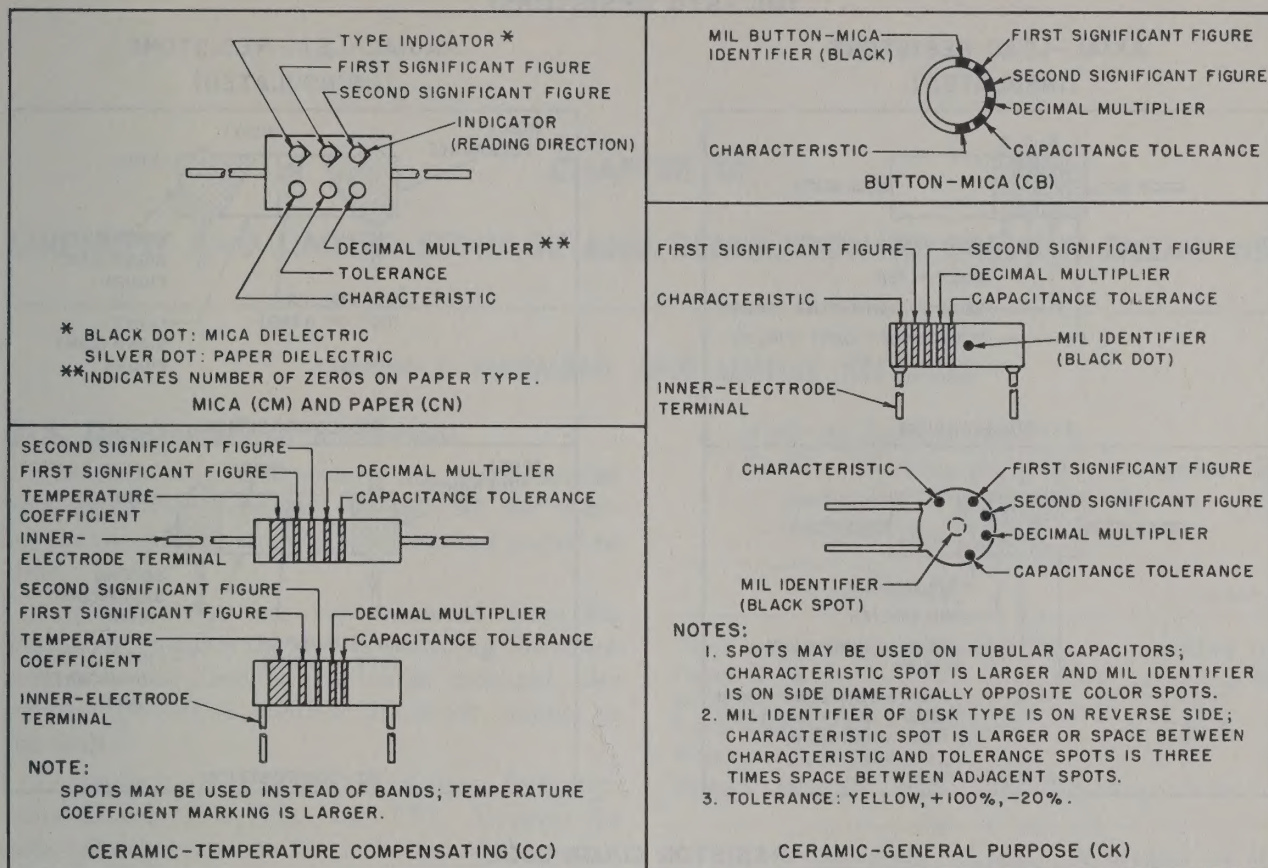
Figure 207—Continued.

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Figure 208. Power supply distribution, functional schematic.

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CAPACITOR COLOR CODE MARKING (MIL-STD CAPACITORS)



CAPACITOR COLOR CODE

COLOR	SIG FIG.	MULTIPLIER		CHARACTERISTIC ¹				TOLERANCE ²					TEMPERATURE COEFFICIENT (UUF/UF/°C)
		DECIMAL	NUMBER OF ZEROS	CM	CN	CB	CK	CM	CN	CB	CC		
											OVER 10UUF	10UUF OR LESS	
BLACK	0	1	NONE		A			20	20	20	20	2	ZERO
BROWN	1	10	1	B	E	B	W				1		-30
RED	2	100	2	C	H		X	2		2	2		-80
ORANGE	3	1,000	3	D	J	D			30				-150
YELLOW	4	10,000	4	E	P								-220
GREEN	5		5	F	R						5	0.5	-330
BLUE	6		6		S								-470
PURPLE (VIOLET)	7		7		T	W							-750
GRAY	8		8			X						0.25	+30
WHITE	9		9								10	1	-330(±500) ³
GOLD		0.1						5		5			+100
SILVER		0.01						10	10	10			

1. LETTERS ARE IN TYPE DESIGNATIONS GIVEN IN MIL-C SPECIFICATIONS.

2. IN PERCENT, EXCEPT IN UUF FOR CC-TYPE CAPACITORS OF 10 UUF OR LESS.

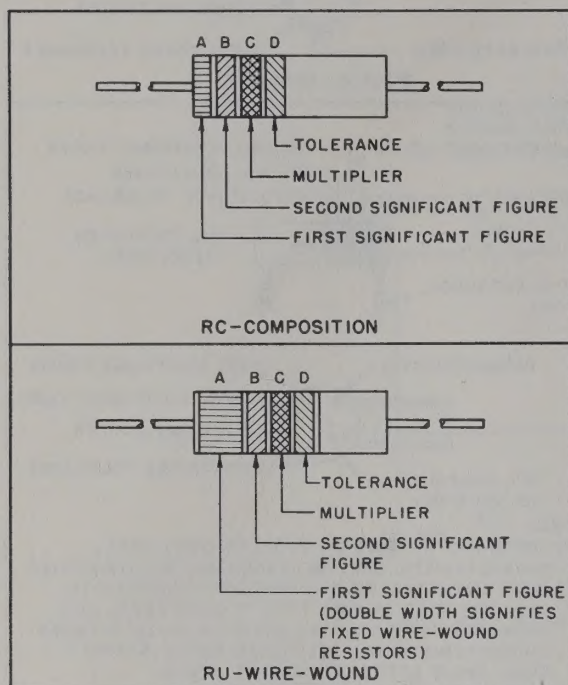
3. INTENDED FOR USE IN CIRCUITS NOT REQUIRING COMPENSATION.

STD-C1

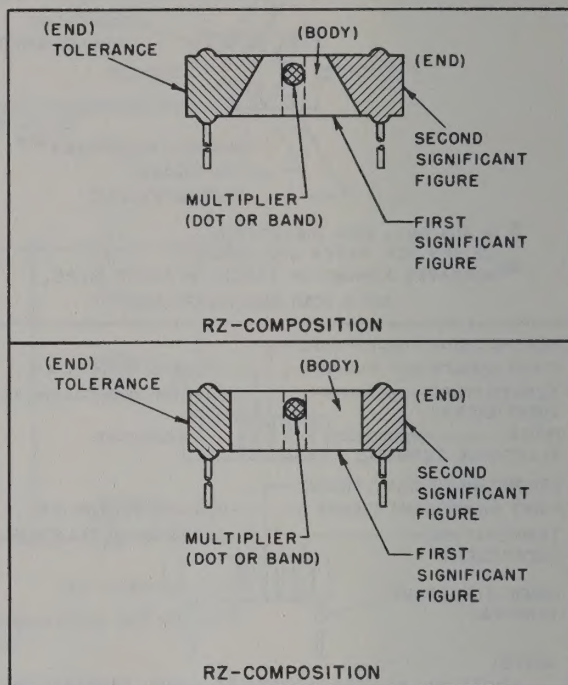
Figure 209. Standard capacitor color code.

RESISTOR COLOR CODE MARKING (MIL-STD RESISTORS)

AXIAL-LEAD RESISTORS (INSULATED)



RADIAL-LEAD RESISTORS (UNINSULATED)



RESISTOR COLOR CODE

BAND A OR BODY*		BAND B OR END*		BAND C OR DOT OR BAND*		BAND D OR END*	
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)
BLACK	0	BLACK	0	BLACK	1	BODY	± 20
BROWN	1	BROWN	1	BROWN	10	SILVER	± 10
RED	2	RED	2	RED	100	GOLD	± 5
ORANGE	3	ORANGE	3	ORANGE	1,000		
YELLOW	4	YELLOW	4	YELLOW	10,000		
GREEN	5	GREEN	5	GREEN	100,000		
BLUE	6	BLUE	6	BLUE	1,000,000		
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7				
GRAY	8	GRAY	8	GOLD	0.1		
WHITE	9	WHITE	9	SILVER	0.01		

* FOR WIRE-WOUND-TYPE RESISTORS, BAND A SHALL BE DOUBLE-WIDTH.
WHEN BODY COLOR IS THE SAME AS THE DOT (OR BAND) OR END COLOR,
THE COLORS ARE DIFFERENTIATED BY SHADE, GLOSS, OR OTHER MEANS.

EXAMPLES (BAND MARKING):

10 OHMS ± 20 PERCENT: BROWN BAND A; BLACK BAND B;
BLACK BAND C; NO BAND D.
4.7 OHMS ± 5 PERCENT: YELLOW BAND A; PURPLE BAND B;
GOLD BAND C; GOLD BAND D.

EXAMPLES (BODY MARKING):

10 OHMS ± 20 PERCENT: BROWN BODY; BLACK END; BLACK DOT
OR BAND; BODY COLOR ON TOLERANCE END.
3,000 OHMS ± 10 PERCENT: ORANGE BODY; BLACK END; RED DOT
OR BAND; SILVER END.

STD-R1

Figure 210. Standard resistor color code.

CHAPTER 10

SHIPMENT AND LIMITED STORAGE AND DEMOLITION TO PREVENT ENEMY USE

Section I. SHIPMENT AND LIMITED STORAGE

215. Disassembly of Equipment

The following instructions are recommended as a guide for preparing the data set for transportation and for storage for a limited period of time.

a. After power has been removed from the equipment, remove the screws fastening the shock mounts to the floor, and if trailer mounted, also remove the screws holding the shock mounts to the wall.

b. Remove all external connections from terminal boards TB1, TB2, and TB3. Remove the external connection to J1 at the top of the terminal board ladder.

c. Make sure the hold-downs for the packages are secure.

d. Check that all electron tubes are firmly in place.

e. Tighten the thumb nuts holding the rack in place.

216. Repacking for Shipment or Limited Storage

The exact procedure for repacking the equipment depends on the material available and the conditions under which the equipment is to be shipped or stored. Use the procedures outlined in *b* below whenever possible. If the original packing case was saved, it should be re-used. The information concerning the original packing (par. 12) will be helpful.

a. Material Requirements.

- (1) The following materials are required for packaging Coordinate Data Set AN/TSQ-36 (fig. 6):

Material	Quantity
Paper, corrugated, single face, flexible.....	60 sq. ft.
Paper, Grade A.....	60 sq. ft.
Strapping, flat steel $\frac{3}{4}$ ".....	34 ft.
Tape, water resistant, gummed.....	20 ft.
Wooden shipping crate.....	1.
Sponge rubber, $3\frac{3}{4}$ " x 1".....	11 ft.

- (2) Dimensions, volume, and weight of the packed crate are as follows:

Box size (in.) (inside)	Cubic feet	Packed weight (lb.)
72 x 24 x 16.....	11	500 (approx.).

b. Packaging (fig. 6).

- (1) Wrap the cabinet girth-wise with grade A paper and single face corrugated paper. Do not wrap over the handle or the shock mounts.
- (2) Place the wrapped cabinet, door side up, on the bottom side of the crate.
- (3) Nail the front and back sides, and the two ends to the bottom, and nail the sides and ends together.
- (4) Nail the top to the crate.
- (5) Apply the flat steel strapping length-wise as shown in figure 6.

Section II. DEMOLITION OF MATERIEL TO PREVENT ENEMY USE

217. General

The demolition procedure outlined in paragraph 218 will be used to prevent the enemy from using or salvaging this equipment. Demolition of the equipment will be accomplished only upon order of the commander.

218. Methods of Destruction

a. Smash. Smash the controls, tubes, transistors, relays, packages, switches, capacitors, transformers, and meter; use sledges, axes, handaxes, pickaxes, hammers, crowbars, or heavy tools.

b. Cut. Cut all connecting wires and cables; use axes, handaxes, or machetes.

c. Burn. Burn cords and technical manuals; use gasoline, kerosene, oil, flame throwers, or incendiary hand grenades.

d. Bend. Bend panels and cabinet.

e. Explode. If explosives are necessary, use firearms, grenades, or TNT.

f. Dispose. Bury or scatter the destroyed parts in slit trenches or fox holes, or throw them into streams.

APPENDIX I

BINARY NUMBERS—THEORY AND APPLICATION

1. Scope

This appendix is intended as a reference source to give enough information on the nature and use of binary numbers to explain how they are used in the transmission of information by the data set. It does not purport to be a textbook on binary arithmetic. For example, in this application, use is made of addition only; subtraction is avoided by the use of an operator, known as a complement, described in paragraph 6 through 8 below. No use is made of multiplication or division.

Note. The binary numbers in this discussion are written in conventional form, that is, with the least significant digit at the right; however, the binary numbers used to illustrate system operation in the theory and maintenance sections of this handbook are written as handled in the equipment, that is, with the least significant digit at the left.

2. Nature of Binary Numbers

a. In the common representation of numbers, successive digits stand for coefficients of successive powers of 10. In the binary system the coefficients are either ZERO's or ONE's and are coefficients of successive powers of 2. In both cases, the value of the number is given by the sum of the series of terms involved, as shown in the following examples:

Scale of 10 (decimal)	Scale of 2 (binary)
$1 \times 10^3 = 1000$	$1 \times 2^3 = 8$
$0 \times 10^2 = 0$	$0 \times 2^2 = 0$
$1 \times 10^1 = 10$	$1 \times 2^1 = 2$
$1 \times 10^0 = 1$	$1 \times 2^0 = 1$

Decimal value = 1011

Decimal value = 11

b. All numbers in the binary system consist of ZERO's and ONE's. For this reason the system is well adapted for use with telephone or

telegraph circuits where the ONE's are represented by signals and the ZERO's by no signals.

c. As indicated in the example above, each digit ONE indicates that the particular power of 2 appropriate to that digit position is to be included in the summation which gives the decimal number. Each digit ZERO indicates that the corresponding power of 2 is replaced by 0 in the summation.

d. ZERO's in the extreme left are not significant in themselves but may be required to complete a signal pattern where the same number of binary digits is sent for each number transmitted. They may also be needed in connection with parallax correction.

e. The following are samples of binary numbers corresponding to decimal numbers which are simple powers of 2:

Number in decimal system	Power	Binary number
1-----	2^0	1
2-----	2^1	10
4-----	2^2	100
8-----	2^3	1000
16-----	2^4	10000
32-----	2^5	100000
64-----	2^6	1000000

f. Intermediate numbers are obtained by addition. For example:

Decimal number	Binary number
$5 = 4 + 1$	101
$13 = 8 + 4 + 1$	1101
$22 = 16 + 4 + 2$	10110
$43 = 32 + 8 + 2 + 1$	101011

3. Determining a Binary Number From a Decimal Number

a. To determine a binary number from a decimal number, divide the number successively by 2, ignoring the remainder in the case of odd num-

bers, as illustrated in the left column of the following table:

<i>Successive division</i>	<i>Binary equivalent</i>
5326	0
2663	1
1331	1
665	1
332	0
166	0
83	1
41	1
20	0
10	0
5	1
2	0
1	1

b. When the division is complete, the binary equivalent of the whole number is obtained by starting at the top and writing, from right to left, a ONE for each odd number in the column and a ZERO for each even number, as shown in the right column of the table above. The top digit of the column is the least significant; the bottom, the most significant. The binary number derived from the example given above is written as follows:

most least
significant digit 1010011001110 significant digit

4. Determining a Decimal Number From a Binary Number

To determine a decimal number from a binary number, start with the least significant digit at the top. Express each binary number as powers of 2 and add. This is illustrated in the following table:

<i>Binary code</i>	<i>Power</i>	<i>Decimal number</i>
Least significant digit	0 × 2 ⁰ =	0
	1 × 2 ¹ =	2
	1 × 2 ² =	4
	1 × 2 ³ =	8
	0 × 2 ⁴ =	0
	0 × 2 ⁵ =	0
	1 × 2 ⁶ =	64
	1 × 2 ⁷ =	128
	0 × 2 ⁸ =	0
	0 × 2 ⁹ =	0
	1 × 2 ¹⁰ =	1024
	0 × 2 ¹¹ =	0
Most significant digit	1 × 2 ¹² =	4096
Decimal sum	=	5326

5. Addition of Binary Numbers

The following basic conventions give the rules for the addition of binary numbers:

0+0=0
1+0=1

0+1=1

1+1=0, with 1 to carry into the next place.

1+1+1=1, with 1 to carry into the next place.

The process is illustrated by an example (adding from right to left):

Add 0 00101 00110 01110
to 0 00111 01010 11000

Sum 0 01100 10001 00110

6. Subtraction of Binary Numbers

Direct subtraction of binary numbers is not used in this equipment. Instead, the required subtraction is carried out in the equipment by the process of complement addition. This method, as described below, involves only addition and finally the dropping of a surplus digit. This is done in order that the receiver, which requires subtraction in order to obtain parallax correction, may use a serial adder instead of a subtracting device. In order to subtract a binary number, B, from a binary number, A, use the following steps:

- Write the number, B, in binary form.
- Write its complement, obtained as described in paragraph 7 below, under it.
- Write the number, A, in binary form below this complement. (The order suggested is merely to make the next operation easier by keeping together the two lines to be added.)
- Add the complement of B to A.
- Drop the digit, 1, which appears at the extreme left of the sum. The remaining binary digits give the number which is the desired difference.

7. Determining the Complement

The process of determining the complement is as follows:

- Build out the binary number, B, by adding ZERO's at the left until it has the same number of digits as the binary number A.
- Note the first ONE, counting from the right. Bring down this ONE and all ZERO's to the right of it unchanged.
- Reverse all other digits (if ONE, change to ZERO; if ZERO, change to ONE), including any ZERO's added in step a.

8. Significance of the Complement

- To illustrate what the complement is and how it is used, an example is given first of a

complement in decimal numbers. The analogy then will be made with the complement given in binary numbers. The complement of any decimal number is the difference obtained when that number is subtracted from a larger number which is an integral power of 10, such as 100, 1000, etc. It may be seen from the example below that adding the complement of a number and then dropping the digit 1 on the extreme left gives the same result as subtracting the original number.

- (1) By direct subtraction 92 subtracted from 5326 is written as follows: $5326 - 92 = 5234$.
- (2) By the use of the complement 92 subtracted from 5326 is written as follows: $10,000 - 92 = 9908$ (the complement). Then this number is added to 5326: $9908 + 5326 = 15234$. Drop the digit 1 on the left and the answer is 5234.
- (3) The individual steps in the process are as follows:

Number	10's complement	Discard	Answer
5326	+ 10,000-92	- 10,000	= 5234

b. In the case of binary numbers, the operation of subtraction by the complement method is analogous to the example given above, except

that here the larger number which is selected to form the complement is a number which is an integral power of 2. In the binary number, this is represented by a digit ONE in the extreme left-hand position so that the final operation of dropping this digit is comparable to dropping the 1 in the decimal case. The significance of the operation is illustrated below both for the binary numbers and their corresponding decimal numbers:

	Decimal	Binary
Number B_	92	0000001011100
"2's" Complement of B (8192-92).	8100	1111110100100
Number A	5326	1010011001110
Add A to Comp B	13426	11010001110010
Discard the 8192	- 8192	(Drop the left-hand ONE)
Result	5234	1010001110010

Note that $8192 = 2^{13}$. In the decimal case using the "2's" complement, the last discarding operation is done by direct subtraction since the quantity to be discarded is no longer represented by a single digit, ONE, (as in the previous decimal example using the "10's" complement). In the binary case, it is discarded merely by dropping the left-hand 1.

APPENDIX II

BASIC CONTROL CIRCUIT ELEMENTS

1. General

This appendix describes the basic control and logic circuits used throughout the data set. A complete description of the system circuitry is given in chapters 7 and 8. This appendix is intended to illustrate the fundamental aspects of the control method so that the combinations of fundamental circuits described in those chapters will be more readily understood.

2. Transistor Circuits

The functions of the data set are performed largely by transistor circuits which act as switching elements. Basically there are two types of such switching elements employed, bistable and monostable circuits. The bistable circuit, sometimes called a flip-flop and designated F/F, is stable in either of two conditions, ON or OFF. The monostable circuit, sometimes called a flip-zero and designated F/O, is stable only in the OFF condition. In this equipment such circuits are point-contact transistor circuits working with a grounded emitter. They are controlled or triggered by application of a voltage to the base. The output is the collector. Some of these switching elements are shown schematically in figure 211, circuits C, D, and E. Compared to the data set speed of signaling, they are very fast in turning ON and somewhat slower in turning OFF. A negative-going trigger voltage of only a microsecond or so applied to the base is sufficient to turn the transistor ON. Turning it OFF requires a positive-going pulse of 5 to 15 microseconds also applied to the base circuit.

3. Clock Pulses and Time Slot Gates

a. A continuing series of negative-going voltage pulses is generated at the rate of 750 pps, the line signaling speed of the system, and these pulses are applied at the time desired under the control of transmission-type diode gates. These

gates are normally closed, presenting a high impedance to the continuously connected source of voltage pulses. During the intervals within the message frame that a turn-on pulse is desired, the gate is enabled. This is done by applying a suitable bias to the gate which changes its impedance to the pulse source to a low value and thus allows the pulse to pass. The negative-going pulses are called clock pulses, designated CP, and are generated by a clock pulse generator deriving its control from a frequency divider supplied, in turn, by a tuning-fork-controlled 1,500-cycle oscillator.

b. The gate-enabling intervals in the transmitter, for example, are derived from a transistor ring counter comprised of ten units ring stages and nine tens ring stages. Each clock pulse causes the ring counter to advance one step. When the ring counter starts, tens ring zero, TR 00, is ON and units ring zero, UR 0, is ON. Succeeding clock pulses trigger the units ring stages UR 1, UR 2, and so on, to UR 9. The next clock pulse triggers the second tens ring stage, TR 10, and UR 0. Each succeeding pulse advances the units ring and every tenth advances the tens ring. Thus, the time slots of the frame may be marked as desired by establishing coincidence of the ON condition of the units and tens rings stages. An AND gate is employed to establish coincidence. This type of logic circuit is illustrated in figure 211, illustrative circuit A. If tens ring stage M is ON and units ring stage N is ON, a potential of -2.5 volts with respect to ground will appear across resistor Ra and time slot M+N is marked. With only tens ring stage M ON and some units ring stage other than N ON, the voltage across Ra is about -12 volts.

c. Not all of the time slots of the frame are employed to enable the functions which must be activated to send a frame of information. Thus,

only those stages of the ring counter required are equipped with AND gates. The AND gate also is used to identify coincidence of events in other instances, such as that illustrated in figure 211, circuit F, which will be discussed later.

4. Gate Circuits

a. The basic element employed to utilize the time slot intervals for activating the transistor circuits is a transmission-type diode gate such as that shown in figure 211, circuit B. These are called time control gates, designated TCG. They are not so designated on the system drawings, however, for two principal reasons. The three elements of each TCG are sometimes included in the standard transistor packages and, in other instances, are elements of a package containing several circuits, not necessarily related in function. Once understood, however, their circuit configuration and their combination with other elements of the system are recognizable on the circuit schematic drawings.

b. With application of a square-wave enabling pulse to the input of the time control gate, the potential at the junction point of the resistor R_g , the capacitor C_g , and the diode CR starts rising from -12 volts to -2.5 volts at the charging rate of C_g in series with R_a and R_g . The time constant of this circuit is chosen so that $(R_a + R_g) C_g$ is small with respect to 1.33 milliseconds, the length of one time slot of the frame, and still not so short that the trigger point of the transistor (fig. 211, circuit C) sees an appreciable change in its normal bias voltage of $+4.5$ volts. Because the continuously-generated clock pulses control the advance of the ring counter, they always occur near the end of the time slot interval marking the ON coincidence of two ring stages. At this time C_g is charged to -2.5 volts. The clock pulse source normally rests at the -2.5 volts applied to the diode CR of the time control gate. The clock pulse itself is a steep negative-going pulse which drops the diode from a potential of -2.5 volts to about -11 volts for about one microsecond. This discharges capacitor C_g very rapidly and because of the impedance of the one-millihenry inductance in the base of the transistor, the base potential of the transistor is lowered to about -4.5 volts. Under these conditions, the bistable flip-flop circuit (fig. 211, illustrative circuit C, for example) changes to the ON state. As mentioned earlier, a positive-

going pulse is required to turn the transistor OFF, and it must be longer in duration than the negative-going clock pulse needed to turn it ON. Monostable F/O transistor circuits of the general configuration illustrated in figure 211, illustrative circuit E, are used to generate these turn-off pulses, called set zero pulses and designated SZ. In general, two types of set zero pulses are used in the system, one of 15 to 45 microseconds duration and about 14 volts amplitude, the other of more than 22 microseconds duration and 2.5 volts amplitude. The larger amplitude pulse is suitable for turning off a single transistor. The low-voltage, low-impedance longer pulse is needed to turn off a number of transistor circuits at the same time. With this exception the functional employment of the two types of pulses is the same. It will be noted in chapters 7 and 8 that there are instances in which a clock pulse and a set zero pulse are gated into a transistor circuit simultaneously. Because the set zero pulse has a much longer duration, it negates and overrides the clock pulse, and the transistor is turned OFF.

c. The foregoing is intended to illustrate the basic data control elements of the system. These elements are as follows: the bistable transistor flip-flops, F/F, which perform the system switching functions; the clock pulses, CP, which activate the transistors to the ON state and trigger the monostable transistor flip-zero's, F/O, to generate the set zero pulses, SZ, to turn OFF the switching transistors; the AND, or coincidence, gates which provide the enabling-bias voltages for the time control gates, TCG, which admit the transistor-activating pulses at the required interval. Familiarity with this basic scheme of control should simplify understanding the functioning of the system and assist in recognizing combinations of these control elements as they are applied throughout the system. Some of these combinations are illustrated in the other lettered sections of figure 211.

d. One example of the use of two transmission-type diode gates in series is illustrated in figure 211, circuit D. Here the gate circuit configuration is employed as a data read-in gate. The read-in gate shown is controlled by the time control gate. This is the basic arrangement used

Figure 211. Basic drive and control elements, illustrative circuits.

(Contained in separate envelope)

to transfer the data received on the binary counters of the transmitter digital section to the shift registers, a shift register stage being the transistor circuit shown in figure 211, circuit D. If a ONE is stored in the associated binary counter, an enabling bias is applied to the data lead shown. The clock pulse applied through the time control gate turns ON this data lead and those other shift register flip-flops whose read-in gates are enabled with data bias from their associated binary counters.

e. Figure 211, circuits F, G, and H, illustrates combinations of time control and AND gates to effect control under a combination of desired conditions.

f. Figure 211, circuit F, shows an arrangement of an AND gate and a time control gate to provide an activating clock pulse when, and only when, two selected circuit elements are in the ON condition.

g. Figure 211, circuit G, shows a configuration affording an activating clock pulse when one of two elements is ON and the other OFF. Note particularly the interconnection of these two basically similar gates. The gate labeled +TCG is the now familiar time control gate. The one labeled TCG- is actually the same thing but its diode is connected to receive the output of

the positive gate and its resistance arm, which has been the input heretofore, is connected to -12 volts. The capacitor remains as the output element. The negative or OFF input is applied to the junction of the two gates. The F/F shown as the OFF element, with which coincidence with an ON element is desired, applies -12 volts to the negative input to the combination gate when the F/F is OFF. Under this condition, both sides of the diode of TCG- are at the same potential and the pulse emanating from +TCG, when its input is enabled by an ON pulse, results in the pulse being passed to the output of TCG-. This combination gate, designated CG on the block diagrams, is used in a number of different instances in the system. Familiarity with the configuration should make it recognizable on the system circuit schematic drawings and should assist materially in understanding the functioning of the associated circuit.

h. Still another example of multiple employment of time control gates is illustrated in figure 211, circuit H, where the control logic is OR. In this case a clock pulse is desired for application to the F/O at time slots 34 or 47 if SR 11 or 12 or 13 are ON. This is the configuration employed for off-scale detection in the receiver digital section.

APPENDIX III

TRANSISTORS

1. Definition

A transistor is a semiconductor device having three or more terminals. In this device the resistance between two electrodes is controlled by the carrier density from a third electrode.

2. The Atom

a. The atom, consisting of a nucleus surrounded by a number of electrons, is electrically neutral. The nucleus possesses a positive charge of several units. Each electron has a charge of minus 1 unit. Associated with the nucleus are a sufficient number of electrons to render the atom neutral.

b. It is possible to convert the atom into an entity called an ion. To do so, the number of electrons associated with the nucleus is either increased or decreased. Adding electrons has the effect of creating a negative ion; subtracting electrons has the effect of creating a positive ion (fig. 212, part A).

3. The Crystal

In a crystal the atoms arrange themselves in a regular pattern, which is called the lattice (fig. 212, part B). The lattice site is the prescribed place in the geometry of the crystal occupied by the atom. The atom is held in its lattice site by a covalent bond of certain electrons of an atom and corresponding electrons of its neighboring atoms. The covalent bond is the interaction between the various electrons in the lattice site.

4. The Electrons

a. The valence electrons account for only a part of the total number of electrons surrounding the nucleus. The others may be called owned electrons, and they lie closer to the nucleus than do the valence electrons. It is possible to remove a few of the atom's electrons, both valence and owned, from their assigned roles by giving them sufficient energy. Upon acquiring sufficient en-

ergy, electrons may become a special type of electron called conduction electrons. These conduction electrons separate themselves from the others and take a position farther away from the nucleus than the valence electrons.

b. In figure 212, part C, the electrons are shown in rings about the nucleus, separated from the nucleus in accordance with their relative energies. Those with the highest energy are farthest from the nucleus. Definite energy gaps exist in materials between the energy band typical of the valence electrons and the energy band typical of the conduction electrons. Also, only those electrons which are present in the conduction band are subject to migration when a potential is applied to the material. This migration is a flow of electric current.

c. In a conducting material the gap between the valence energy band and the conduction energy band is very small (or zero); consequently, the conduction band is readily occupied. Conduction in materials such as copper and aluminum results from this small energy gap. On the other hand, the energy gap found in an insulator is very large. Materials with this energy gap of intermediate size are called semiconductors. Although in a semiconductor the conduction band is not normally occupied, it is possible for electrons to occupy it by imparting energy to them in the form of heat, light, or electricity. With a typical semiconductor, such as germanium, the conduction at room temperature is small, and the material has a high resistance. Increasing the temperature imparts energy to the electrons, raising them to the conduction band, and decreases the resistance of the material. This characteristic of a semiconductor is called intrinsic semiconductivity.

5. Addition of Impurities

The intrinsic semiconductivity can be increased and controlled by the addition of a small amount

of impurity into the material. For purposes of illustration, presume that the crystal lattice of germanium is constructed as shown in figure 212, part B, that the nucleus is given a charge of plus four units, and that each atom has four electrons, giving it a neutral charge. An atom of arsenic, which is added to this structure, is depicted as having a nucleus charge of five units, complemented by five electrons. When an arsenic atom is inserted as a substitute for the center germanium atom in figure 212, part D, four of the five electrons are used to complete the covalent bond which typifies germanium, and the fifth electron is left relatively free. The arsenic atom then becomes an ion with one positive charge, but since there is one free electron, the net charge of the material is neutral.

6. N-Type Germanium

a. In addition to having opposite charges, the ions are distinguished from the electrons in that the ion is an immobile charge fixed in the lattice geometry, while the electron is a mobile particle. The type of germanium in which an excess of free electrons has been deliberately created is given the name N-type germanium. The name donor is given to that class of materials which is capable of providing free electrons if it is inserted as an impurity. The addition of the impurity is called doping.

b. Similar to the doping of pure germanium with the donor material is the process of inserting an atom of a material having a nucleus charge of plus three units complemented by three electrons. Such a material is indium (fig. 212, part E).

7. Holes

The three electrons which the indium brings to the lattice are not sufficient to complete the typical covalent bond, and a fourth electron must be taken from some place else in the lattice. Such an electron deficiency resulting from the introduction of the indium atom is called a hole and is treated as a positive particle. The hole is said to migrate to the position vacated by the filling electron. The indium atom produces a negative ion and a positive hole in a manner similar to the production of a positive ion and a free electron by arsenic. The name acceptor is given to that class of materials which is capable of providing holes when it is inserted as an impurity.

8. P-Type Germanium

Being equal in numbers, the negative ion and positive hole do not alter the uncharged condition of the germanium sample. Again, the ion is fixed, and the hole is mobile. Materials such as indium are termed acceptors, and the type of germanium produced by acceptor doping is termed P-type.

9. Hole and Electron Flow

a. The density of the free electrons and holes is controlled by controlling the number of foreign, or impure, atoms added to the germanium. Intrinsic conduction in a semiconductor takes place because the number of electrons and holes is equal. Upon the application of a battery, the holes migrating in one direction add their charge-carrying capacity directly to that of electrons migrating in the opposite direction, developing a net current flow. The property of transistor action occurs because it is possible to create selectively an excess either of holes or electrons and to control, by polarity, the flow of charge carriers of one type or the other. Electrons outnumber holes in N-type germanium; therefore, in N-type germanium electrons are called majority carriers and holes are called minority carriers. By contrast, the P-type germanium holes outnumber electrons so the holes are called majority carriers and the electrons are called minority carriers.

b. Such distinction is not possible with intrinsic semiconductivity, since holes and electrons appear in equal numbers. Thus intrinsic or heat-induced semiconductivity is undesirable in impurity semiconductivity, because at higher temperatures the ability to control the character of the conductivity is lost.

10. Junctions

PN junction is the name given to a block of germanium containing both a P and an N region separated by an interface, or plane. Figure 212, part F, illustrates that in the N region neutrality results from an equality of the positive ions and the negative electrons, and in the P region it results from an equal number of negative ions and holes. Thus, the originally neutral germanium has not acquired any net charge as a result of the addition of either donor or acceptor atoms. In understanding transistor action it is convenient to regard the ion charges as being masters in a master-slave relationship, where the mobile

charges, electrons or holes, are slaves. In the master-slave concept, holes in the P region looking across the boundary or junction into the N region are confronted with an array of positive ions which repel them and force them to remain in the P region. Similarly the electrons in the N region are repelled by the negative ions in the P region, forcing the electrons to remain in the N region. This concept is equivalent to what would be obtained by collecting all of the ion centers in each region and representing them by a total fixed charge. In the P region this net charge would be negative, and in the N region it would be positive. The potential hill shown in figure 212, part G, is a graphic representation showing the separation of the P and N regions.

11. Potential Hills

a. Majority carriers confronted by the potential hill are prevented from passing into the adjacent region. Only those very few majority carriers which happen to have absorbed additional energies are free to cross the boundary and become minority carriers. The potential hill can be regarded as both a barrier to the migration of majority carriers, and as an invitation to the minority carriers to return to the region in which they were initially confined. This potential hill can be modified by the application of certain potentials external to the transistor.

b. If an external battery is connected as shown in figure 212, part H, so that its polarity aids the internal polarity, the prohibition against the migration of majority carriers is reinforced. Graphically speaking, the potential hill has been raised. Conversely, the potential hill may be lowered by the application of an external bias in opposition to the internal polarity. The effect of a lowered potential hill is evidenced by increased current flow under the influence of the same magnitude of applied potential.

12. Battery Functions

a. The battery serves both a static and dynamic function. Its static function is the modification of the potential hill. Its dynamic function is the injection or withdrawal of mobile carriers from the germanium. Decreasing the magnitude of the potential hill (forward bias) requires that the positive side of a battery be connected to the P region and the negative side of the battery to the N region. The positive pole of the battery

attracts electrons, and attracting electrons from the P region is identically equal to an injection of holes.

b. There is a prescribed number of holes or electrons which can coexist with the ions in the crystal lattice if a neutral balance is to be maintained. The injection of a hole into the P region by the application of a battery bias temporarily disturbs this balance, and will, a short time later, be compensated by a hole being forced across the boundary into the N region. The boundary hill over which the hole is traveling has been lowered by the application of the external bias. The hole in the N region can then be collected by the negative side of the battery (fig. 212, part J).

13. Junction Transistor

a. Both junction type and point contact transistors are used throughout the data set. The type of transistor shown in figure 212, part L, is called a junction transistor and is discussed here first. The point contact transistor discussion follows.

b. The three regions of the transistor shown in the figure are called emitter, base, and collector. At each junction is a hill which may be raised or lowered by the application of external potentials.

c. It is the purpose in a transistor circuit to introduce current (mobile carriers) into the emitter, and to extract as many of these mobile carriers as possible from the collector. Travel of the carriers consists of two phases. The first phase concerns a hole leaving the emitter and entering the base. To start the carrier on its way, forward bias is applied between the emitter and base electrodes, reducing the magnitude of the emitter-to-base hill. This permits many holes to enter the N region where they become minority carriers. For the second phase, a large potential hill (back bias) presents both a large barrier to majority carriers and a strong attraction to minority carriers. Back biasing the base-to-collector junction offers the holes the option of returning to the emitter or continuing on to the collector. Sliding down the large potential hill is more attractive to these minority carriers than returning to the emitter. Thus, for the most part, holes continue on from the base to the collector.

14. Common Base Connection

The process of all the carriers injected into the emitter being collected at the collector is ideally

100 percent efficient; however, certain mechanisms occur in the base and give rise to the base current which may be measured in the base electrode (fig. 212, part K). In practice, 95 to 99 percent of the current introduced in the emitter may be obtained at the collector. The remaining one to five percent appears as base current. The ratio of the collector current to the emitter current is given the designation alpha (α), and, in a junction transistor, is never greater than one. It should be noted that forward bias of the emitter-to-base junction creates a characteristically low impedance emitter circuit, while the back biased collector-to-base junction creates a characteristically high impedance collector circuit.

15. Voltage Gain

a. Voltage gain of the transistor occurs because of the nearly equal current flow in the emitter circuit and the collector circuit, and the much higher impedance of the collector circuit. A low drive voltage is required to inject a certain amount of current into a low impedance circuit. The same amount of current emerges, with negligible loss, at the collector circuit and is extracted in a high impedance circuit. The ratio between the high collector voltage and the low emitter voltage is the voltage gain of the transistor. Since the current is about the same, the ratio will be about the same as the ratio of the collector impedance to the emitter impedance.

b. In the circuit shown in figure 212, part M, the dc bias determines the static current flow in the emitter-to-base and collector-to-base circuits, and the transformer applies the varying voltage which determined the instantaneous dynamic current flow. A relatively low voltage is needed to pass a given current into the emitter circuit, while the collector circuit, being back biased, has a relatively high resistance for a load. Since the current in both circuits is about the same, the output voltage is higher than the input, resulting in a voltage gain.

16. Common Emitter

With ammeters in both the emitter-to-base and the collector-to-emitter, it can be seen that there is a change in the collector current about 20 times greater than the change in the base current (fig. 212, part N). As was seen in figure 212, part K, the base current amounts to about five units of the total number of 100 units, thus,

modulating the base circuit results in a current gain of nearly 20 times at the collector. The voltage gain of the grounded emitter is a combination of current gain and the output-to-input impedance ratio.

17. Point Contact Transistors

a. A single block of germanium, whether N-type or P-type, tends to have a charge that makes a thin surface layer act like a P-type semiconductor. When the emitter wire, shown in figure 212, part P, is made positive with respect to the base, current flows in the emitter circuit. Within the semiconductor, this current consists of the flow of positive holes which originate in the P-type surface layer under the emitter contact. If this contact is located sufficiently close to the collector contact, the positive holes are attracted by the electric field of the negatively charged collector, and most of them go to the collector and are there discharged. This action causes an increment of current flow in the collector circuit. As a result, the magnitude of the collector current may be controlled by controlling the emitter current.

b. It was stated earlier that the ratio of the collector current to emitter current of the junction transistor is less than unity. In the case of the point-contact transistor, however, this ratio may be two or three. This is explained with the aid of figure 212, part P. The collector current may be regarded as the algebraic sum of three individual components. First, there is the reverse leakage current which flows even in the absence of emitter current and is like that of a rectifier reverse current. Because electrons have a negative charge, the electric current they carry is opposite to the direction of their flow. Second, there is the current of positive holes being collected. Third, there is an additional electron current component originating at the collector contact and resulting from the act of hole collection. As the positive holes approach the collector, they attract additional electrons from the collector, many of which do not recombine, but which find their way to the base. It is this third current component, represented in figure 212, part P, by the flow labeled induced electron current, which is responsible for the current amplification. In a typical point contact transistor, the induced current may be about twice as large as the hole current which causes it. As a result, the

total current increment appearing in the collector circuit may be about three times as large as the emitter current.

18. Junction and Point Contact Transistors

In the ordinary junction transistor, the changes in the current *out* of the collector are slightly less than the changes in the current *into* the emitter. A junction transistor can be connected in ways that make it an amplifier of currents, but the amplified currents are in such a direction that only negative feedback can be obtained with simple circuits. On the other hand, the point contact transistor with its inherent current gain greater than unity is capable of positive feedback, making it particularly well suited for use in oscillator and switching circuits. One point contact transistor can be used in switching circuits where two junction transistors would ordinarily be required. For this reason, and because of its rapid rise time in pulse application, the point contact transistor is used extensively in the data set. Circuit symbols for the two types of transistors are shown in figure 212, part R.

19. Flip-Flop and Flip-Zero Operation

a. When point contact transistors are operated with large signals, such as the pulses used in the data set, they have nonlinear characteristics which make them useful as flip-flop and flip-zero circuits. In a circuit such as shown in part A of figure 213 the variation of base current with base voltage is similar to that depicted in part B. The curve shows three regions which, for purposes of this discussion, are called the OFF, TRANSITION, and ON regions. The OFF region is a positive resistance region and is stable; the transistor is at cut off. The TRANSITION region is a negative resistance region and is unstable; the transistor amplifies. When operated in this region, a transient or noise voltage may be enough to cause a sudden shift to either the ON or OFF region. The ON region is stable, and it too is a positive resistance region; the transistor is at saturation.

b. Within the ON and OFF regions the circuit behaves as a normal stable circuit about the established operating point. An input signal at the base may displace the operating point out of one stable region, through the unstable region, and into the other stable region.

c. A typical flip-zero circuit is shown in part C of figure 213. The characteristic curve ABCD and load line EF is shown in part D of figure 213. The operating point is established at point P in the OFF region by the +4.5 volts applied at the base through L1. The circuit remains in this condition unless an external voltage is applied to change the condition. This is done here by the application of a negative clock pulse at point X of part C of the figure during the application of an enabling gate voltage at point Y. The positive-going enabling pulse biases diode CR1 to the conducting condition, allowing the negative clock pulse to pass through it and through capacitor C1 to the base. The negative pulse causes the operating point P to fall past B and enter the TRANSITION region. The base current tends to increase rapidly due to the feedback from the collector. A large negative pulse is then developed across the coil which opposes this change in current and the operating point jumps to P1. The sudden increase of collector current through resistor R2 drops the collector from -12 volts to -2.5 volts. The voltage across the coil decays exponentially and the operating point moves from P1 to C. At this time the base current suddenly tries to decrease and the voltage across the coil reverses to oppose this increase. This positive voltage across the coil cuts off the collector current and the collector voltage therefore returns the -12 volts. The output is a positive-going pulse as indicated.

d. Part E of figure 213 is a typical flip-flop circuit. The circuits of parts C and E of this figure are similar except for the addition of resistor R3 and diode CR2. Normally the circuit is in the OFF condition at approximately point P, which is determined by the external loads and the +4.5-volt bias at the base (part F of fig. 213). Upon application of a negative clock pulse and positive gate voltage to the base, the base voltage is driven negative in the same manner as in part C of figure 213. The operating point P moves to B, jumps to E, and falls back to stable operating point P1 in the ON region where it is held by the voltage drop across R3. Since in the OFF condition R3 has a small voltage drop across it, it has only a small effect on the operating point, but when the circuit is driven far into the ON region, the drop across R3 (negative at the base

end) is large enough to overcome the +4.5-volt bias and to establish the new operating point at P1, where it remains until further action is taken.

e. The circuit is reset by the application of a positive set zero pulse at the base through isolation diode CR2. This positive pulse drives the operating point P1 past C into the TRANSITION region and, because of the reduced current through R3 and the resulting reduced voltage drop across it, the operating point jumps to F and then reverts to its original operating point established by the +4.5-volt bias.

f. In the OFF condition the collector is at about -12 volts, and in the ON condition the collector is at about -2.5 volts. The output voltage,

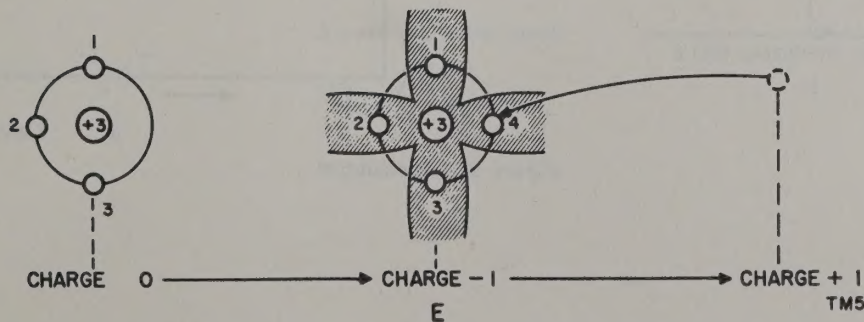
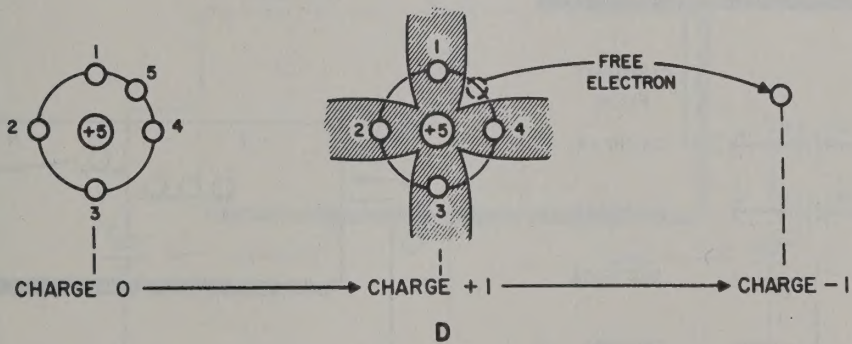
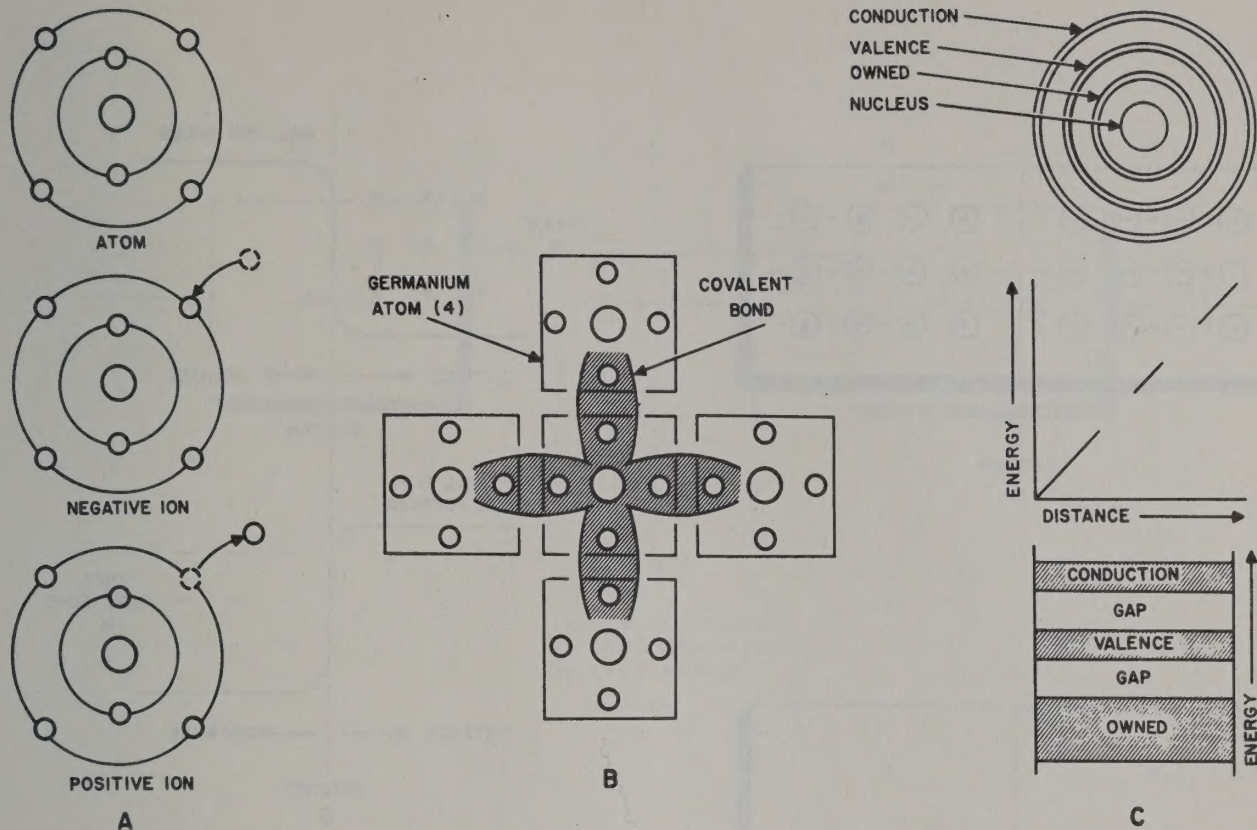
between the application of the clock pulse and the set zero pulse, is a rectangular wave, positive-going with an amplitude of about 9.5 volts.

20. Transistor Parameters

It is possible to connect the transistor with its base grounded, its emitter grounded, or its collector grounded. Each type of connection has its own general parameters which are listed in table I. In general, the grounded base connection is equivalent to the grounded grid connection for an electron tube, and the grounded emitter and grounded collector are equivalent to the grounded cathode and grounded plate, respectively, of the electron tube.

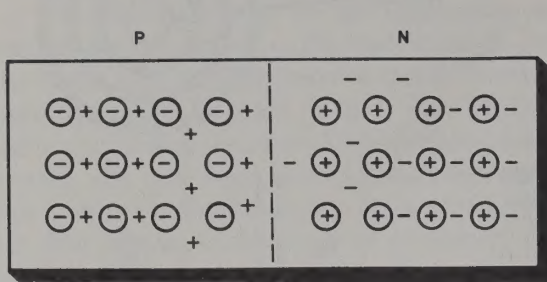
Table VIII. Transistor parameters (typical values)

Parameters	Grounded base	Grounded emitter	Grounded collector
Input impedance-----	100 ohms (low)-----	300-1,500 ohms (moderately low).	High (varies with output impedance).
Output impedance----	100K to 500K (high)-----	3,500-5,000 ohms (moderately low).	Moderate.
Power gain-----	18-25 db (moderate)-----	30-40 db (high)-----	Moderate.
Stability-----	Good-----	Moderate-----	Poor.
Phase reversal-----	No-----	Yes-----	No.
Applications-----	Lowest input impedance-----	Highest power gain-----	Impedance matching.

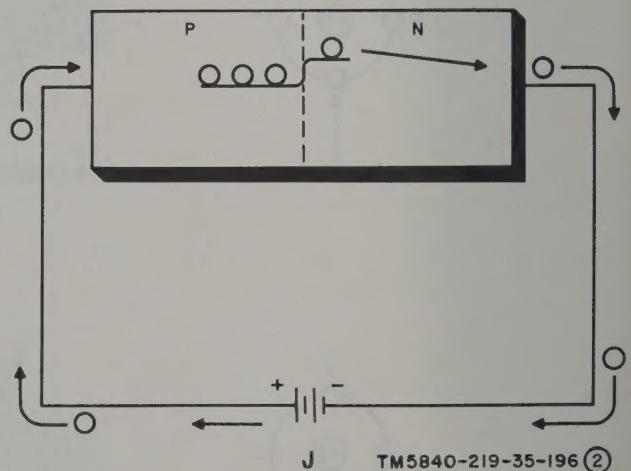
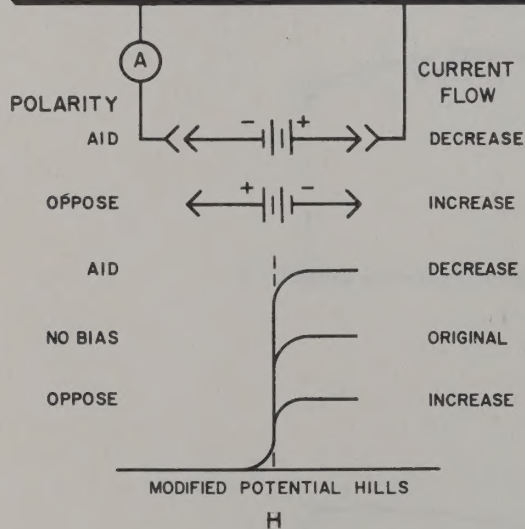
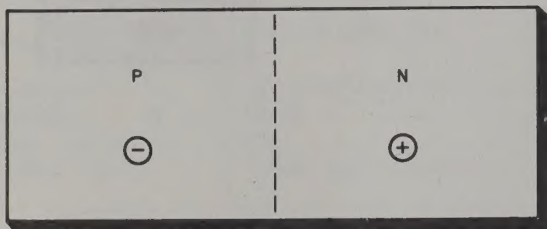
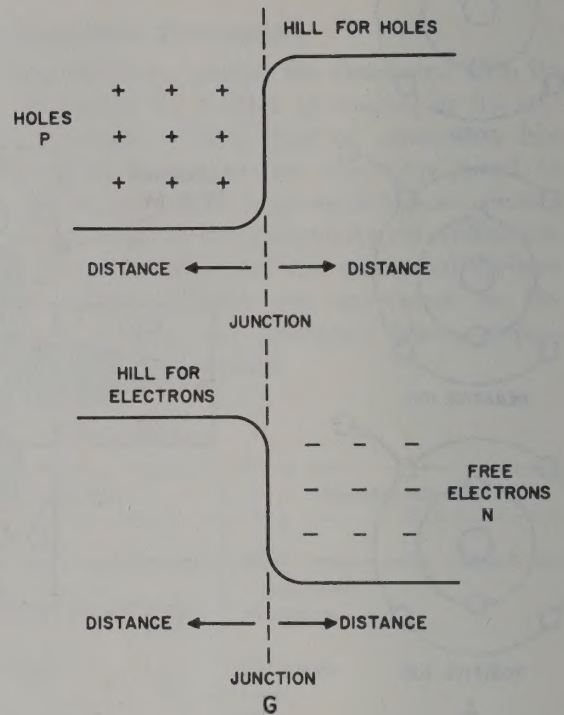


TM5840-219-35-196 (1)

Figure 212. Transistor development, illustrations.

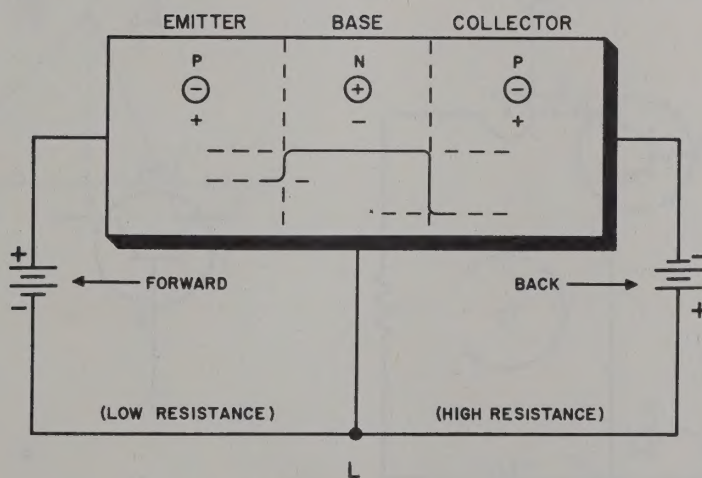
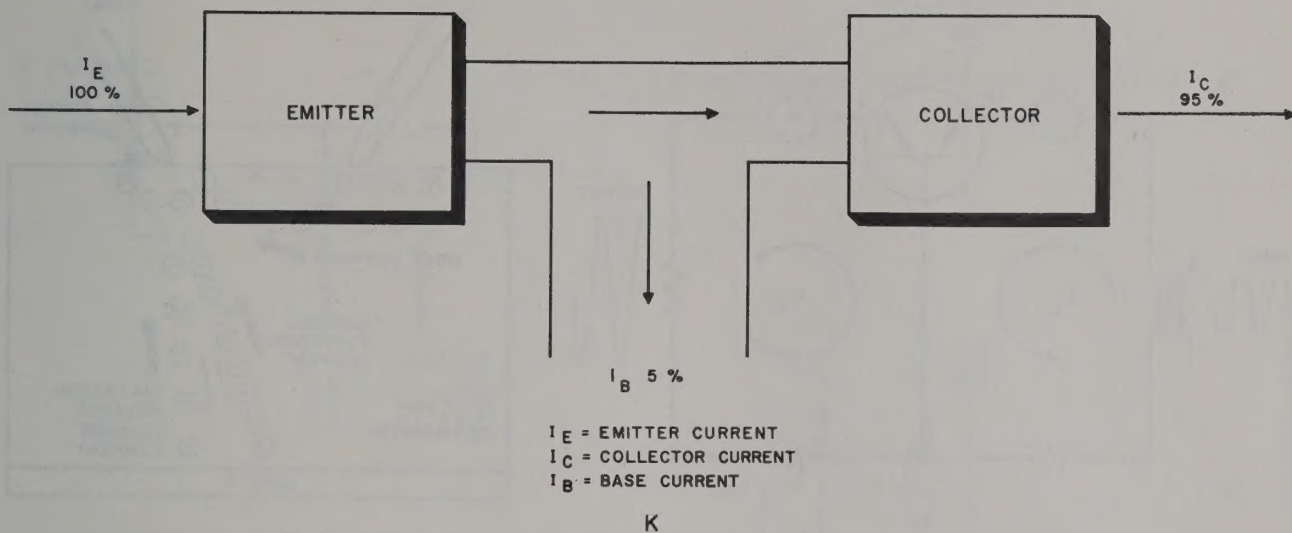


JUNCTION
F



J TM5840-219-35-196 ②

Figure 212—Continued.



TM5840-219-35-196 ③

Figure 212—Continued.

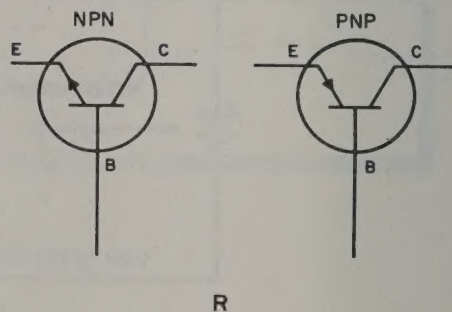
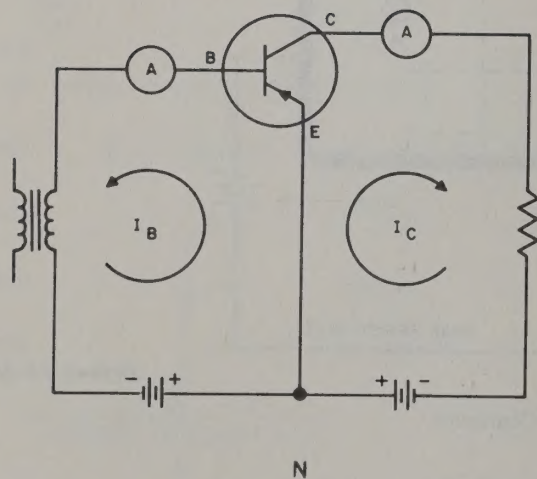
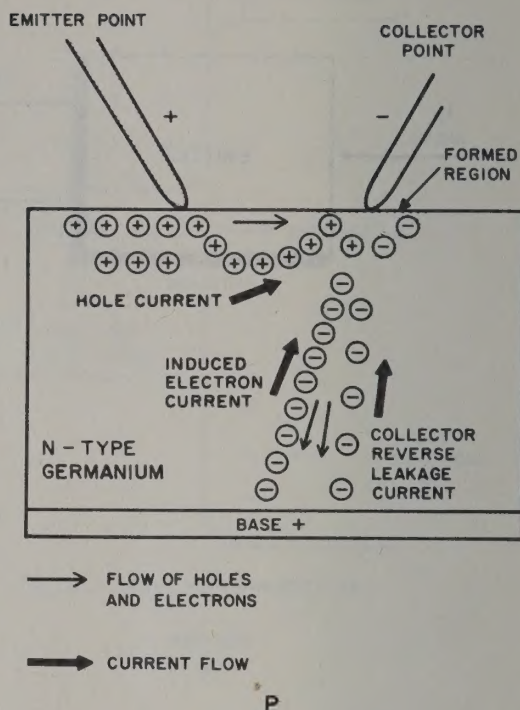
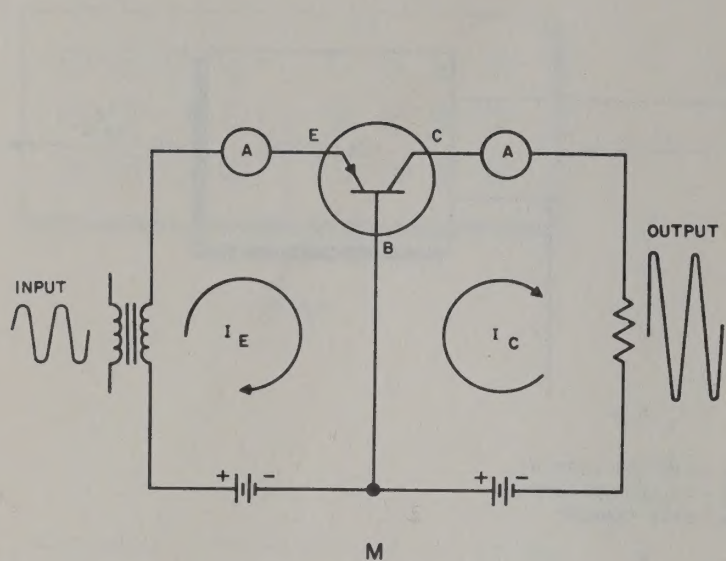


Figure 212—Continued.

TM 5840-219-35-196 (4)

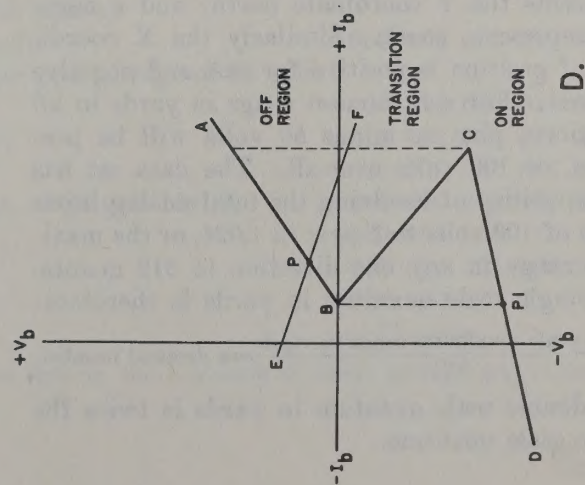
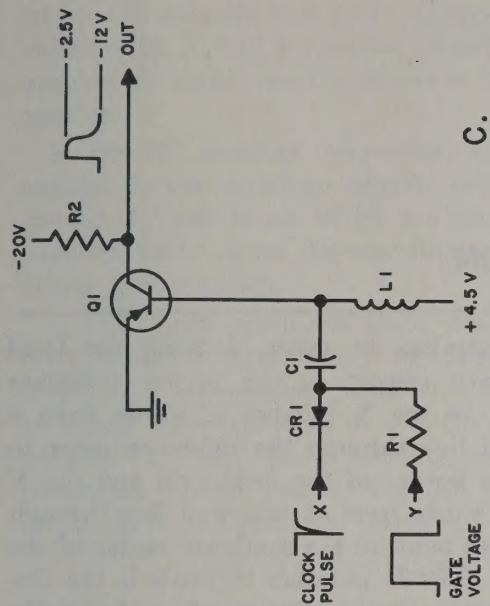
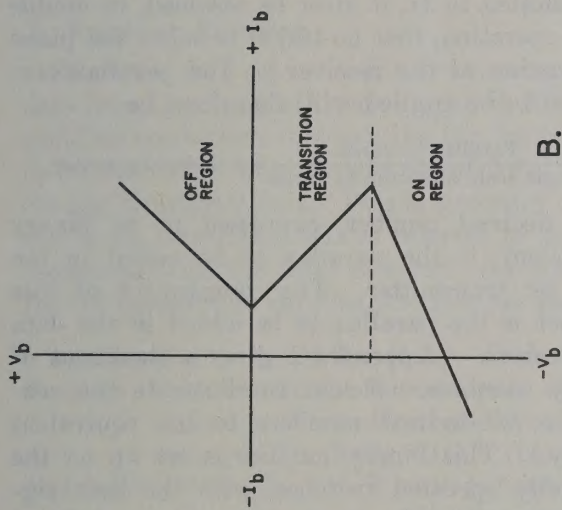


Figure 213. Point contact transistor circuits, simplified schematic.

APPENDIX IV

PARALLAX CORRECTION

1. General

a. Parallax corrections are applied in the transmitter and in the receiver, or receivers, with which it communicates in order to permit all target positional data to be interpreted in relation to a master reference point. It is therefore a fixed number which is changed only when the station location or the master reference point is changed or when the station shifts between single scale and double scale operation. Ordinarily, the commanding officer specifies the master reference coordinates and the coordinates of the location, but the operating personnel should understand the relationship of location and reference point coordinates and the binary number which is manually set into the data set equipment on the parallax switches.

b. Certain assumptions can be made to illustrate this relationship. Ranges are ordinarily given in yards. Computer devices associated with radar installations which may be served by the data set will present positional coordinates as positive or negative values of dc analog voltage. The data set is arranged to accept either ± 50 volts or ± 100 volts. Assuming, for example, that the ± 50 -volt range is in use, a positive voltage represents the Y coordinate north; and a negative represents south. Similarly the X coordinate of position is positive for east and negative for west. For a maximum range in yards in all directions, plus or minus 50 volts will be presented, or 100 volts over-all. The data set has the capability of resolving the total analog input range of 100 volts to 1 part in 1,024, or the maximum range in any one direction to 512 quanta. The single scale quantum in yards is therefore:

$$\frac{\text{Single scale maximum range in yards}}{512} = \text{a decimal number.}$$

The double scale quantum in yards is twice the single scale quantum.

c. The parallax in yards, defining the local position with respect to the master reference point, will be the X number of yards from a north-south line through the reference point to the western border of the local grid and the Y number of yards from an east-west line through the reference point to the southern border of the local grid. The H parallax in yards is the distance between a point 1,024 single scale quanta below sea level and a point 512 quanta below the local plane of location. (Because only 10 digits are allotted to H, it must be assumed, in double scale operation, that no target is below the plane of location of the receiver.) The parallax correction to be applied will, therefore, be

$$\frac{\text{Parallax in yards}}{\text{Single scale quantum in yards}} = \text{a decimal number.}$$

This decimal number, expressed in its binary equivalent, is the parallax to be added in the data set transmitter. The complement of this number is the parallax to be added in the data set receiver. (Appendix I gives a treatment of binary numbers sufficient to illustrate the conversion of decimal numbers to the equivalent binary.) This binary number is set up on the manually operated switches, with the least significant digit set in on the left and the digit of the largest significance on the right.

2. Transmitter Parallax

a. When the data set is used to transmit coordinate data which is referred to the origin of a larger master grid, relatively large values of parallax-correction data are added to the transmitted data. P_H , P_X , and P_Y parallax switches (on the coordinate data transmitter group panel) provide for adding his parallax correction in binary form. The digital earth curvature correction is added algebraically to the X and Y parallax before the parallax is set in. The parallax

corrections are based upon the over-all system, of which the data set is a part. Consequently, the values of H, X, and Y parallax (which are stereographic distances) must originate at higher headquarters.

b. The H parallax correction, expressed in quanta, is converted to binary form (see appendix I) and is set in by the use of the P_H parallax switches on the coordinate data transmitter group panel.

c. The digital earth curvature correction (par. 39d) is added algebraically to both the X and Y parallax corrections. Each sum is converted to binary form and is set in with the appropriate parallax switches. As an example, an X parallax correction of 200 quanta is added to a digital earth curvature parallax correction of -4:

$$200 - 4 = 196 \text{ quanta}$$

This value, converted to binary form, yields the X parallax-correction word 001 000 110 000 0 (appendix I).

3. Receiver Parallax

When the data set is used to receive coordinate data from the origin of a master grid, H, X, and Y parallax corrections representing the transmitter-to-receiver offset must be subtracted from the incoming coordinate data. This is necessary so that the target coordinate data is referred to the grid associated with the local receiver. As described for the transmitter parallax, the receiver parallax

must be converted to binary form (no digital earth curvature correction is added). However, subtraction of parallax is accomplished by addition of the binary parallax complement (appendix I). As an example, X parallax correction of 300 quanta yields the binary word:

001 101 001 000 0

The binary complement of this word is:

000 000 000 000 01
subtract 001 101 001 000 0

001 010 110 111

11 complement (disregard 1 in fourteenth place).

4. Typical Examples of Computing Parallax Correction Quantities

Six examples of computation for the parallax are given below. Three are for computing the Y coordinate: single scale to single scale, single scale to double scale, and double to double scale. Three are for computing the parallax for the H coordinate: single scale to single scale, double scale to single scale, and single scale to double scale. The computation for the X coordinate is performed in the same manner as for the Y coordinate. By the use of these examples, the parallax can be computed, once the geographical positions of the grids have been determined. In all cases, the reference between grids is the west and south junction (origin) of the X and Y coordinates of each grid.

a. Example No. 1—Y Coordinate, Single Scale (SS) to Single Scale.

Problem: To transmit the Y coordinate of a target from a transmitter operating in single scale and located at the center of grid No. 1 to a receiver operating in single scale at the center of single scale grid No. 2 (fig. 215). (Least significant digit appears at the left.)

At SS XMTR No. 1: (a) Y analog input = -25 volts (by inspection of fig. 215)

(Encoder output = 256 pulses)

(b) Digital equivalent of volts = 000 000 001 000 0

(c) Y parallax (P_{Y_1}) (master grid to edge of SS grid No. 1) = 000 000 000 011 0

(d) Output line code (b+c) = 000 000 001 011 0

At SS RCVR No. 2: (e) Line code input = 000 000 001 011 0

(f) P_{Y_2} (master grid to edge of SS grid No. 2) = 000 000 000 101 0

(g) Complement of (f) = 000 000 000 110 1

(h) Sum of (e) and (g) = 000 000 001 100 0 (1)*

(j) DLU contents = 000 000 001 1

(k) Analog output voltage = +25 volts

*The digit in parentheses is not actually present in the receiver, but is a result of binary addition and is shown for illustration.

b. Example No. 2—Y Coordinate, Single Scale (SS) to Double Scale (DS).

Problem: To transmit the Y coordinate of a target from a transmitter operating in single scale at the center of grid No. 1 (fig. 215) to a receiver operating in double scale at the center of grid No. 2 (fig. 215). (Least significant digit appears at the left.)

At SS XMTR No. 1:		(a) Y analog input = -25 volts	
		(Encoder output = 256 pulses)	
		(b) Digital equivalent of -25 volts	= 000 000 001 000 0
		(c) Y parallax (P_{Y1}) (master grid to edge of SS grid No. 1)	= 000 000 000 011 0
		(d) Output line code (b+c)	= 000 000 001 011 0
At DS RCVR No. 2:		(e) Line code input	= 000 000 001 011 0
		(f) Line code shifted one TS (due to programming)	= (0) 000 000 010 110 0*
		(g) P_{Y2} (master grid to DS No. 2 in DS size quanta)	= 000 000 000 010 0
		(h) Complement of (g)	= 000 000 000 011 1
		(j) Sum of (f) and (h)	= 000 000 010 100 0 (1)*
		(k) DLU contents	= 000 000 010 1
		(l) Analog output voltage	= +12.5 volts

*The digit in parentheses is not actually present in the receiver, but is the theoretical result of the operation and is shown for illustration.

c. Example No. 3—Y Coordinate, Double Scale (DS) to Single Scale (SS).

Problem: To transmit the Y coordinate of a target from a transmitter operating in double scale at center of grid No. 2 to a receiver operating in single scale at the center of grid No. 1 (fig. 215). (Least significant digit appears at the left.)

At DS XMTR No. 2:		(a) Y analog input = +12.5 volts	
		(Encoder output = 640 pulses)	
		(b) Digital equivalent of +12.5 volts	= 000 000 010 100 0
		(c) Binary counter output to shift registers	= 000 000 001 010 0 (0)*
		(d) Y parallax (P_{Y1}) (master grid to DS No. 2 in SS size quanta)	= 000 000 000 001 0
		(e) Output line code (c+d)	= 000 000 001 011 0
At SS RCVR No. 1:		(f) Input line code	= 000 000 001 011 0
		(g) P_{Y1} (master grid to edge of SS grid No. 1)	= 000 000 000 011 0
		(h) Complement of (g)	= 000 000 000 010 1
		(j) Sum of (f) and (h)	= 000 000 001 000 0 (1)*
		(k) DLU contents	= 000 000 001 0
		(l) Analog output voltage	= -25 volts

*The digits in parentheses are not actually present, but are shown for illustration. The off scale detection light will not go OFF because sampling is done only in the 11th, 12th, and 13th digits.

d. Example No. 4—H Coordinate, Single Scale (SS) to Single Scale.

Problem: To transmit the H coordinate of a target from a transmitter operating in single scale at center of grid No. 1 to a receiver operating single scale at grid No. 2 (fig. 214). (Least significant digit appears at the left.)

At SS XMTR No. 1:		(a) H analog input = +37.5 volts	
		(Encoder output = 896 pulses)	
		(b) Digital equivalent of +37.5 volts	= 000 000 011 1
		(c) H parallax (P_{H1}) (master grid to bottom of SS grid No. 1)	= 000 000 000 1
		(d) Output line code (b+c)	= 000 000 011 0 (1)*

*The digit in parentheses is dropped out in the shift register, so it is not present on the output line code.

At SS RCVR No. 2:	(e) Line code input	=000 000 011 0
	(f) P_{H_2} (master grid to bottom of SS grid No. 2)	=000 000 010 1
	(g) Complement of (f)	=000 000 011 0
	(h) Sum of (e) and (g)	=000 000 001 1
	(j) Analog output voltage	=+25 volts

e. Example No. 5—H Coordinate, Double Scale (DS) to Single Scale (SS).

Problem: To transmit the H coordinate of a target from a transmitter operating in double scale at center of grid No. 1 to a receiver in single scale at grid No. 2 (fig. 214). (Least significant digit appears at the left.)

At DS XMTR No. 1:	(a) H analog input =+18.75 volts (Encoder output =384 pulses)	
	(b) Binary counter output to shift registers	=000 000 011 0 (1)*
	(c) H parallax (P_{H1}) (master grid to DS grid No. 1, SS granularity)	=000 000 000 0**
	(d) Output line code (b + c)	=000 000 011 0
At SS RCVR No. 2:	(e) P_{H2} (master grid to bottom of SS grid No. 2)	=000 000 010 1
	(f) Complement of (e)	=000 000 011 0
	(g) Sum of (d) and (f)	=000 000 001 1 (0)***
	(h) DLU contents	=000 000 001 1
	(i) Analog output voltage	=+25 volts

*Shifted for DS operation by starting count in BC 2 instead of BC 1: thus line code contains count with SS granularity. The 1 in parentheses is not transferred to line code.

**All zeros because the master grid was selected with its H reference at the bottom of the DS grid.

***Digits in parentheses do not appear in the receiver, but are shown for illustration.

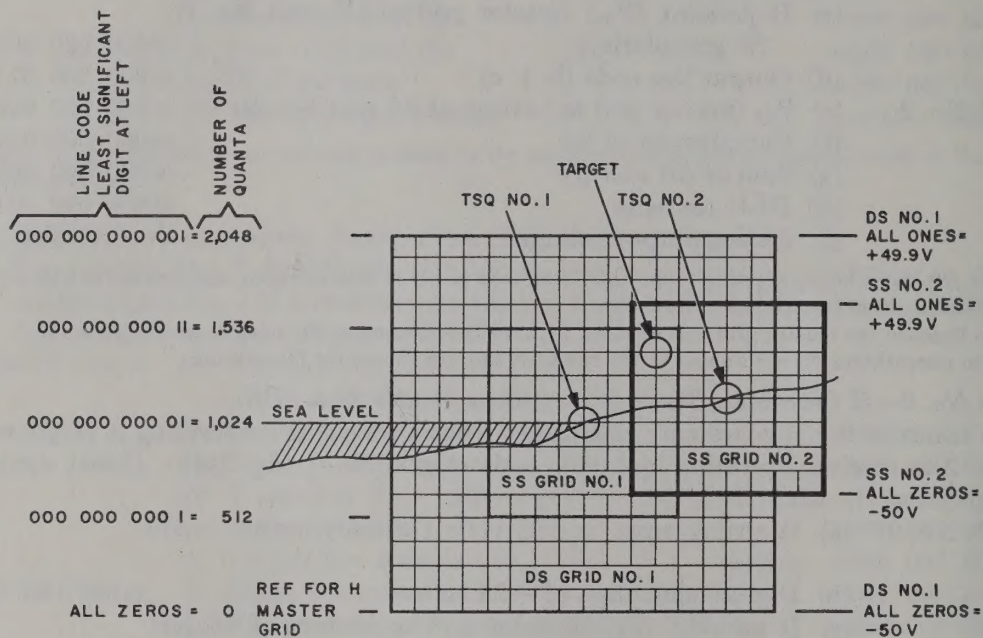
f. Example No. 6—H Coordinate Single Scale (SS) to Double Scale (DS).

Problem: To transmit the H coordinate of a target from a transmitter operating in single scale at grid No. 2 to receiver operating in double scale at grid No. 1 (fig. 214). (Least significant digit appears at the left.)

At SS XMTR No. 2:	(a) H analog input =+25 volts (Encoder output =512 pulses)	
	(b) Digital equivalent of +25 volts	=000 000 001 1
	(c) H parallax (P_{H1}) (master grid to bottom of SS grid No. 2)	=000 000 010 1
	(d) Output line code (b + c)	=000 000 011 0 (1)
At DS RCVR No. 1:	(e) Input line code shifted (due to change in programming for DS operation)	=(0) 000 000 110 0*
	(f) P_{H2} (master grid to DS grid No. 1 in DS quanta)	=000 000 000 0**
	(g) Complement of (f)	=000 000 000 0
	(h) Sum of (e) + (g)	=000 000 110 0
	(j) 1 inserted in DLU No. 10 (in DS only)	=000 000 000 1
	(k) Total contents of DLU's	=000 000 110 1
	(l) Analog output voltage	=+18.75 volts

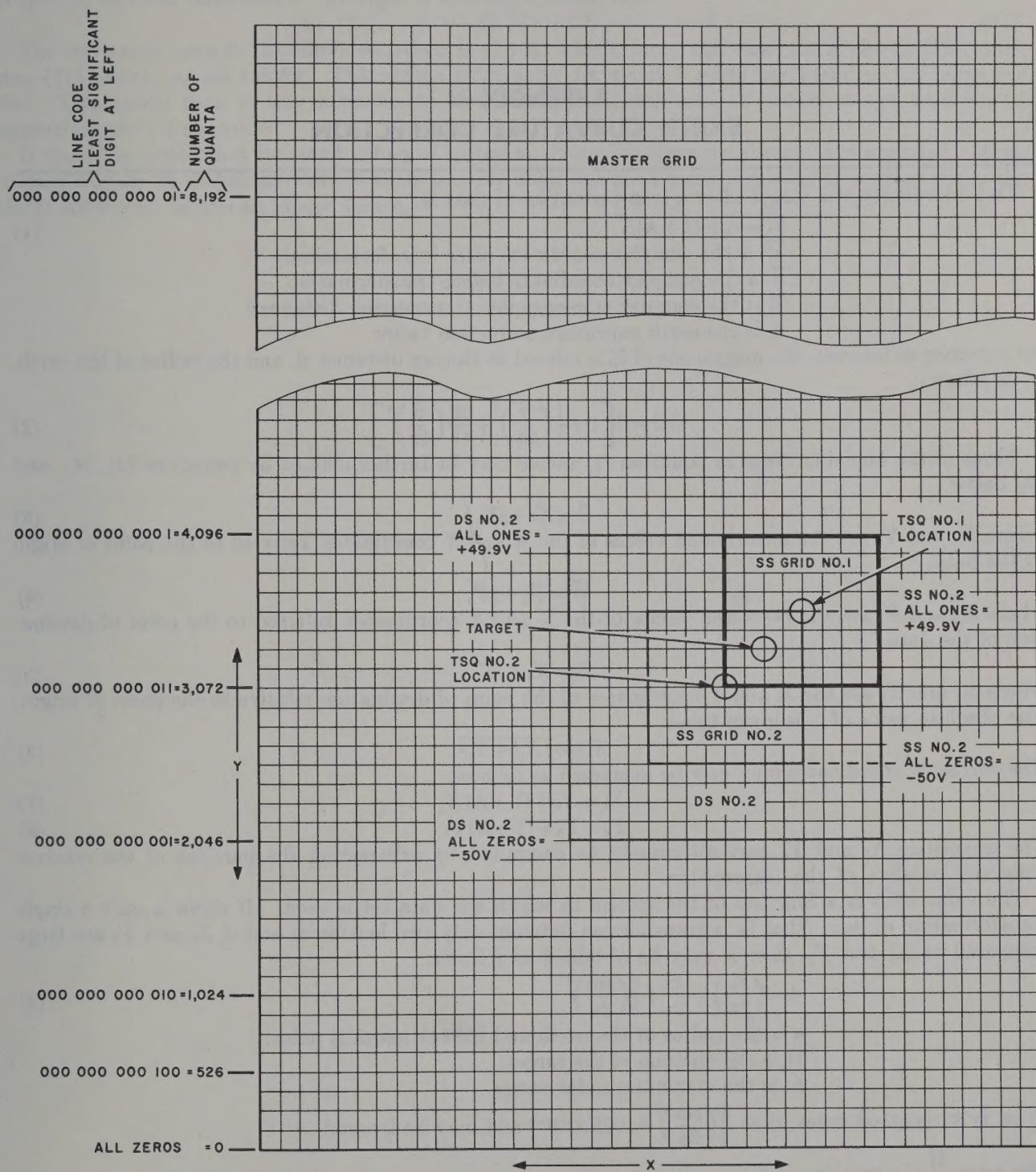
*Zero in 10th digit because the 1 in 11th digit at XMTR was not transmitted.

**Distance equals zero due to selection of master grid, so all zeros. Shown here for illustration only.



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Figure 214. H coordinate parallax, SS and DS.



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Figure 215. X and Y coordinate parallax, SS and DS.

APPENDIX V EARTH CURVATURE CORRECTION

The coordinate of a target after a transformation of data is:

$$\bar{W} = \bar{r}_0 + (1+A)\bar{S} \quad (1)$$

$\bar{W}$ is the complex coordinate after transformation.

$\bar{S}$ is the complex coordinate before transformation.

$\bar{r}_0$ is the complex stereographic transmission distance.

A is the earth curvature correction factor.

As a matter of interest, the magnitude of $\bar{r}_0$ is related to the arc distance, d, and the radius of the earth, a, as follows:

$$|\bar{r}_0| = d \left[1 + \frac{1}{3} \left(\frac{d}{2a} \right)^2 + \frac{2}{15} \left(\frac{d}{2a} \right)^4 \right] \quad (2)$$

Three of the four quantities in equation (1) above may be further defined by equations (3), (4), and (5) below.

$$\bar{S} = X_1 + jY_1 \quad (3)$$

where X_1 and Y_1 are the uncorrected values of the X and Y coordinates, referred to the point of origin of the data.

$$\bar{W} = X_2 + jY_2 \quad (4)$$

where X_2 and Y_2 are the corrected values of the X and Y coordinates, referred to the point of destination of the data.

$$\bar{r}_0 = X_0 + jY_0 \quad (5)$$

where X_0 and Y_0 are the X and Y coordinates of the point of destination relative to the point of origin. The absolute value of r_0 is given by—

$$|\bar{r}_0| = \sqrt{X_0^2 + Y_0^2} \quad (6)$$

The corrected coordinates may now be expressed as follows:

$$X_2 = X_0 + (1+A)X_1 \quad (7)$$

$$Y_2 = Y_0 + (1+A)Y_1 \quad (8)$$

The quantities X_0 and Y_0 may alternately be computed by subtracting the parallax of the receiver from the parallax of the transmitter.

The value of A is a function of the system in which the data set is used. If there is only a single transformation of data (that is, a transmission between only two locations) and if X_0 and Y_0 are large compared to X_1 and Y_1 , then A may be obtained as follows:

$$A = \left(\frac{\bar{r}_0}{2a} \right)^2 - \frac{H}{2a} + \frac{3}{8} \left(\frac{\rho m}{2a} \right)^2 \quad (9)$$

a is the radius of the earth and is 3441 nautical miles.

H is the altitude of the target.

m is the maximum radar range.

If ρm is 80 nautical miles, then $\frac{3}{8} \left(\frac{\rho m}{2a} \right)^2 = 0.05 \times 10^{-3}$ and may be ignored.

The term $\frac{H}{2a}$ is a function of target altitude. Since there is no provision for correction as a function of

H, an average value of H must be used. If average H is 5 nautical miles then $\frac{H}{2a}$ is 0.73×10^{-3} .

Equation (9) above may now be expressed as follows:

$$A = \overline{r_0^2} \times 2.12 \times 10^{-8} - 0.146 \times 10^{-3} \times H \text{ (average)} \quad (10)$$

H (average) here used is expressed in nautical miles.

If $r_0 = 600$ nautical miles and H (average) is 5 nautical miles, then:

$$A = (7.63 \times 10^{-3}) - (0.73 \times 10^{-3}) = 6.9 \times 10^{-3} \quad (11)$$

The correction term in the above equations is $(1+A)$ which, using the value for A obtained in equation (11) above, equals 1.0069. This differs from unity by about 7 parts per 1,000, or 3.5 parts per 500. This means that, in this instance, the earth curvature correction, at extreme range, amounts to approximately 3.5 quanta.

It should be noted that for small values of r_0 (not as shown in above equations), A is negative. Also, it should again be cautioned that, if there is more than one such transformation of a given data, the above correction factors no longer suffice.

GLOSSARY

Section I. ABBREVIATIONS

AGC.....	Automatic gain control	LU.....	Lockup
ALL.....	Automatic start gate	MS.....	Manual start
ALU.....	Auxiliary lockup	MSPG.....	Manual start pulse generator
ALUR.....	Auxiliary lockup release	OSD.....	Off scale detection
AND.....	Coincidence gate	PH.....	H coordinate parallax
AR.....	Auxiliary relay	PS.....	Pulse shaper
AUX.....	Auxiliary	PSR.....	Parallax storage register
AZS.....	Automatic zero set	PX.....	X coordinate parallax
BC.....	Binary counter	PY.....	Y coordinate parallax
CCS.....	Clear carry storage	Rf.....	Feedback resistance
CG.....	Combination gate (positive and negative)	RIP.....	Read-in pulse
CON.....	Continuous operation	RPLU.....	Reference short circuit protection lockup
CP.....	Clock pulse	RPD.....	Reference protection delay
CPG.....	Coincidence pulse generator	RPR.....	Reference short circuit protection relay
DLU.....	Data lockup	RS.....	Remote start
DLUR.....	Data lockup release	RSR.....	Remote start relay
DR.....	Data relay	RSRP.....	Remote start receiver pulse
DS.....	Double scale	RT.....	Reset
DSA.....	Data storage amplifier	RTC.....	Ready tone control
DSR.....	Data storage relay	SLU.....	Storage lockup
ECCA.....	Earth curvature correction adjust	SLUR.....	Storage lockup release
ECCLU.....	Earth curvature correction lockup	SP.....	Sampling pulse
ECCR.....	Earth curvature correction relay	SR.....	Shift register
ECR.....	Earth curvature relay	SRC.....	Shift register control
ECRLU.....	Earth curvature relay lockup	SS.....	Single scale
ENC.....	Encoder	STC.....	Start transmitter control
ERP.....	Encoder reset pulse	STP.....	Start transmitter pulse
ESP.....	Encoder start pulse	TCG.....	Time control gate
Etgt.....	Target voltages	TR.....	Tens ring stage
F/F.....	Flip-flop circuit (bistable)	TRR.....	Tens ring reset
F/O.....	Flip-zero circuit (monostable)	TSG.....	Time slot gate
FSC.....	Frame start control	UR.....	Units ring stage
FLU.....	Feedback lockup	URR.....	Units ring reset
FR.....	Feedback relay	XR.....	X coordinate relay
GATE.....	Transmission gate	XRLU.....	X coordinate relay lockup
G/S.....	Ground/slant	YR.....	Y coordinate relay
HR.....	H coordinate relay	YRLU.....	Y coordinate relay lockup
HRLU.....	H coordinate relay lockup	ZP.....	Set zero pulse
HUP.....	Height unknown pulse		

Section II. DEFINITIONS OF UNUSUAL TERMS

- Auxiliary data.* Information not necessarily related to coordinate data. Provisions are made for its transmission during each frame.
- Auxiliary lockup.* Bistable (F/F) circuits which actuate the auxiliary data relays. Used in the coordinate data receiver.
- Auxiliary lockup release.* A pulse generating circuit to release the auxiliary lockups at the required time in each frame. Used in the coordinate data receiver.
- Auxiliary relays.* Relays, actuated by the auxiliary lockups, which store auxiliary binary data for use by associated equipment. Used in the coordinate data receiver.
- Automatic zero set.* A signal developed in the automatic zero set to maintain encoder and decoder dc amplifier balance.
- Binary counter.* An arrangement of bistable and monostable circuits and associated gates, to count successive pulses by dividing their number by 2 in each stage.
- Bistable circuit.* A circuit one transistor, having two stable conditions, ON and OFF. It changes conditions under the influence of externally applied voltage pulses. See appendix III.
- Bit.* A binary digit.
- Clear carry storage.* A signal used to clear the carry storage section of the serial adder of a ONE left over from the preceding frame. Used in the data set receiver.
- Clock pulse.* The basic timing pulse of the data set. It occurs 750 times a second and has an amplitude of about 9 volts, is negative-going, and has a duration of about 1.5 microseconds.
- Coincidence pulse generator.* A combination of circuit elements which produces a voltage pulse only when two or more activating pulses are present simultaneously.
- Combination gate.* A combination of circuit elements which produces a voltage pulse when an actuating pulse and enabling biases are present.
- Continuous operation.* A mode of operation whereby one complete frame or train of data is transmitted, and is immediately followed by succeeding frames or trains of data.
- Coordinate multiplex.* A method used for connecting coordinate voltages in proper sequence to the encoder.
- Data lockup.* A bistable circuit which actuates the data relays under control of time slot voltages and clock pulses.
- Data relay.* A relay, actuated by a data lockup, which applies voltages to the decoder network for conversion from digital to analog information.
- Binary number.* A number made up of binary digits, using two as the radix, or base.
- Binary word.* A word consisting of binary digits.
- Digital data.* Data expressed by ONE's and ZERO's.
- Data storage amplifier.* A single stage cathode follower for temporarily storing coordinate data.
- Data storage relay.* A relay used for connecting analog coordinate voltage to its data storage amplifier at appropriate times.
- Double scale.* A mode of operation where data transmitted and received is for use on a double scale grid.
- Earth curvature correction adjust.* An adjustable resistance used in the encoder and decoder for modifying coordinate data to correct for curvature of the earth.
- Earth curvature correction lockup.* A bistable circuit which actuates the earth curvature correction relay.
- Earth curvature correction relay.* A relay used in the transmitter and receiver for inserting earth curvature correction resistance.
- Earth curvature relay lockup.* A bistable circuit used to actuate the earth curvature correction relay.
- Encoder.* A part of the data set transmitter used to convert analog data to digital data.
- Encoder reset pulse.* A voltage pulse developed at specified times to cause the encoder to reset the sweep voltage in preparation for the succeeding data count.
- Encoder start pulse.* A voltage pulse developed at specified times to cause the encoder to start the sweep voltage at the beginning of each coordinate count.
- Feedback lockup.* A bistable circuit used to actuate the feedback relay in the coordinate data receiver.
- Feedback relay.* A relay used to connect the output of each data storage amplifier to the input

- of the decoder amplifier as feedback voltage. It is also used in connection with the test cathode follower for adjustment purposes.
- Feedback relay lockup.* A bistable circuit used to actuate the feedback relay at designated times.
- Flip-flop.* A bistable transistor circuit.
- Flip-zero.* A monostable transistor circuit.
- Frame.* One complete sequence of ready, synchronizing, auxiliary, and coordinate data for a single target.
- Frame start control.* A gate circuit used to start the ring counter stages at appropriate times.
- H coordinate relay.* A relay used to connect its associated coordinate analog voltage to the encoder input at appropriate times.
- H coordinate relay lockup.* A bistable circuit used to actuate the H coordinate relay.
- H parallax.* A binary number added to the coordinate digital data to correct for parallax between different stations of the system.
- Lockup.* A bistable circuit used to actuate a relay at designated times.
- Monostable circuit.* A transistor circuit having only one stable condition. It remains in the OFF condition until triggered ON by an external pulse, after which it immediately returns to OFF. See appendix III.
- Parallax storage register.* A bistable circuit which accepts the first digit of parallax one time slot ahead of the first data digit to present them in coincidence to the serial adder.
- Pulsing relay.* A relay used in the multiplexer to connect alternate targets to odd and even lines.
- Pulsing relay lockup.* A bistable circuit used to actuate the pulsing relay.
- Quantum.* The smallest interval of analog voltage that can be distinguished after conversion to a binary number.
- Read-in gate.* A time control gate.
- Read-in pulses.* Gated clock pulses used to trigger data and auxiliary lockups.
- Ready tone control.* A function of the transmitter which gates the modulator to transmit 600-cycle ready signal for three time slots.
- Remote start.* A function which causes the transmitter to stop sending at the end of a frame or train, and to wait for a start signal from a remote station before resuming transmission of a single frame or train.
- Remote start relay.* The relay which connects the transmitting line to the amplifier-detector in the transmitter during remote start operation. Upon receipt of a remote start signal it connects the line to the transmitter output.
- Reset.* A function which resets the ring counters in preparation for a new frame.
- Sampling pulse.* A pulse developed in the receiver slot center gate at the coincidence of every eighth pulse from the 6,000-pps generator. It is used to trigger the clock pulse generator.
- Set zero pulse.* A positive-going pulse, 15 to 40 microseconds in duration, and approximately 3.5 volts in amplitude. It occurs a few microseconds ahead of the clock pulse and is used to restore a bistable circuit to the OFF condition.
- Shift register.* A bistable circuit having a memory output circuit. The bistable circuit element, when turned ON, stores a digit, and upon being reset, holds the input of the succeeding shift register stage open to allow a clock pulse to enter.
- Single scale.* A mode of operation where data transmitted and received is intended for use on a single scale grid.
- Start transmitter control.* A signal developed in the remote start section to start the transmitter upon receipt of a remote start signal.
- Storage lockup.* A bistable circuit used to actuate a data storage relay.
- Storage lockup release.* A monostable circuit used to reset a storage lockup.
- Tens ring reset.* A monostable circuit used to reset the tens ring counters.
- Tens ring stage.* A bistable circuit used as a decade counter, and operated as a part of a chain with other tens ring counter stages. The chain advances one stage for every ten counts of the units ring counters, and with them, generates the time slot gate voltage.
- Time slot.* A division of a transmitted or received frame. All timing functions of the data set are based on time slots.
- Time control gate.* A gate circuit, usually consisting of a diode, a resistor, and a capacitor. It is used to allow a clock pulse to pass through it when it is enabled by a time slot voltage.
- Transmission gate.* A gate circuit, usually consisting of a diode, a resistor, and a capacitor.

It allows a clock pulse to pass through it when the diode is enabled by a bias voltage.

Units ring stage. A bistable circuit used as a decade counter, and operated as a part of a chain with other units ring stages. The chain advances continuously, and, used with the tens ring stages, generates the time slot gate voltage.

Units ring reset. A monostable circuit used to reset the units ring counters.

X coordinate relay. A relay used to connect the X coordinate target voltage to the input of the encoder.

X coordinate relay lockup. A bistable circuit which actuates the X coordinate relay.

X parallax. A word added to the X coordinate word at both the transmitter and receiver to correct for parallax in the X coordinate.

Y coordinate relay. A relay used to connect the Y coordinate target voltage to the input of the encoder.

Y coordinate relay lockup. A bistable circuit which actuates the Y coordinate relay.

Y parallax. A word added to the Y coordinate word at both the transmitter and receiver to correct for parallax in the Y coordinate.

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[AG 413.44 (10 Apr 59)]

By Order of *Wilber M. Brucker*, Secretary of the Army:

MAXWELL D. TAYLOR,
General, United States Army,
Chief of Staff.

Official:

R. V. LEE,
Major General, United States Army,
The Adjutant General.

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US ARADCOM (2)	USA Sig Engr Agcy (1)	11-7 (2)
US ARADCOM Rgn (2)	USA Comm Agcy (2)	11-16 (2)
OS Maj Comd (5)	USA Sig Eqp Spt Agcy (2)	11-57 (2)
OS Base Comd (5)	USA Sig Msl Spt Agcy (13)	11-500 (AA-AE) (2)
Log Comd (5)	WRAMC (1)	11-587 (2)
USA Ord Msl Comd (3)	AFIP (1)	11-592 (2)
MDW (1)	AMS (1)	11-597 (2)
Armies (5) except First USA (7)		

NG: State AG (3); units—same as Active Army except allowance is one copy to each unit.

USAR: None.

For explanation of abbreviations used, see AR 320-50.

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FIGURES

2	132	165 (4)	174 (2)	187
3	133	168	174 (3)	196
4	162 (1)	169	176	197
7	162 (2)	170 (1)	177 (1)	199
20	162 (3)	170 (2)	177 (2)	202
81	162 (4)	171 (1)	177 (3)	203 (1)
82	163 (1)	171 (2)	179	203 (2)
83	163 (2)	171 (3)	180	204
88	163 (3)	171 (4)	181	205
101	164 (1)	172 (1)	182 (1)	206
108	164 (2)	172 (2)	182 (2)	207 (1)
109	165 (1)	172 (3)	184	207 (2)
111	165 (2)	173	185	208
131	165 (3)	174 (1)	186	211

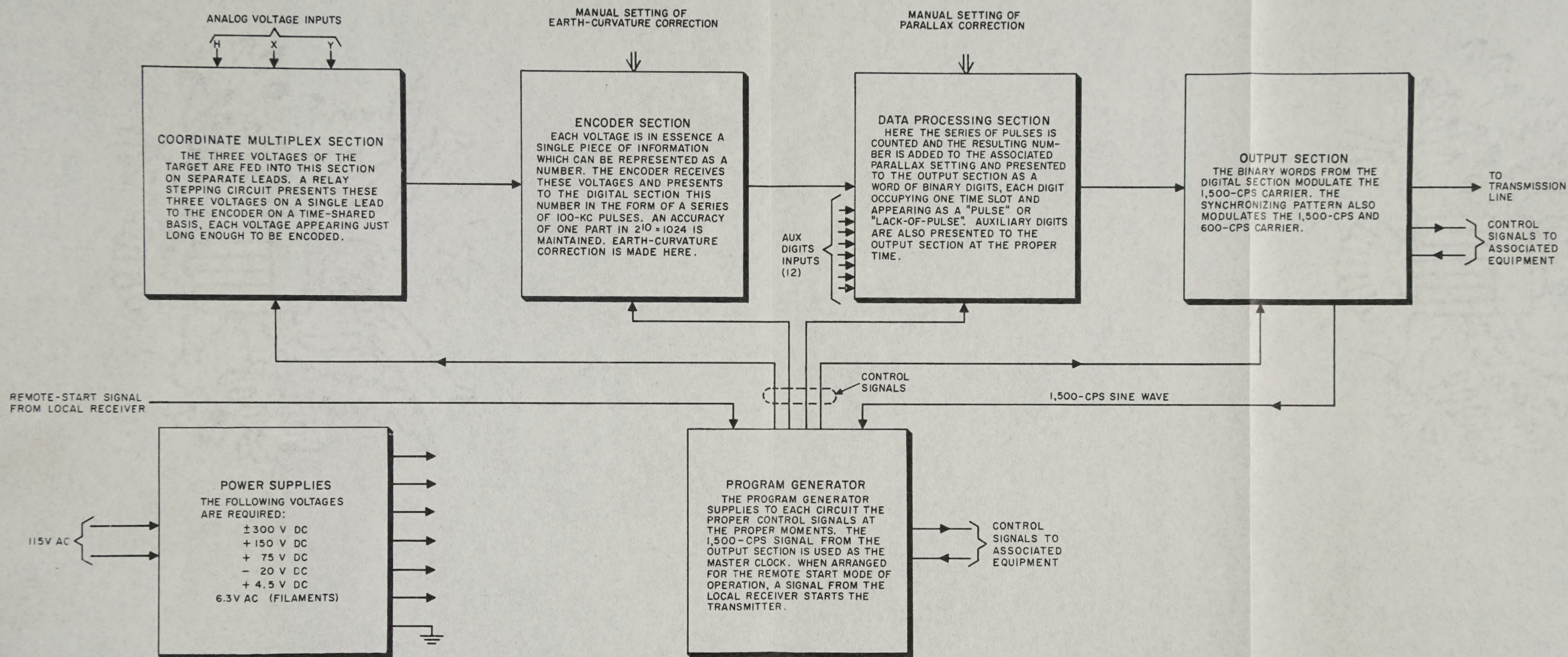


Figure 3. Coordinate data transmitter unit T-721/TSQ-36, functional block diagram.

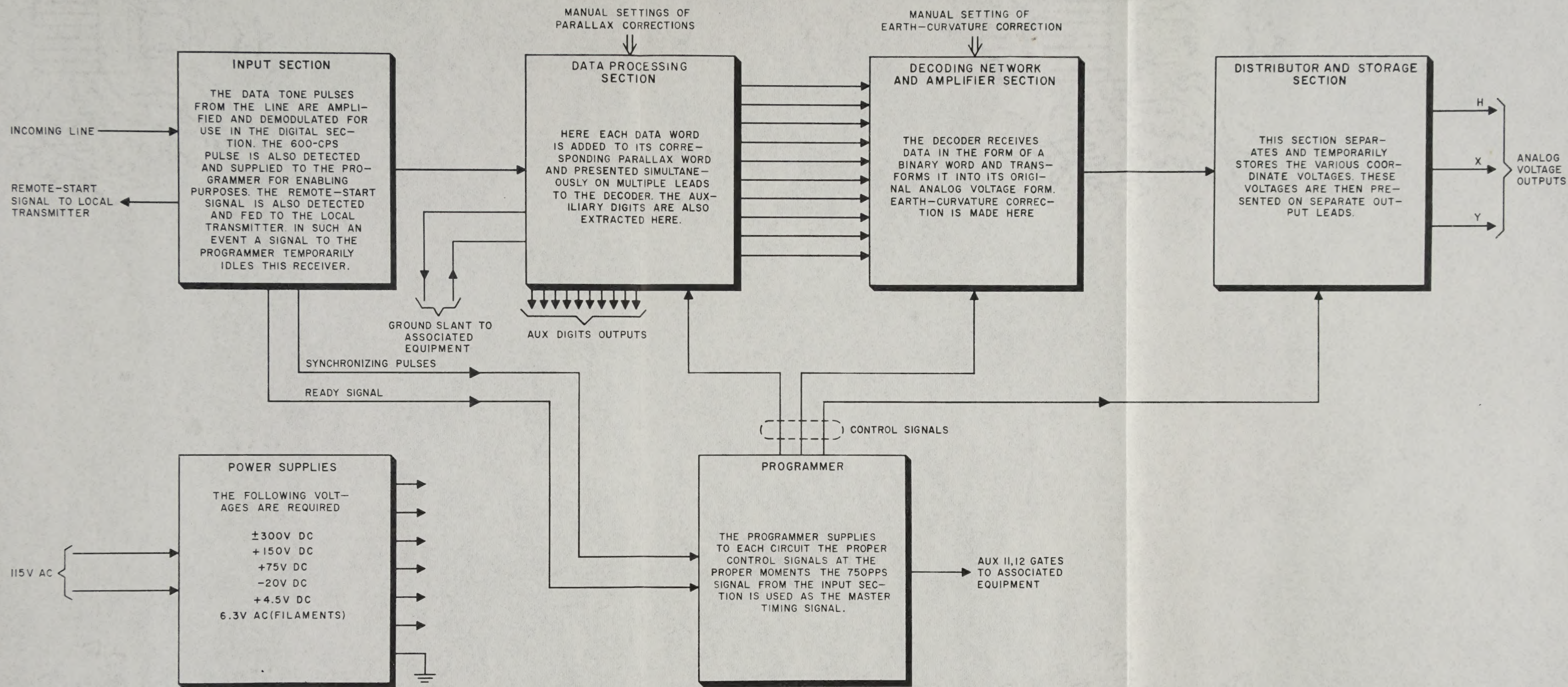


Figure 4. Coordinate data receiver unit R-930/TSQ-36, functional block diagram.

NOTE:
 SYNC AND DATA PULSES CONSIST OF TWO CYCLES
 OF A 1500-CPS TONE.

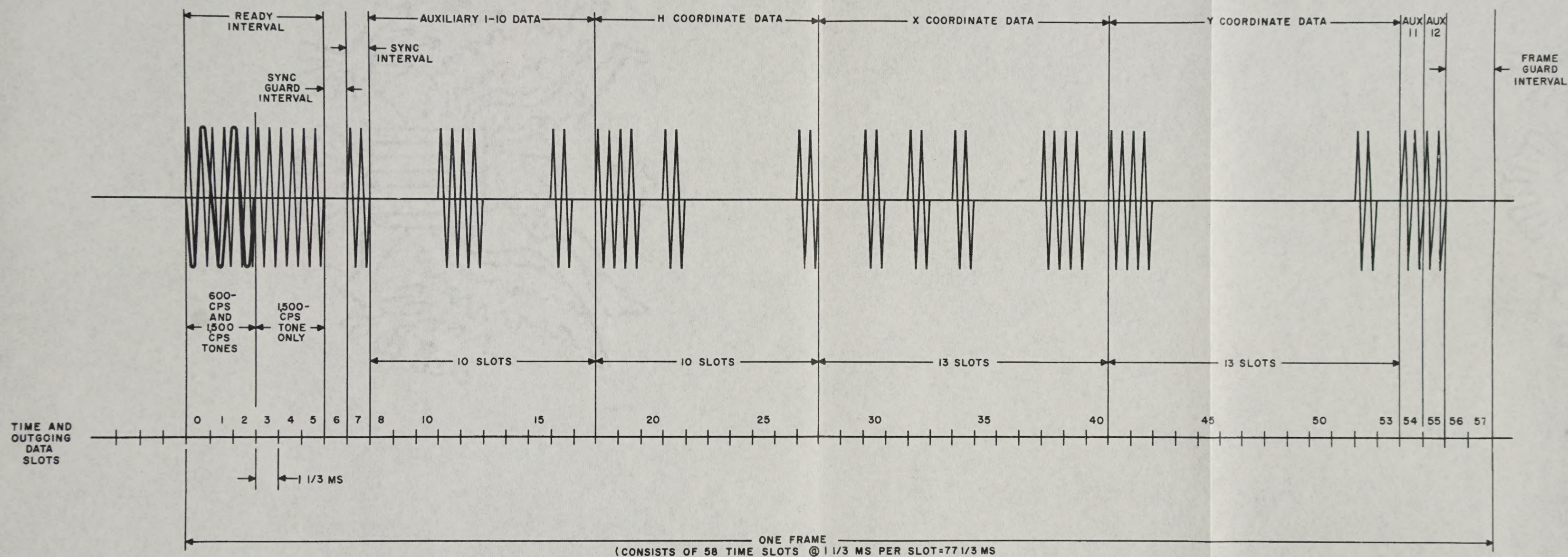


Figure 2. Typical cycle of transmitted message.

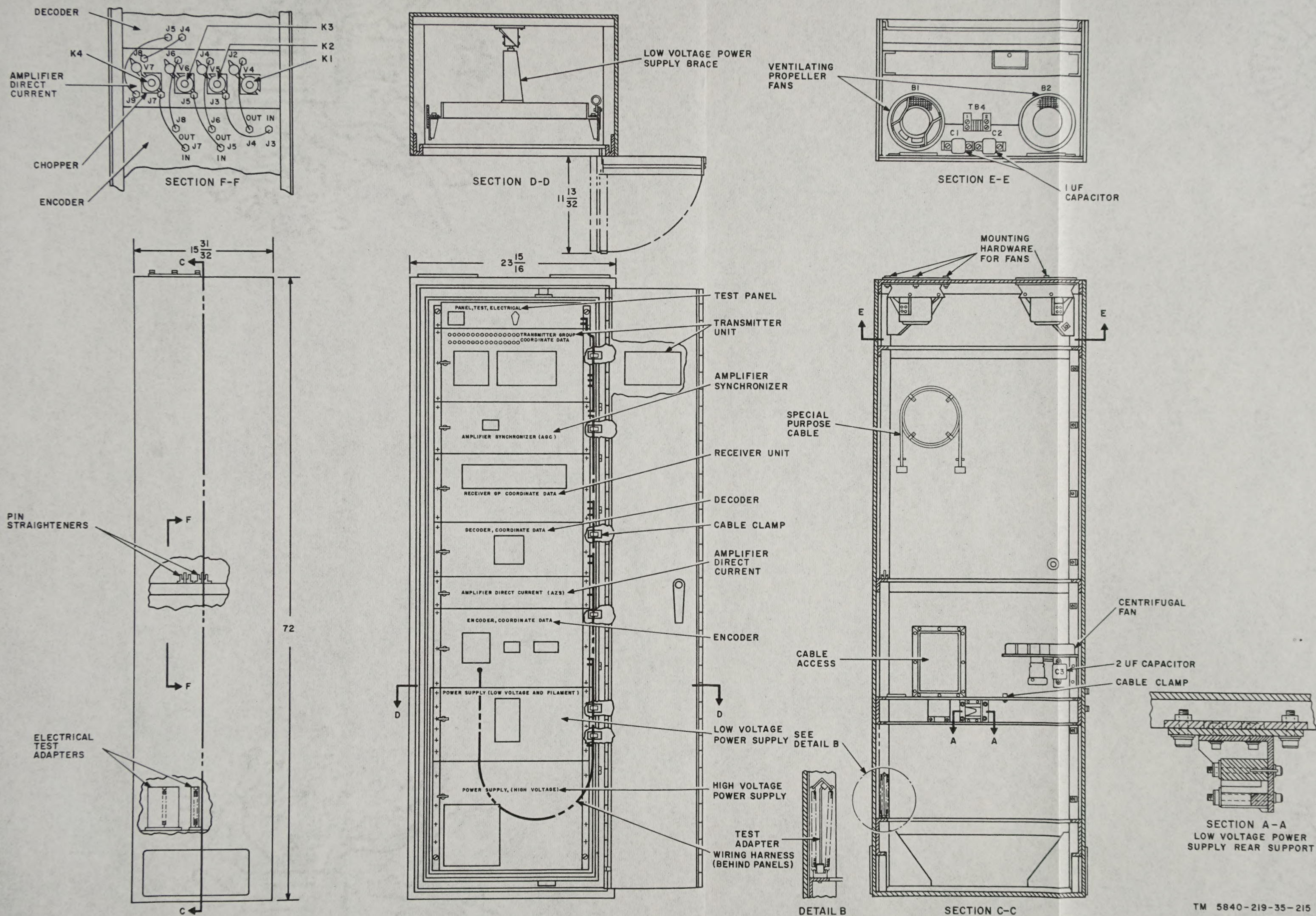


Figure 7. Coordinate data set AN/TSQ-36, installation drawing.

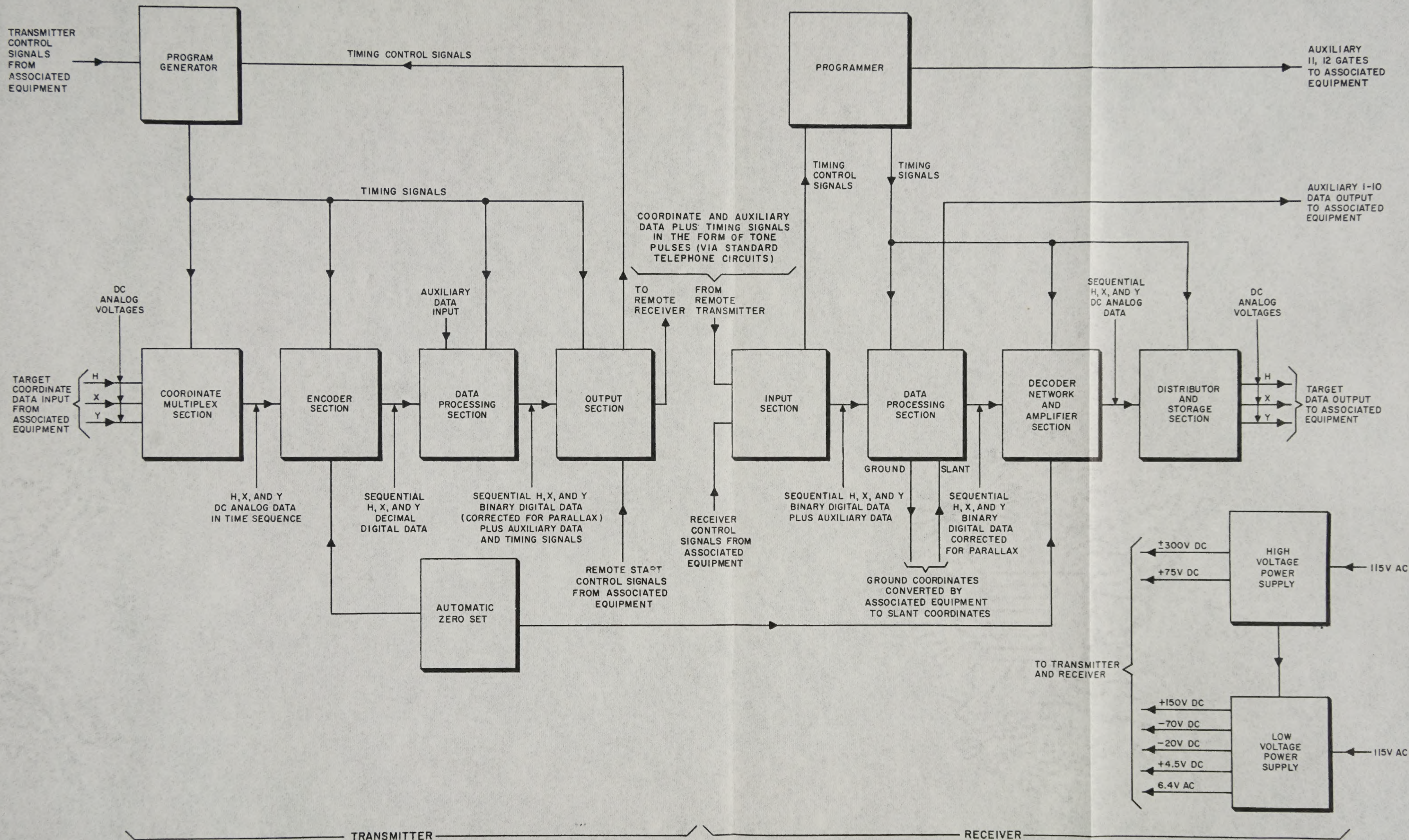
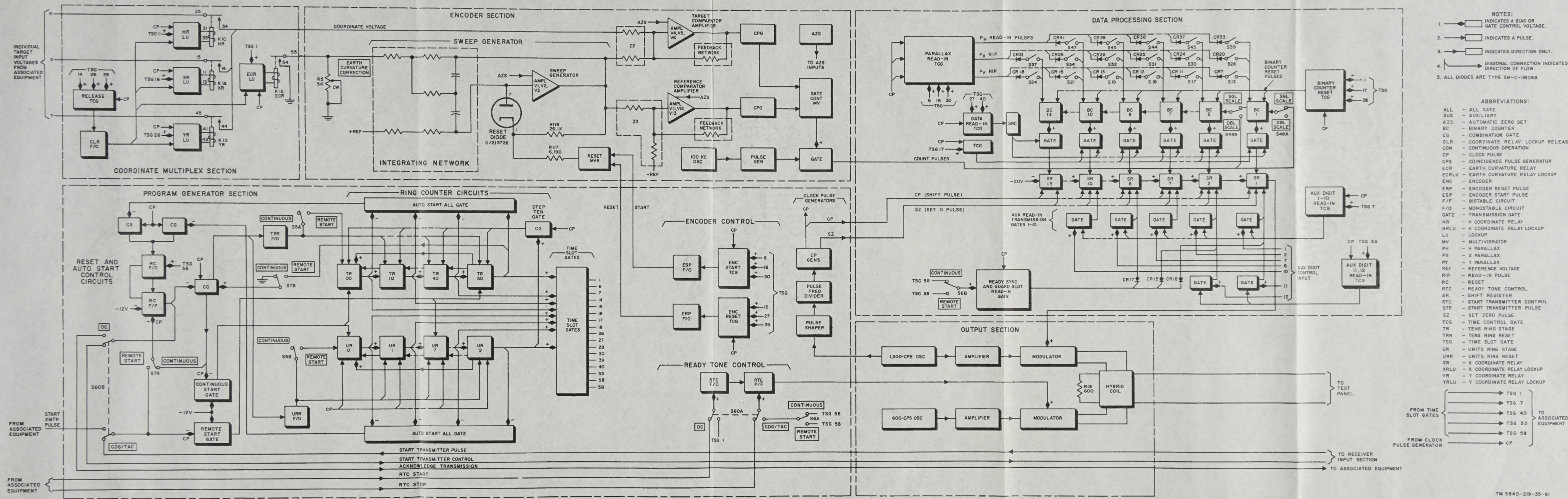


Figure 20. Coordinate data set AN/TSQ-36, basic block diagram.



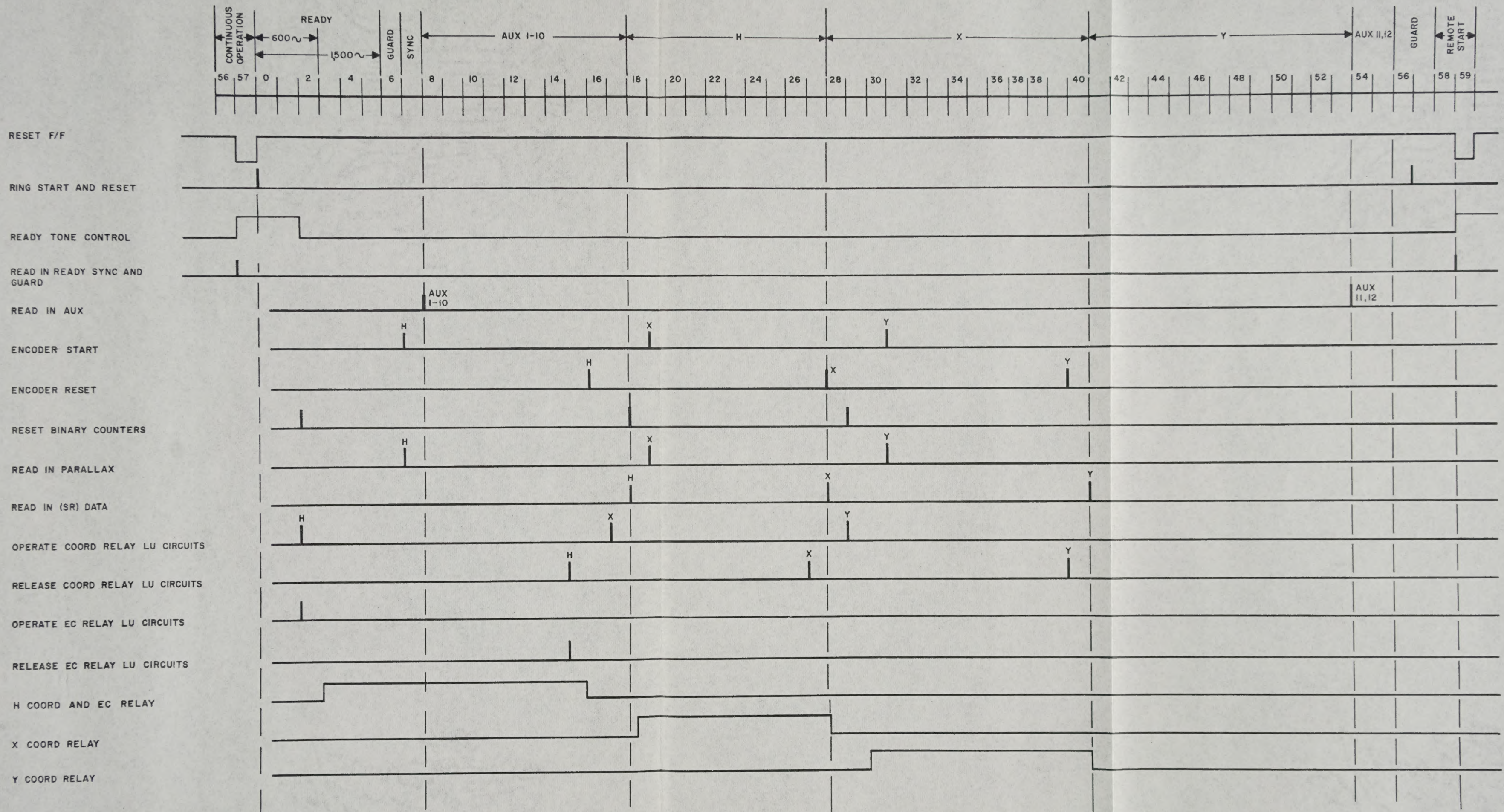


Figure 82. Transmitter, timing diagram.

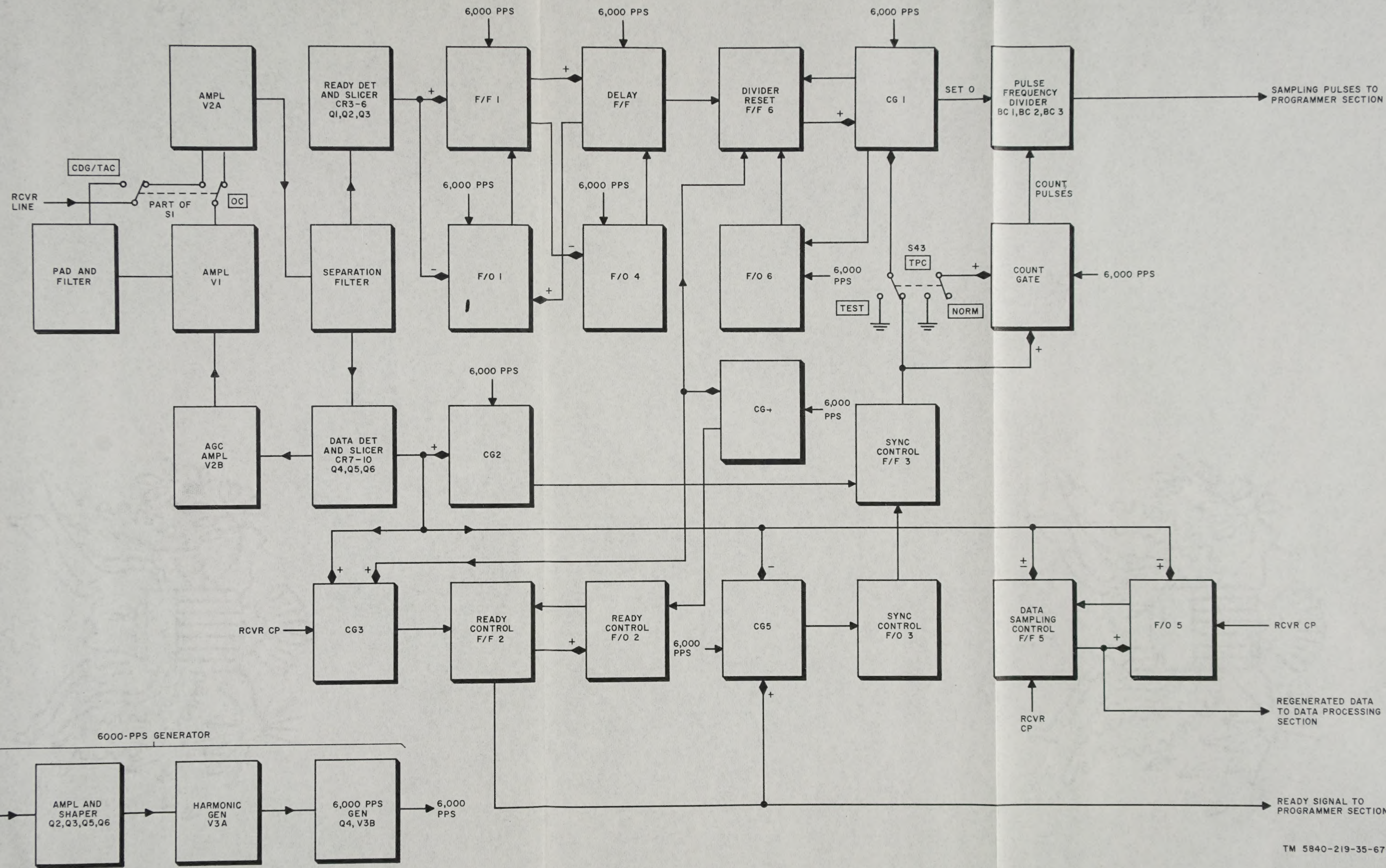
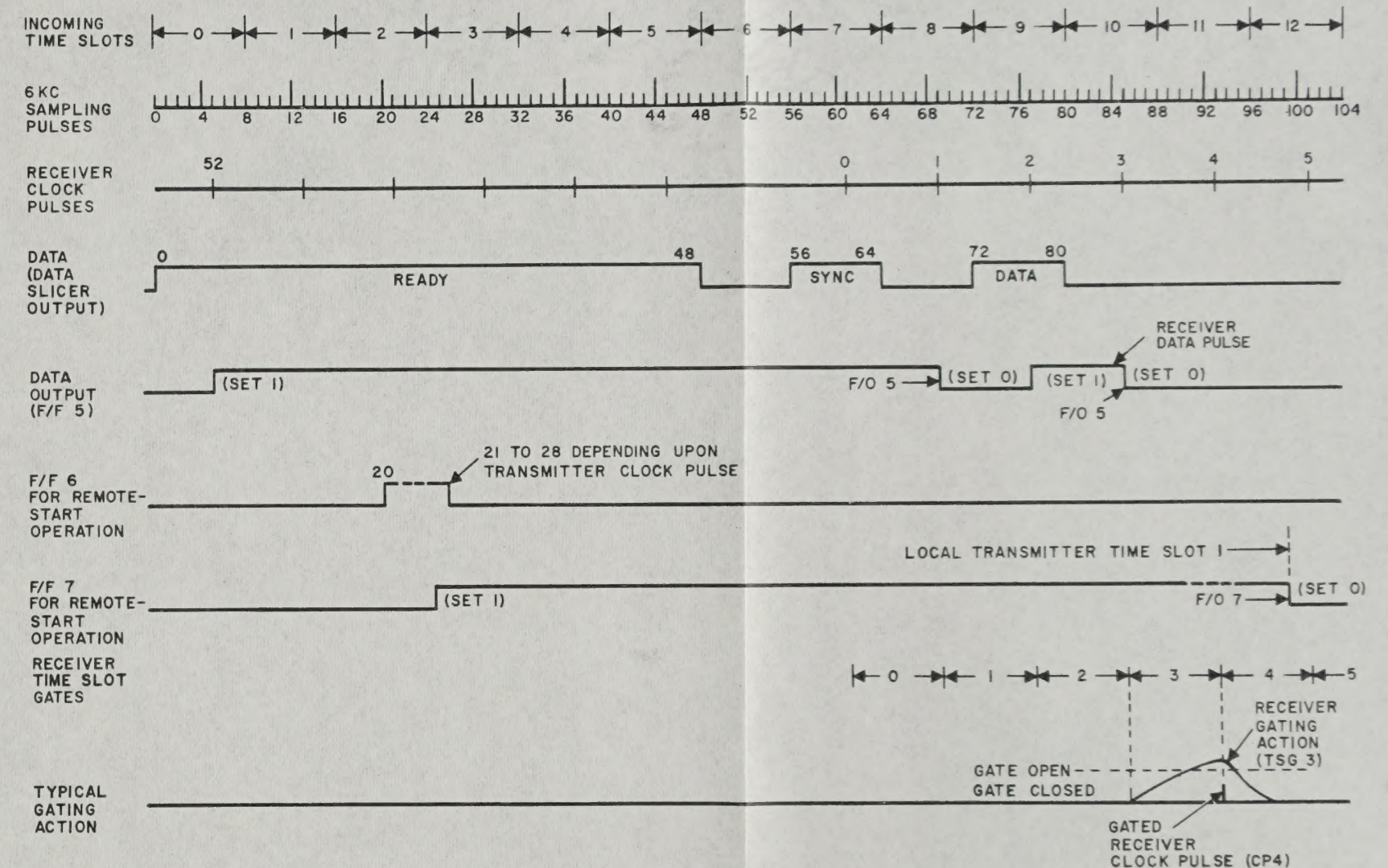
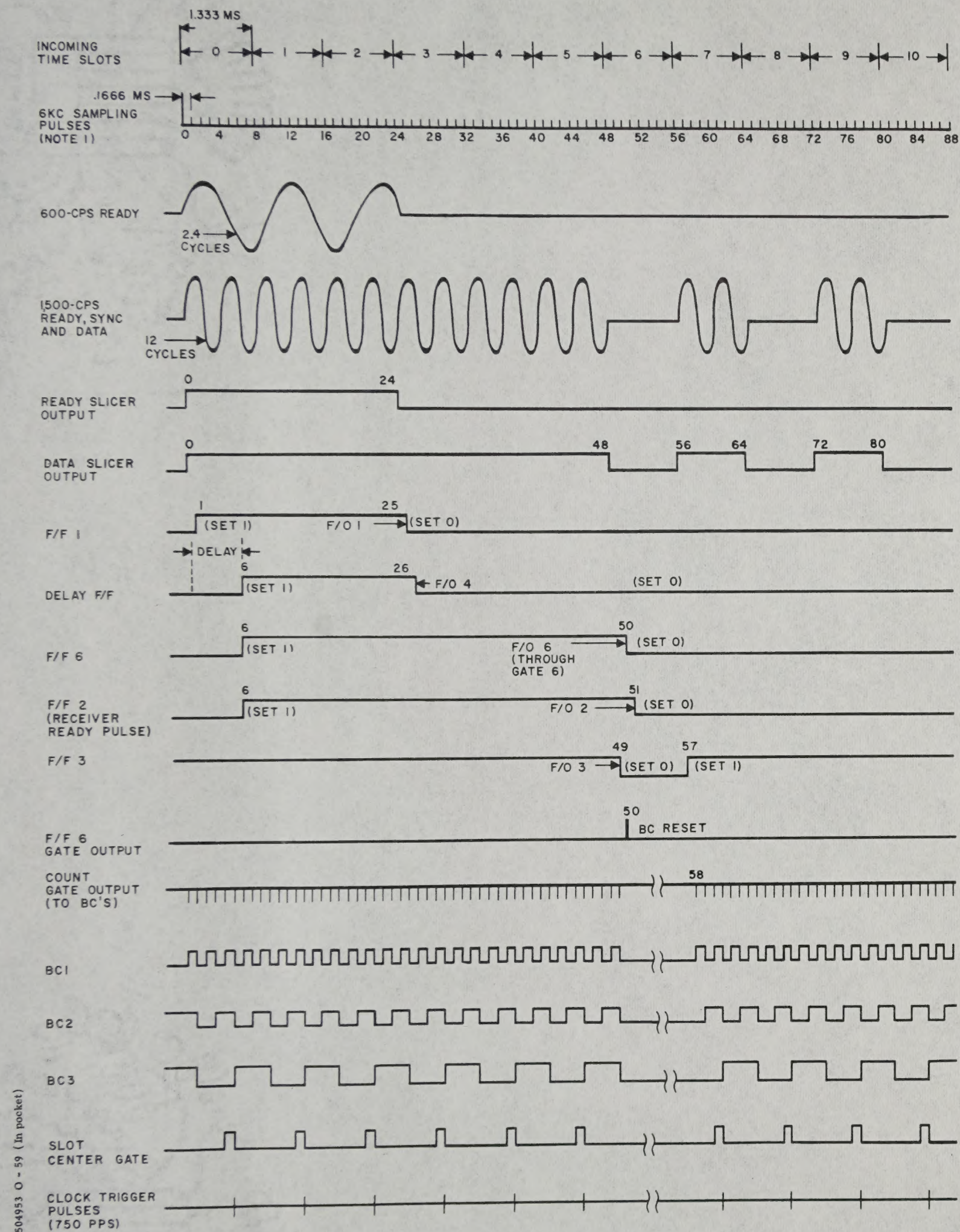


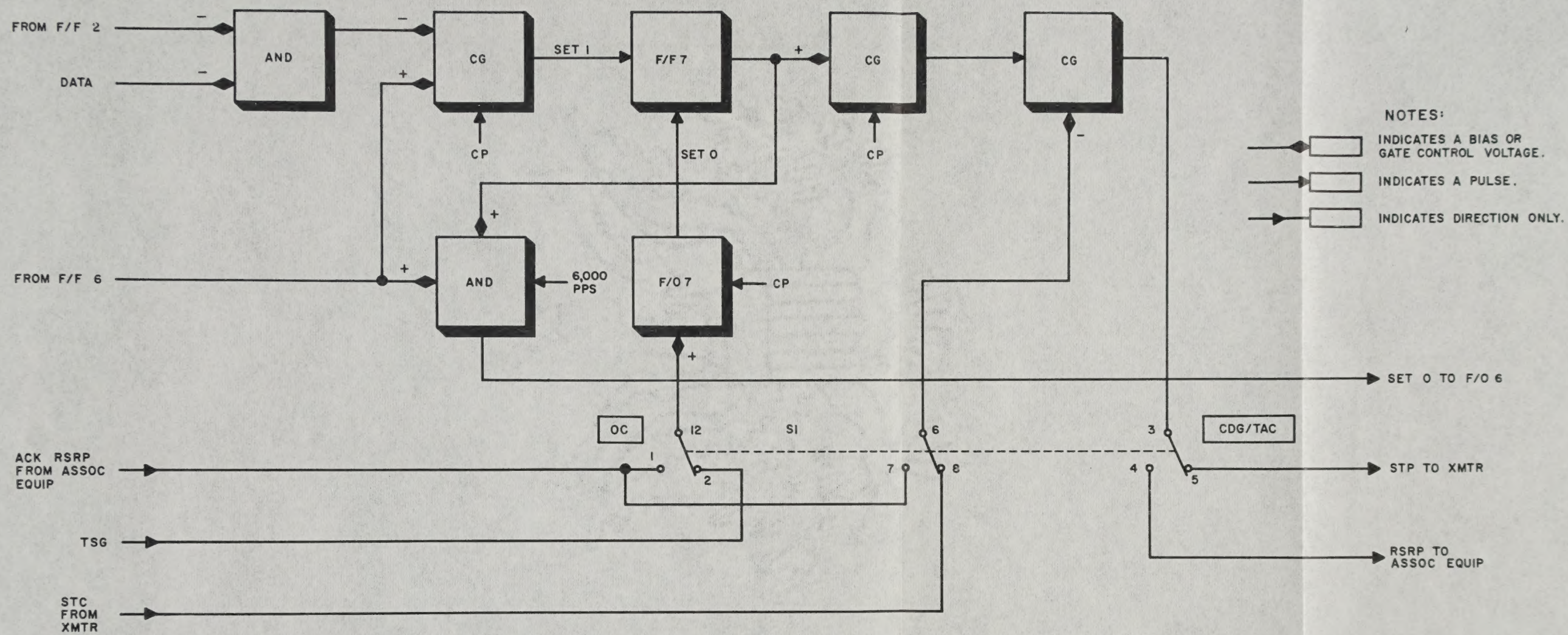
Figure 83. Receiver input section, detailed block diagram.



NOTE

THE TIMING RELATION BETWEEN THE 6KC SAMPLING PULSES AND THE INCOMING DATA IS STRICTLY RANDOM. THE RELATIONSHIP SHOWN IS FOR CONVENIENCE OF IDENTIFICATION ONLY, HOWEVER, A SHIFT OF THE INCOMING DATA TIMING CAN NOT RESULT IN A GREATER ERROR THAN ± 83 MICROSECONDS.

Figure 88. Receiver input section, timing diagram.



504953 O - 59 (In pocket)

TM 5840-219-35-82

Figure 101.—Remote start circuits, block diagram.

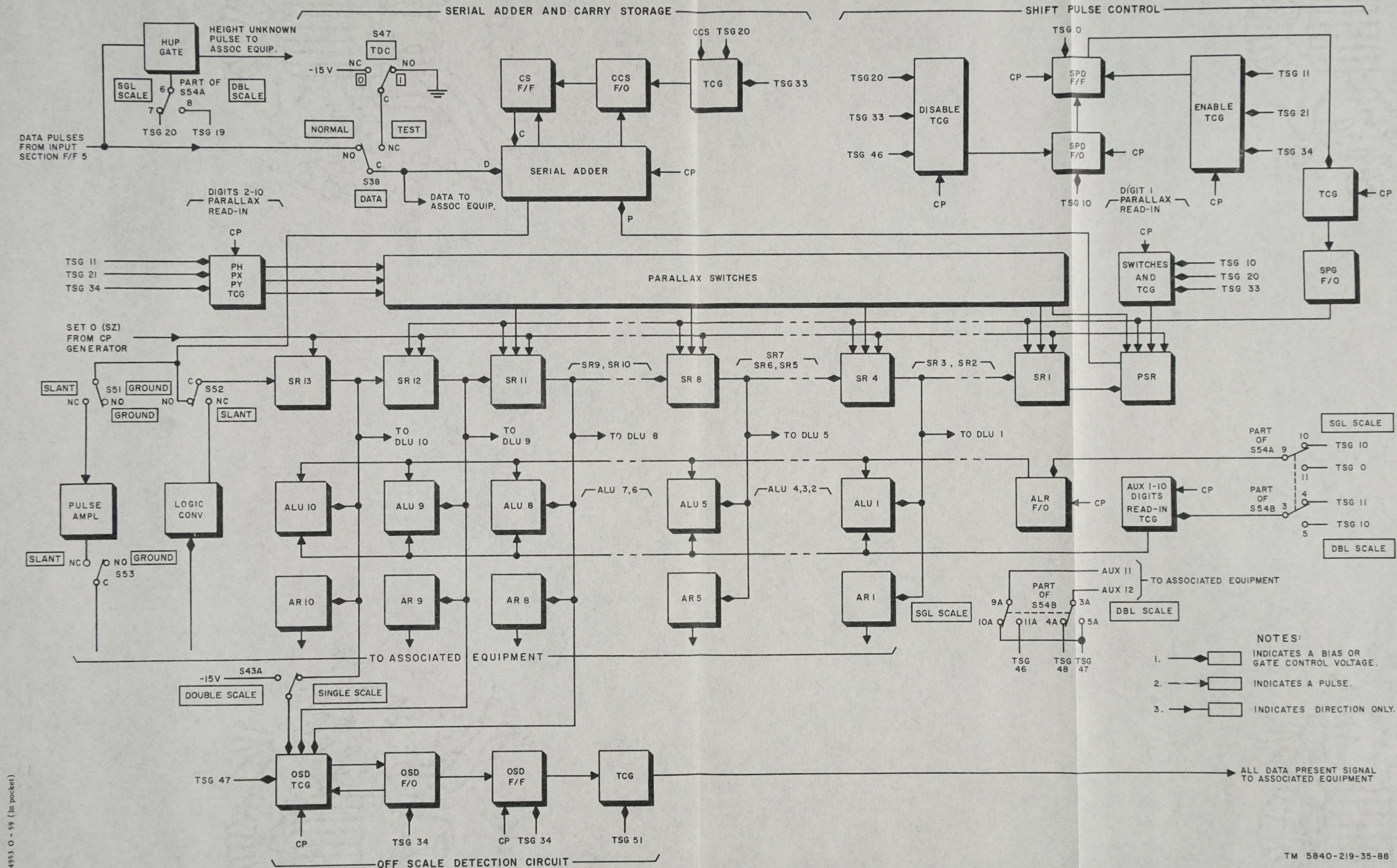
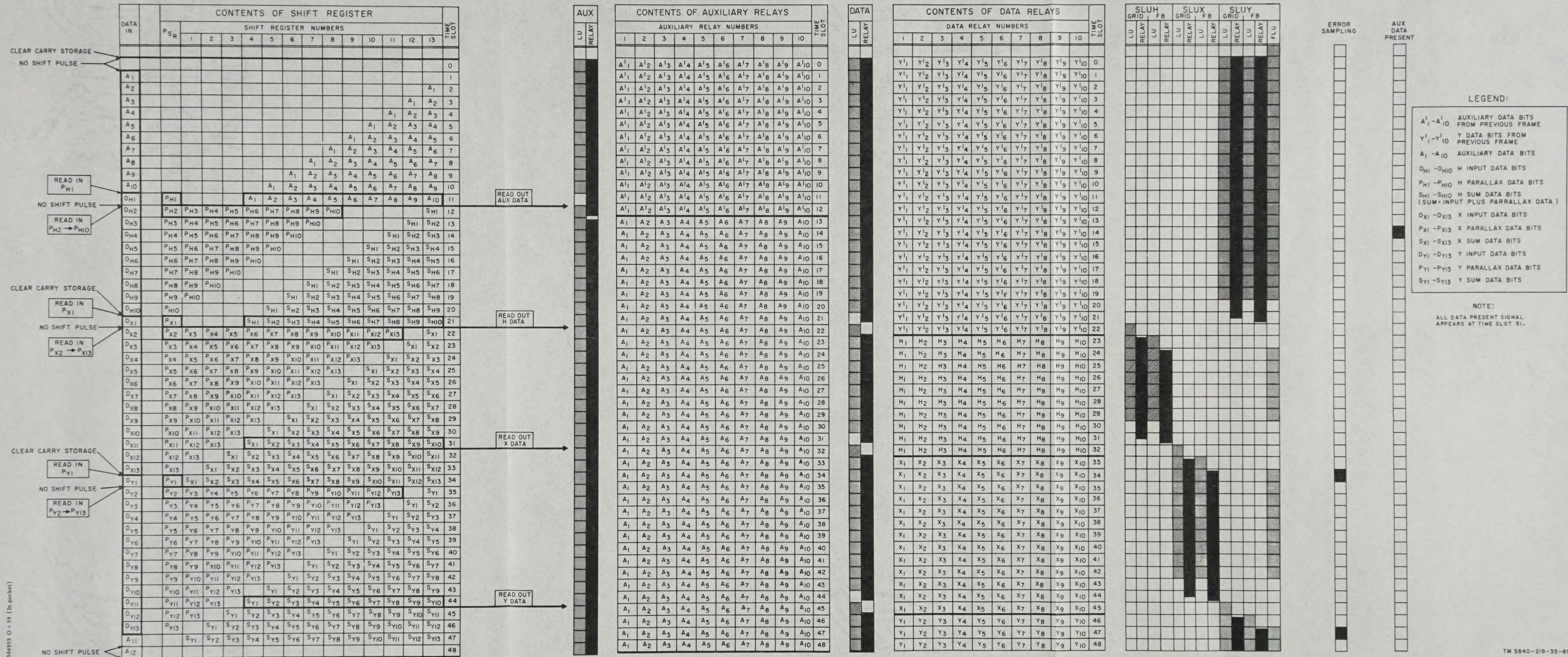


Figure 108. Receiver data processing, block diagram.



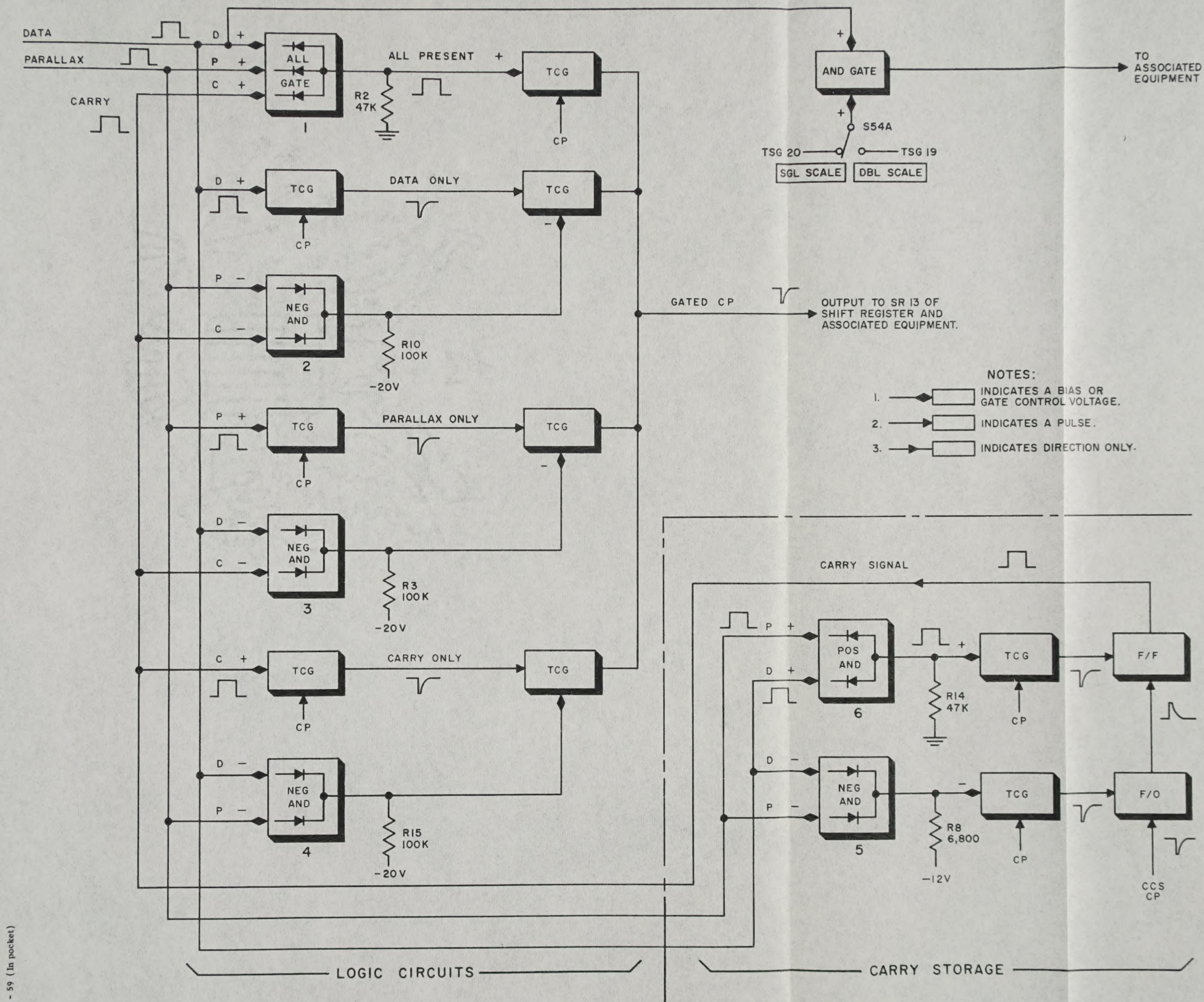


Figure 111. Serial adder, block diagram.

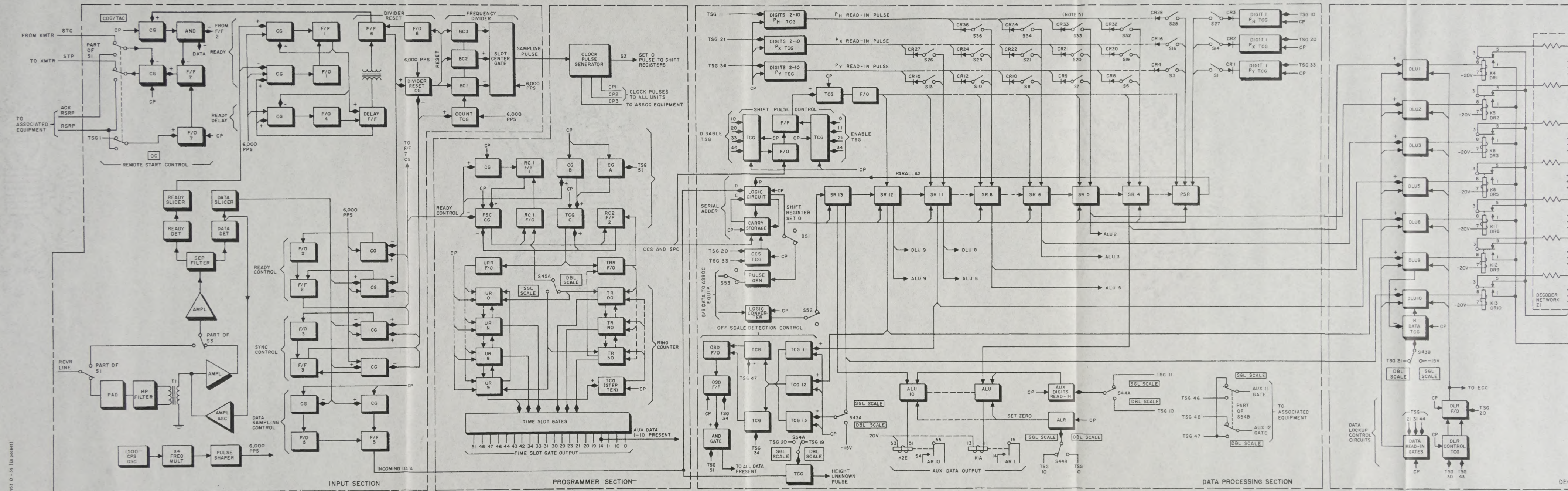
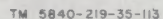
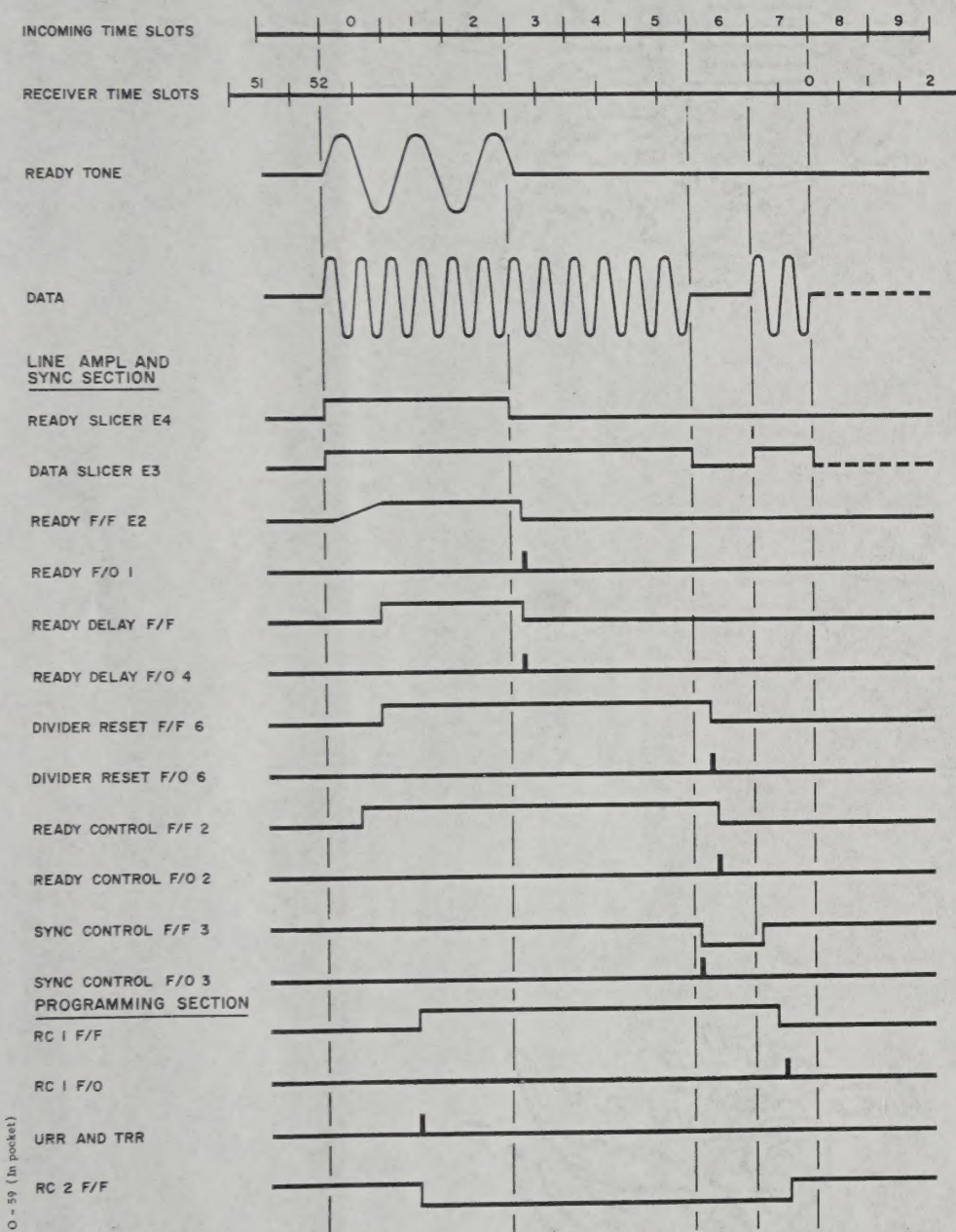


Figure 131. Receiver, block diagram.



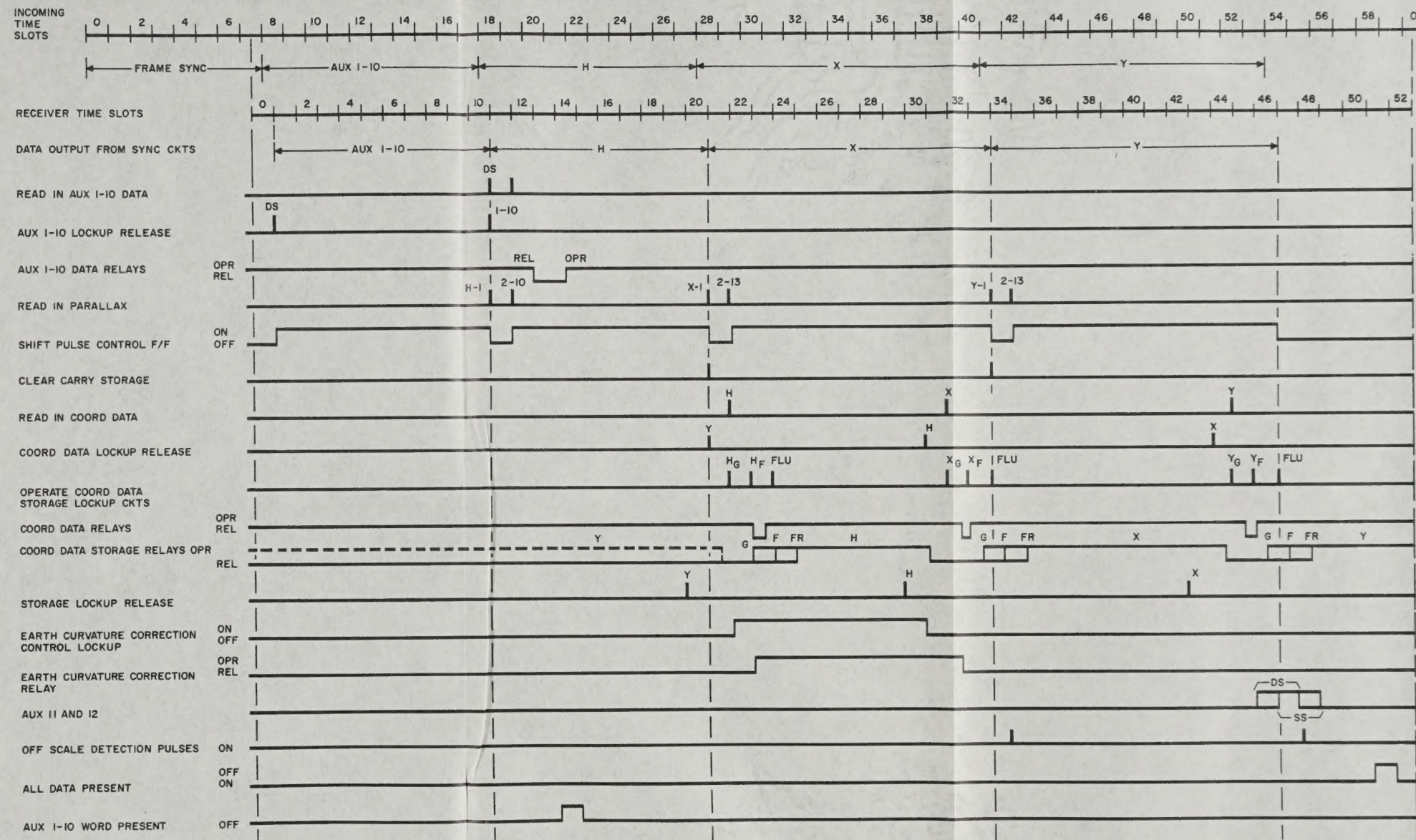
TM 5840-219-35-113

SYNCHRONIZING AND PROGRAMMING



A

DATA PROCESSING



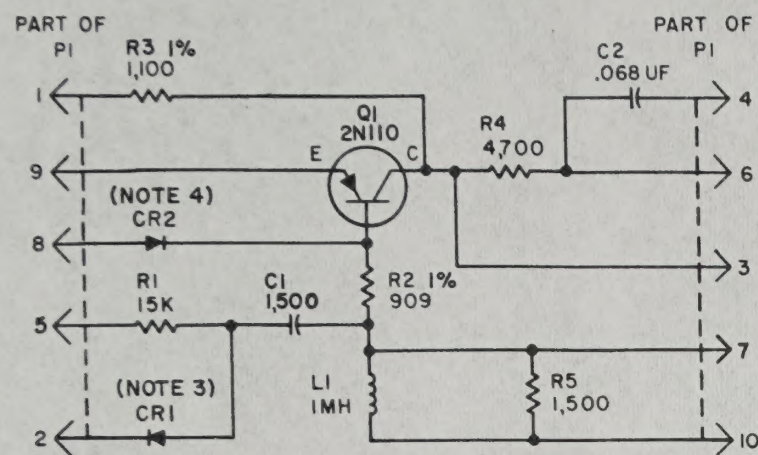
B

ABBREVIATION	FUNCTIONAL DESIGNATION
AUX	AUXILIARY
DS	DOUBLE SCALE
F	FEEDBACK RELAY
F/F	BISTABLE CIRCUIT
FLU	FEEDBACK LOCKUP
F/O	MONOSTABLE CIRCUIT
FR	FEEDBACK RELAY
G	GRID RELAY
H	H COORDINATE
Hf	H COORDINATE FEEDBACK
Hg	H COORDINATE GRID
SS	SINGLE SCALE
TRR	TENS RING RESET
URR	UNITS RING RESET
X	X COORDINATE
Xf	X COORDINATE FEEDBACK
Xg	X COORDINATE GRID
Y	Y COORDINATE
Yf	Y COORDINATE FEEDBACK
Yg	Y COORDINATE GRID

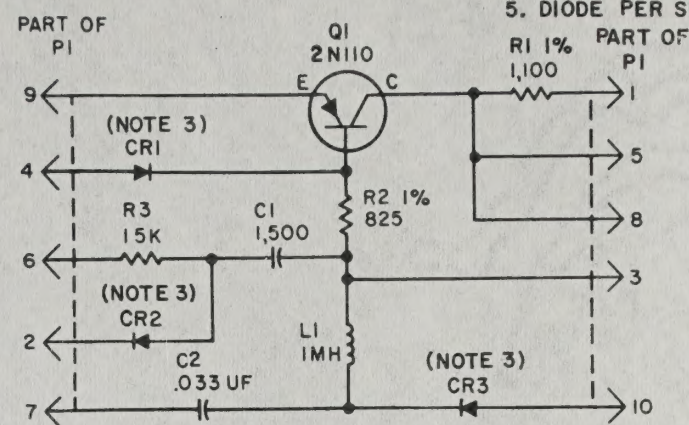
Figure 133. Receiver, timing diagram.

NOTES:

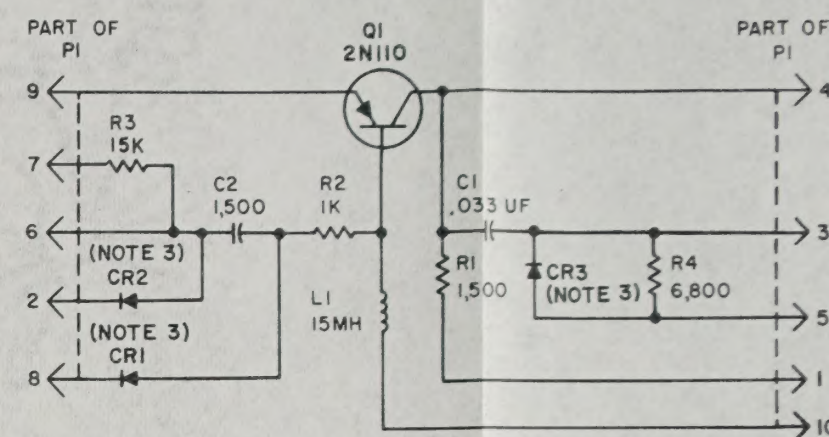
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN UUF.
2. UNLESS OTHERWISE INDICATED, RESISTORS ARE $\pm 5\%$ TOLERANCE.
3. DIODE PER SM-B-181088.
4. DIODE PER SM-B-181094.
5. DIODE PER SM-B-181092.



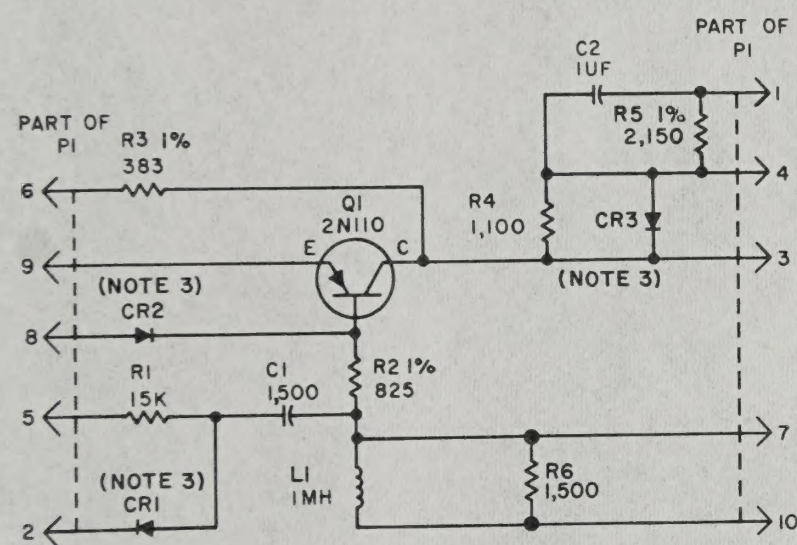
A PACKAGE



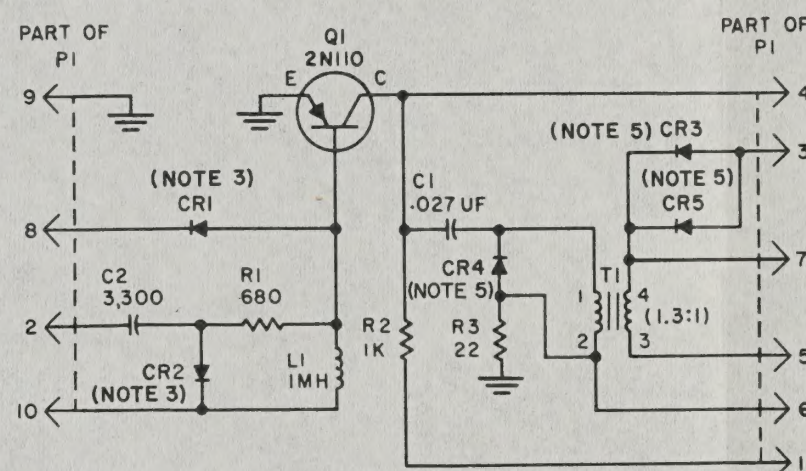
B PACKAGE



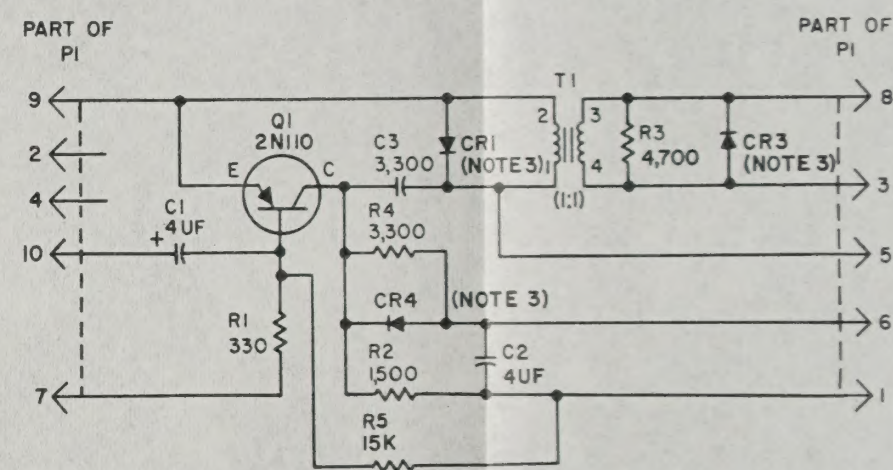
C PACKAGE



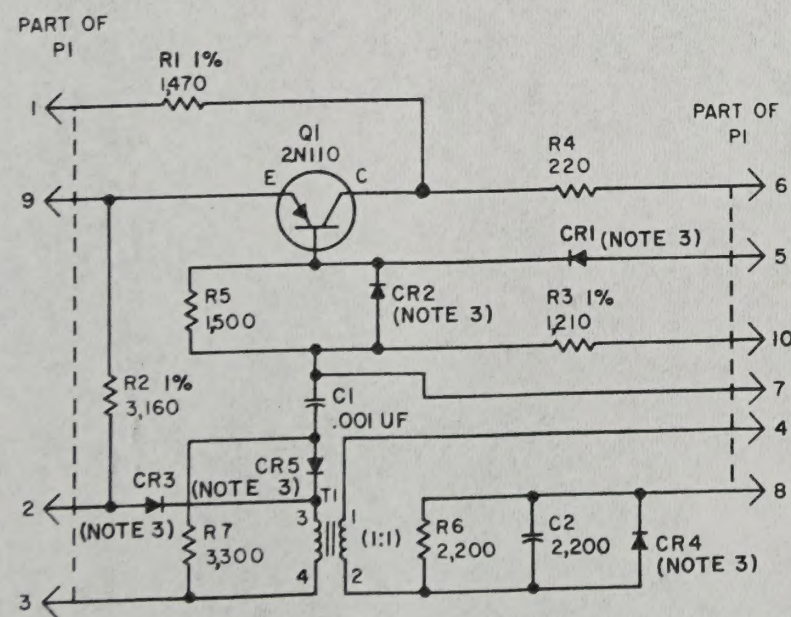
D PACKAGE



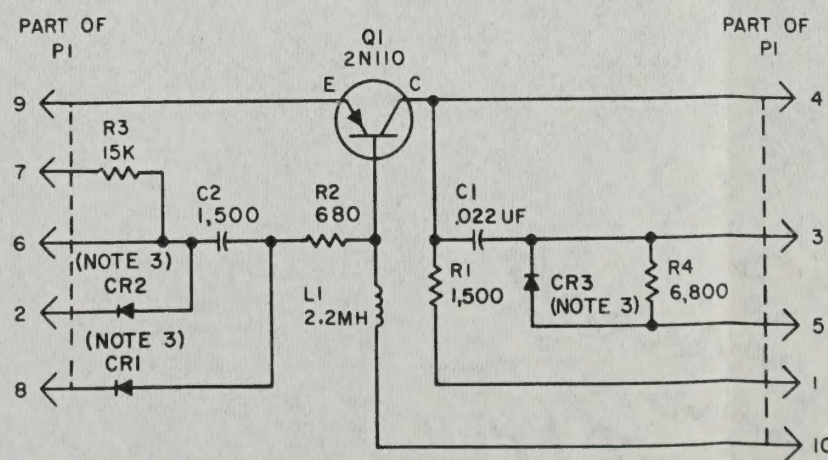
E PACKAGE



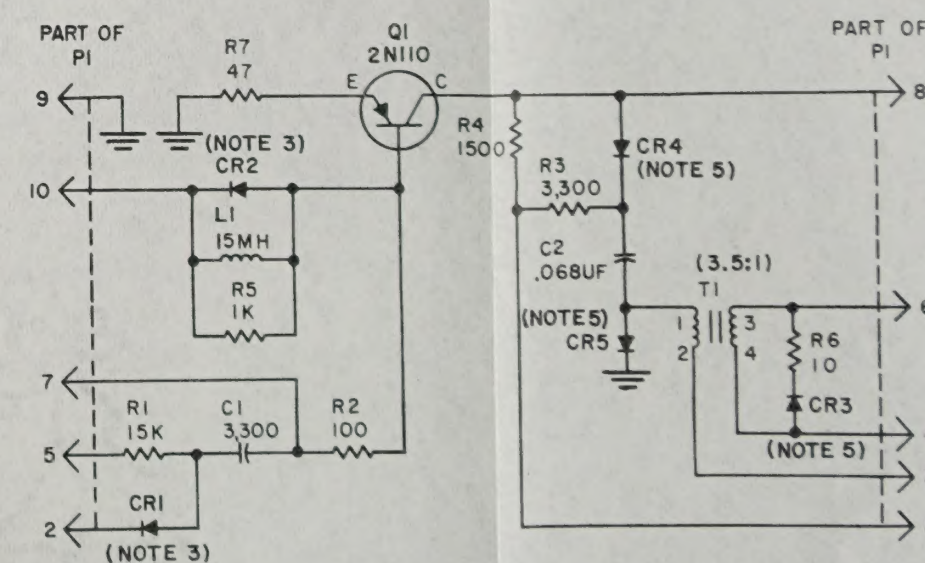
J PACKAGE



K PACKAGE



L PACKAGE



M PACKAGE

Figure 133. Package schematics.

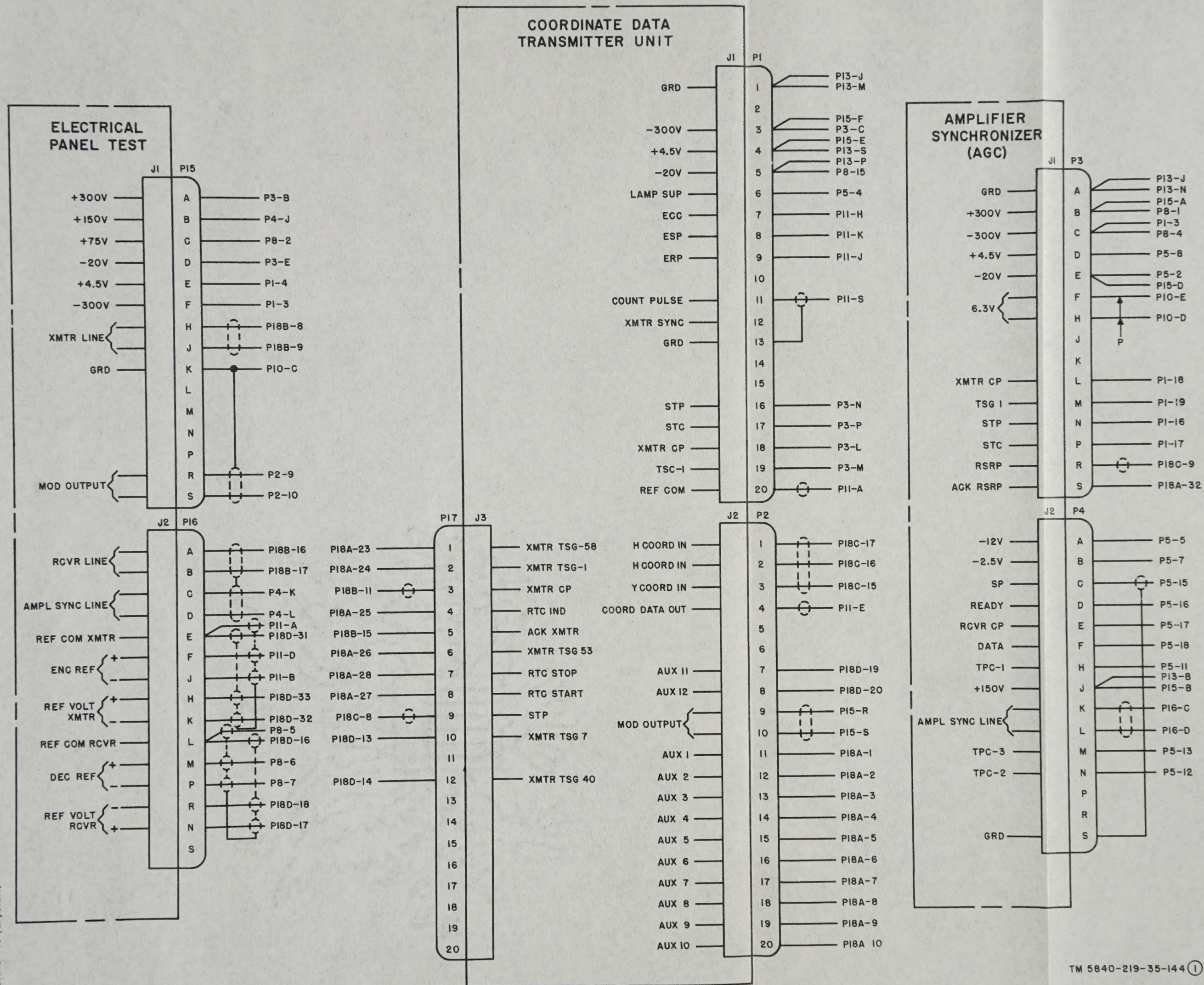


Figure 162. Coordinate data set AN/TSQ-36, interconnecting schematic.

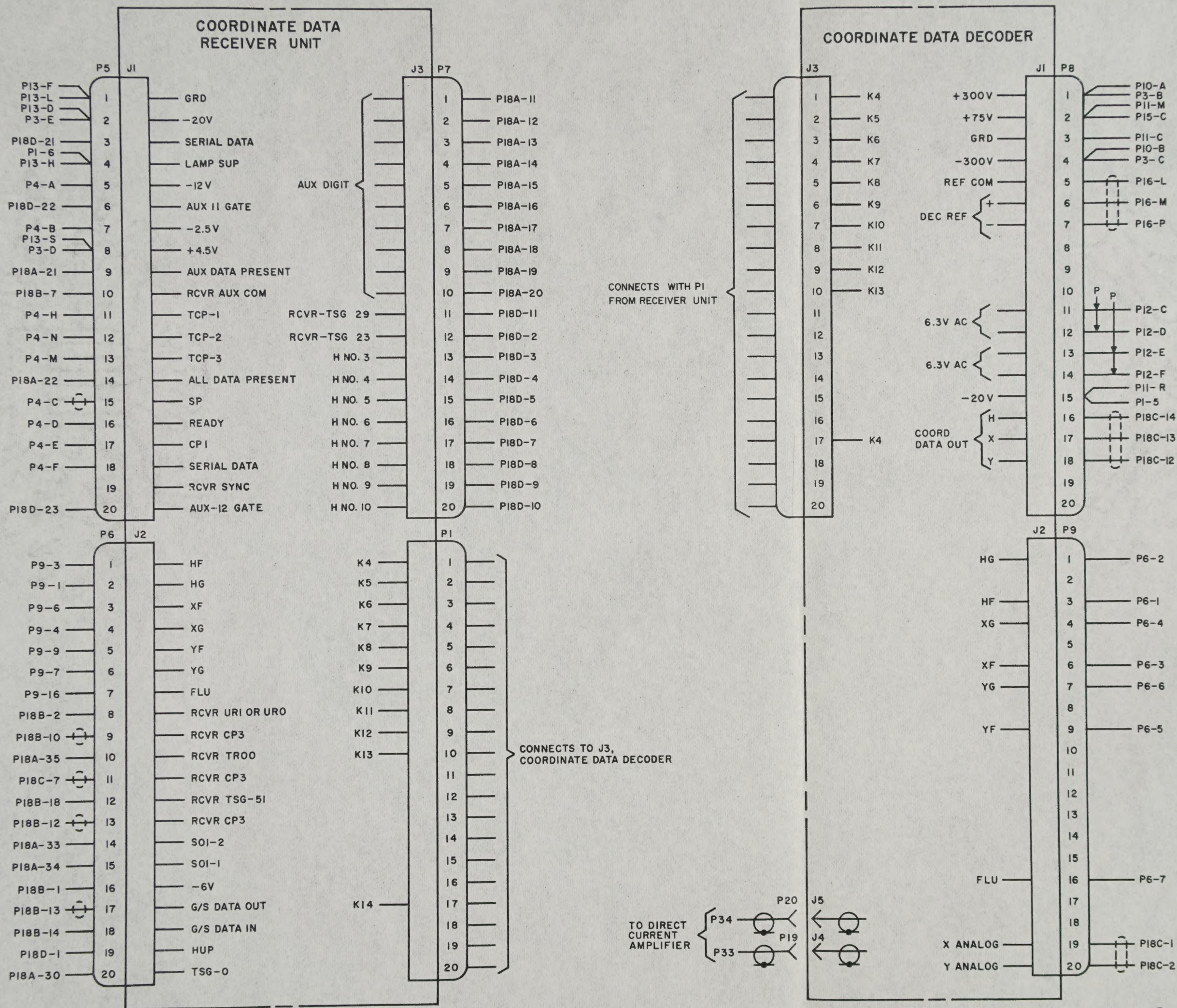
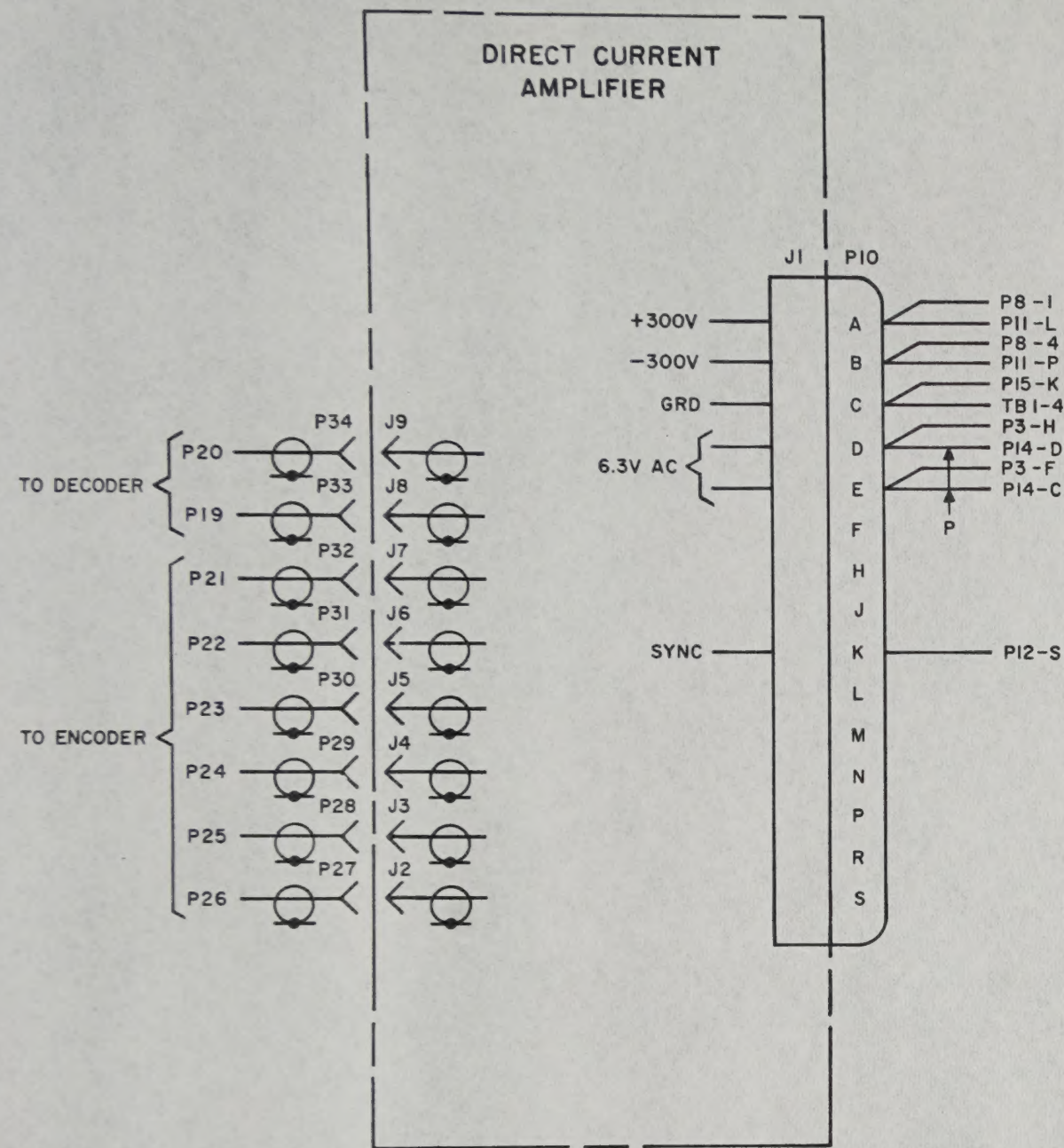
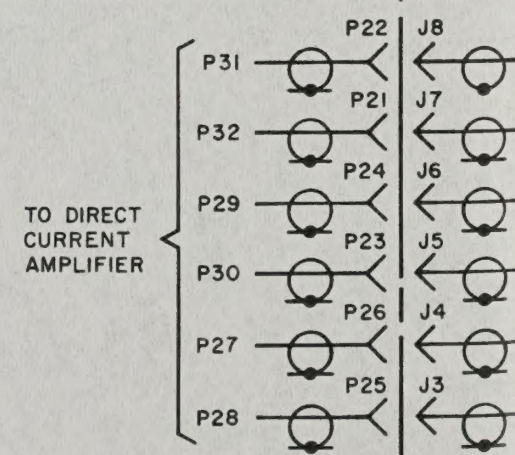
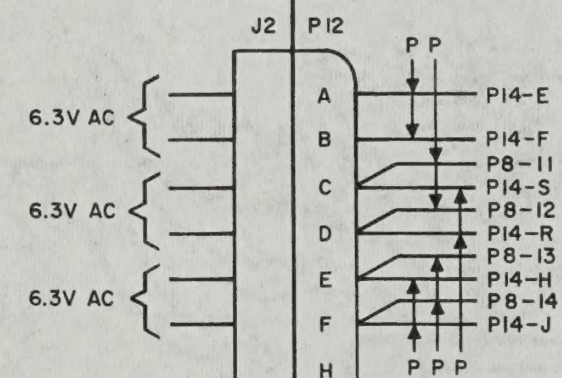
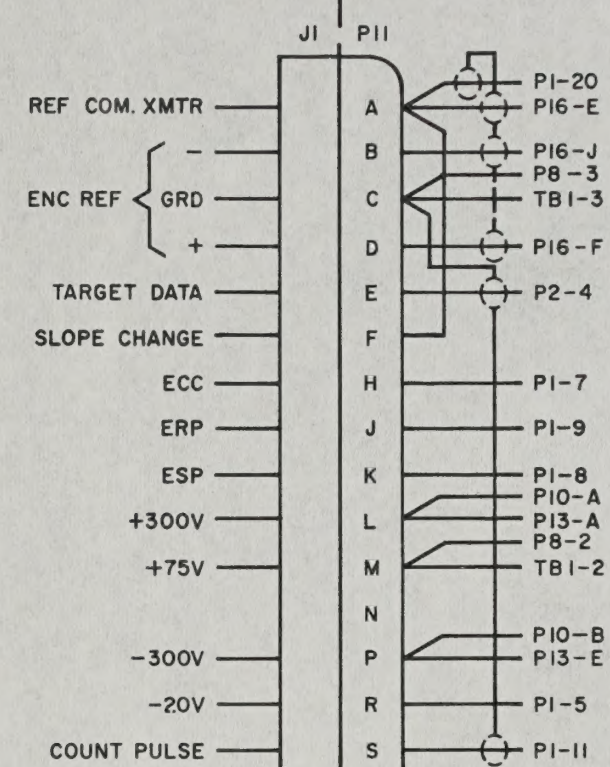


Figure 162—Continued.



COORDINATE DATA ENCODER



POWER SUPPLY (60 $\sim$ LOW VOLTAGE AND FIL)

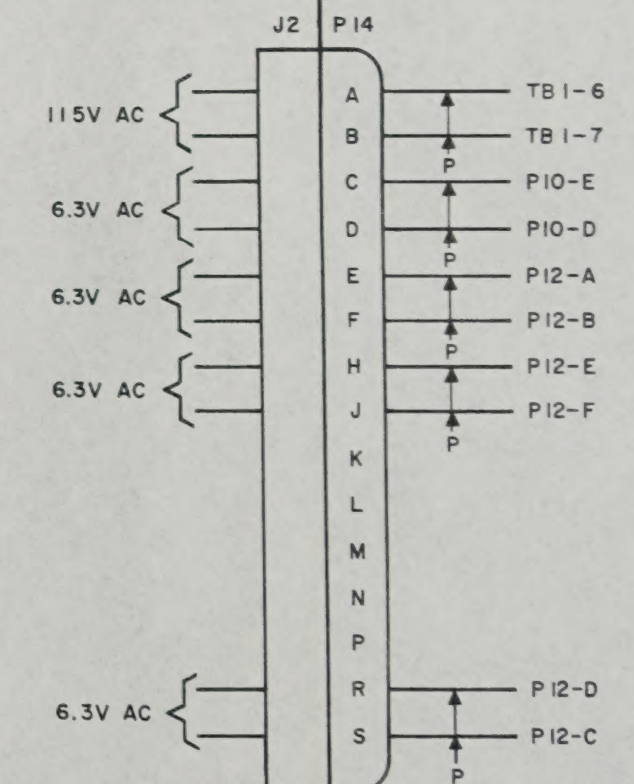
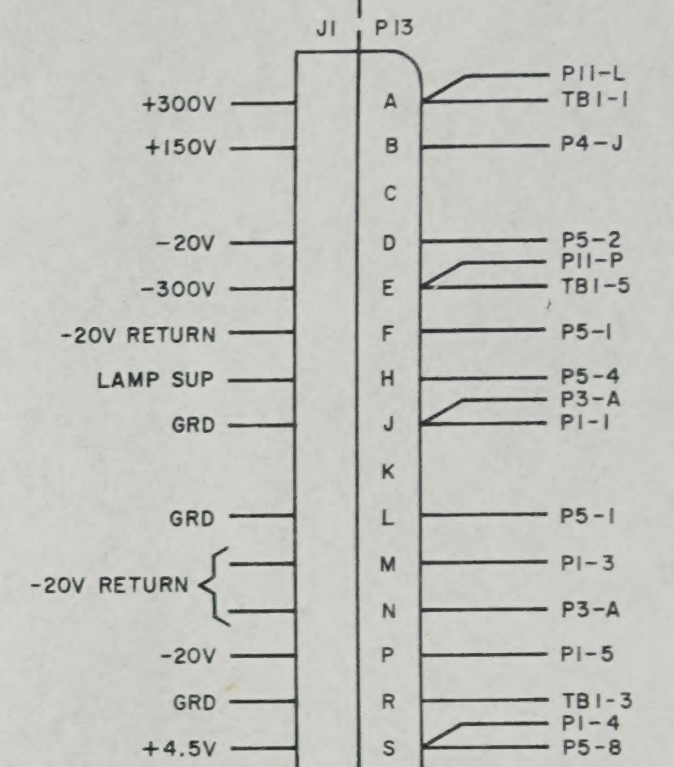


Figure 162—Continued.

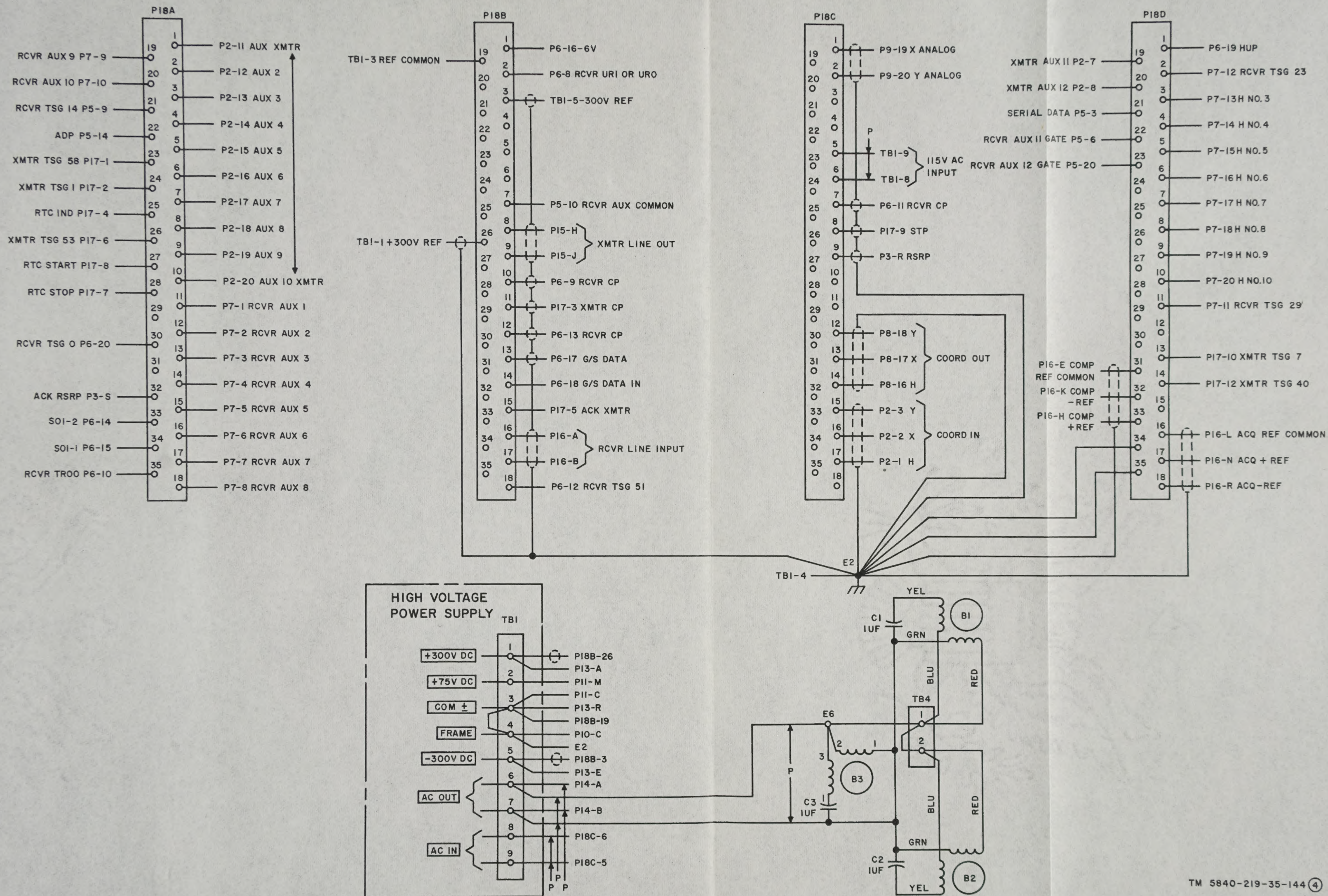


Figure 162—Continued.

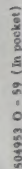


Figure 163. Coordinate data transmitter unit T-721/TSQ-36, schematic.

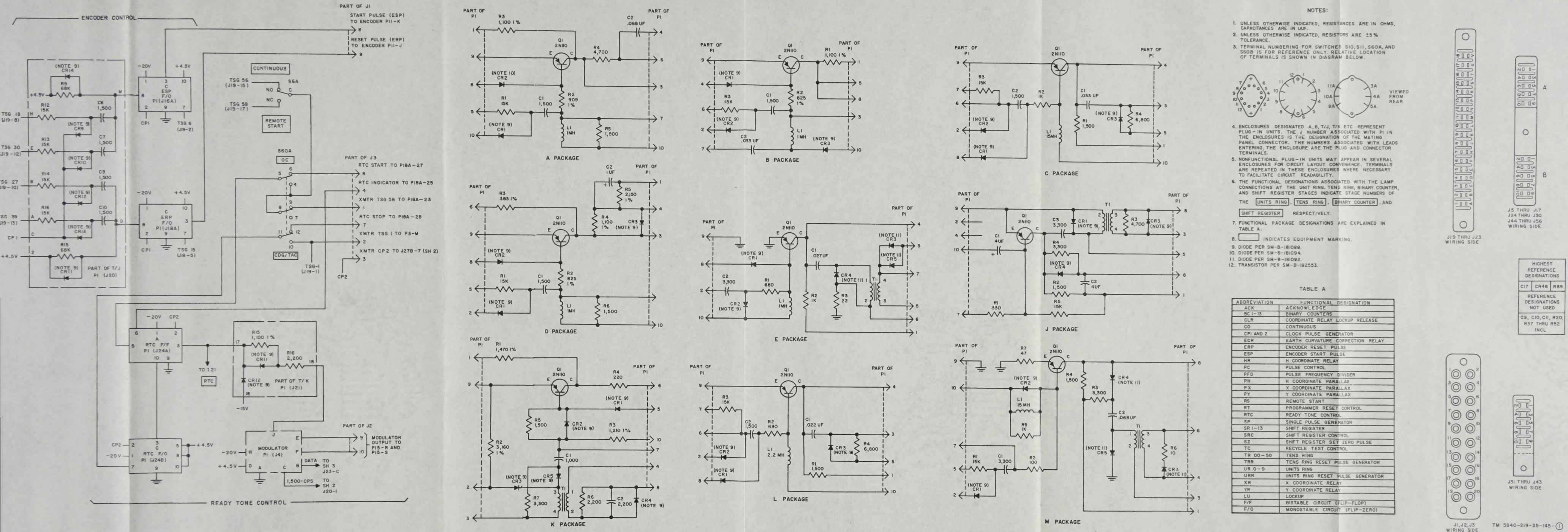


Figure 163. Coordinate data transmitter unit T-721/TSQ-36, schematic.

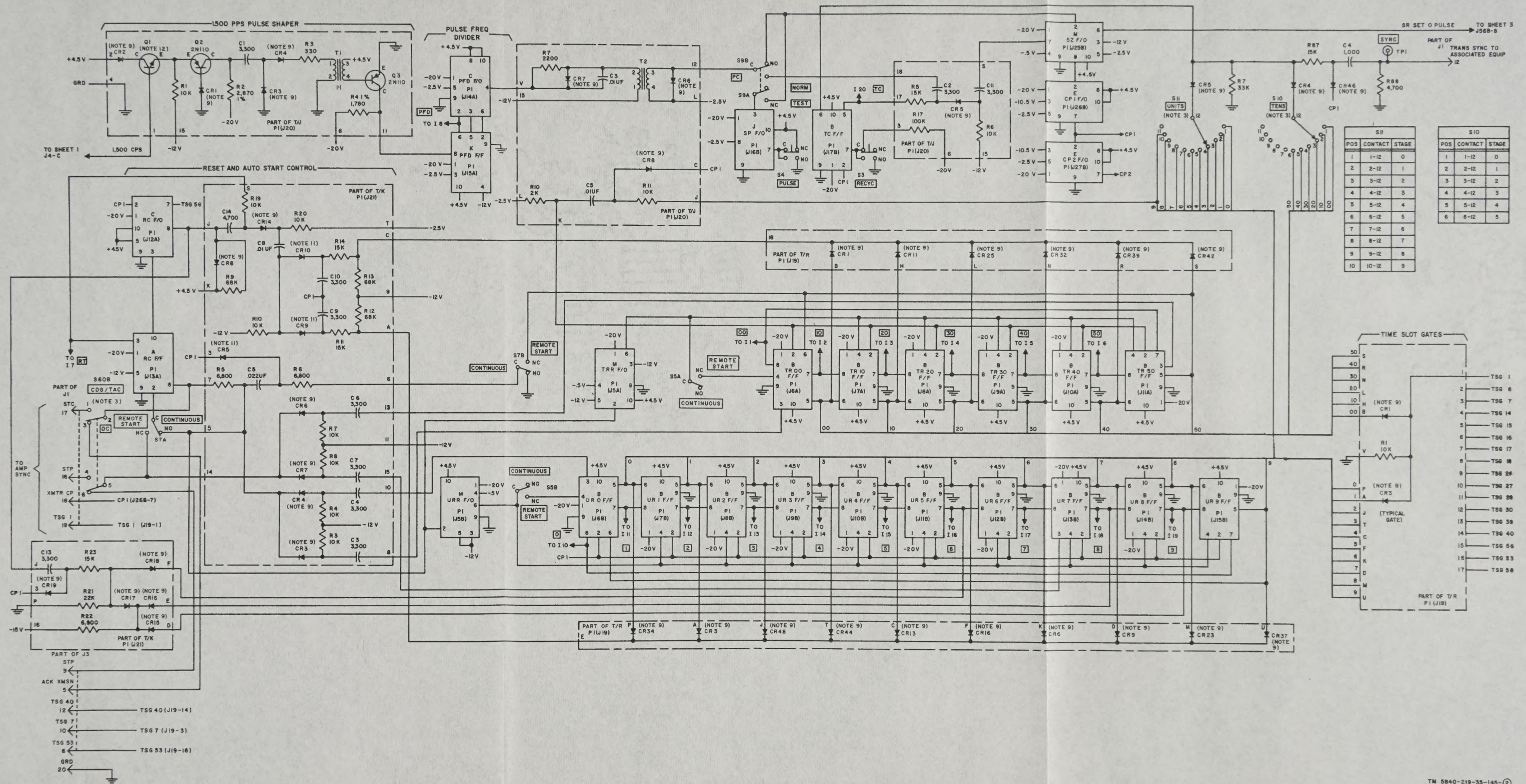


Figure 163-Continued.

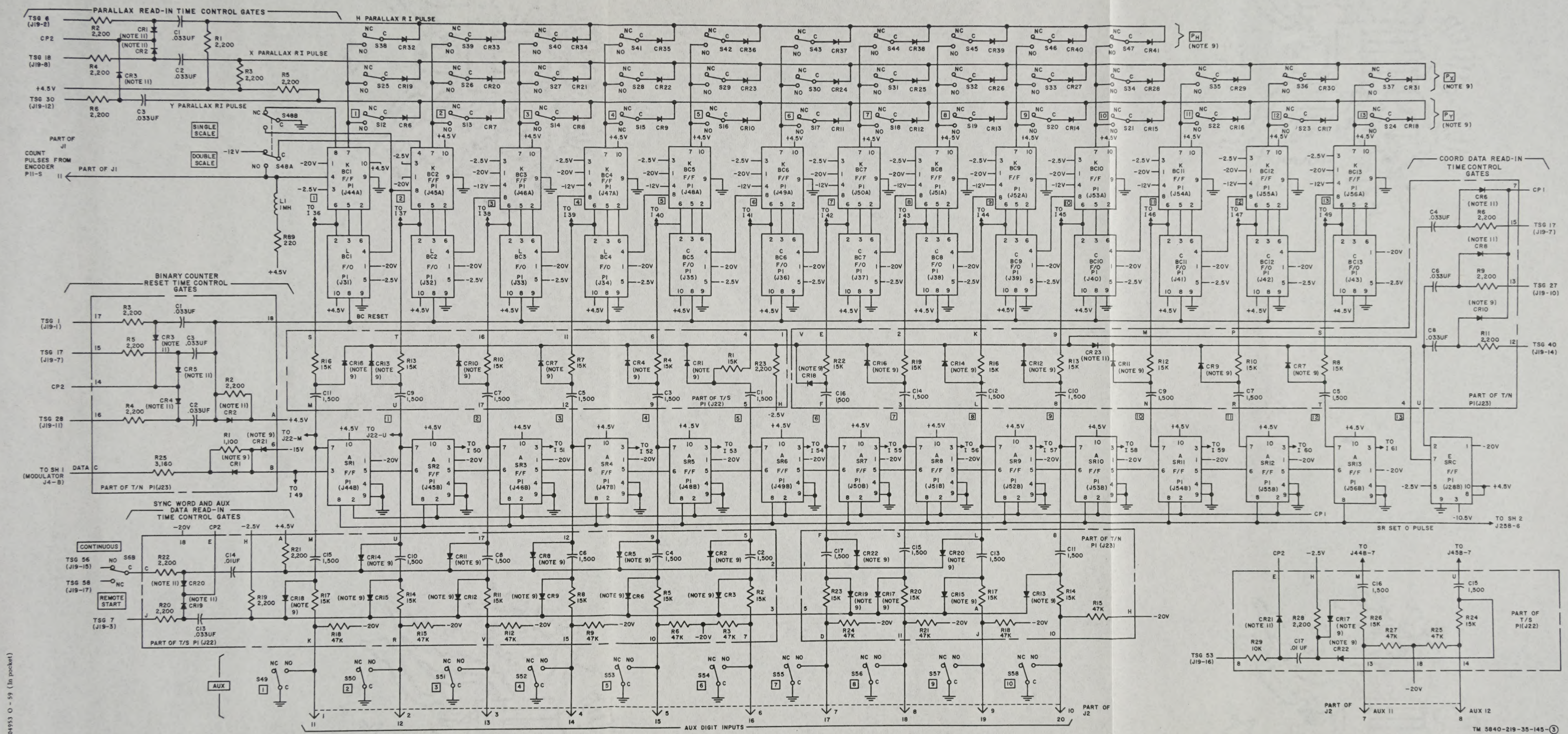


Figure 163—Continued.

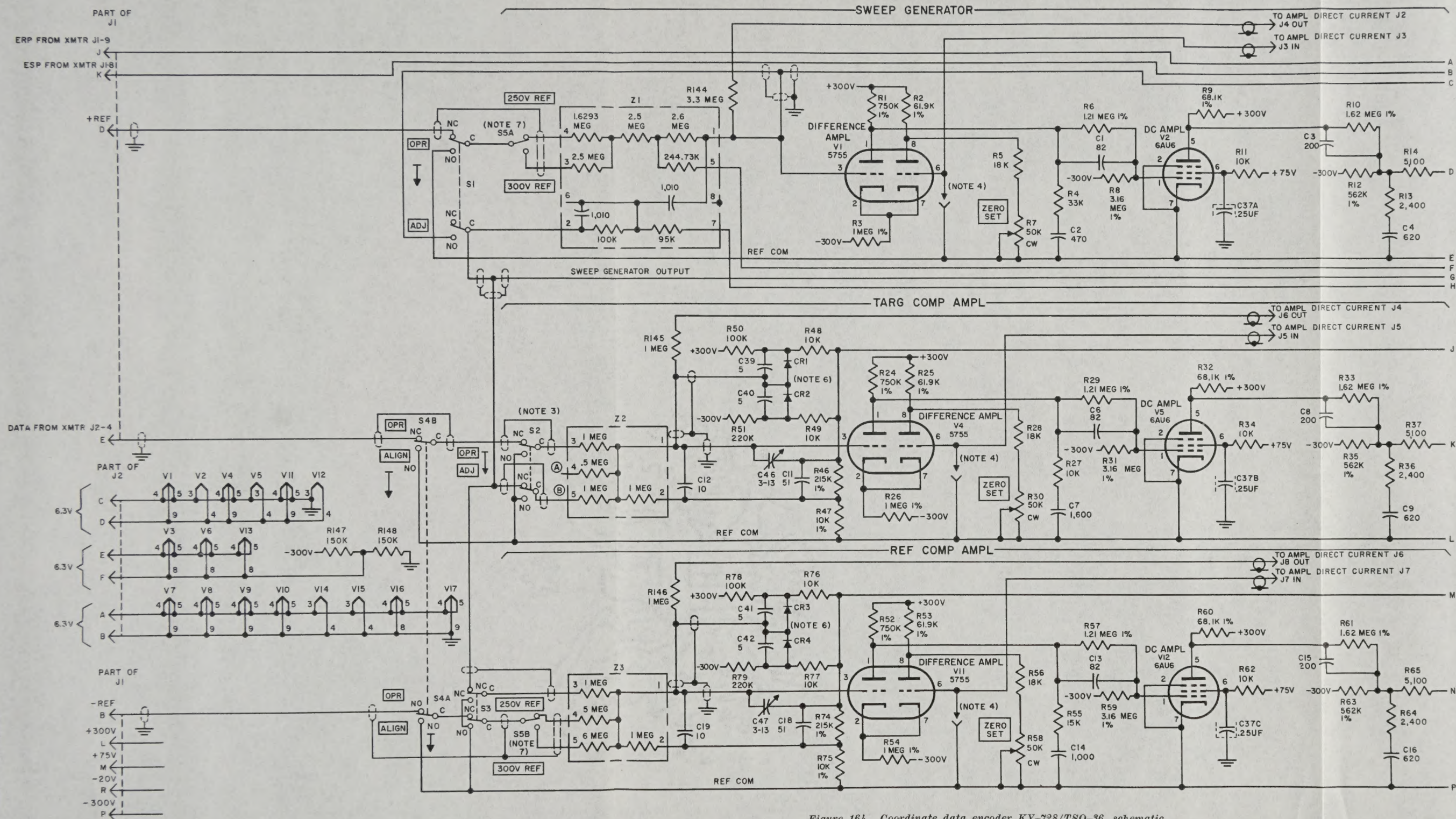


Figure 164. Coordinate data encoder KY-728/TSQ-36, schematic.

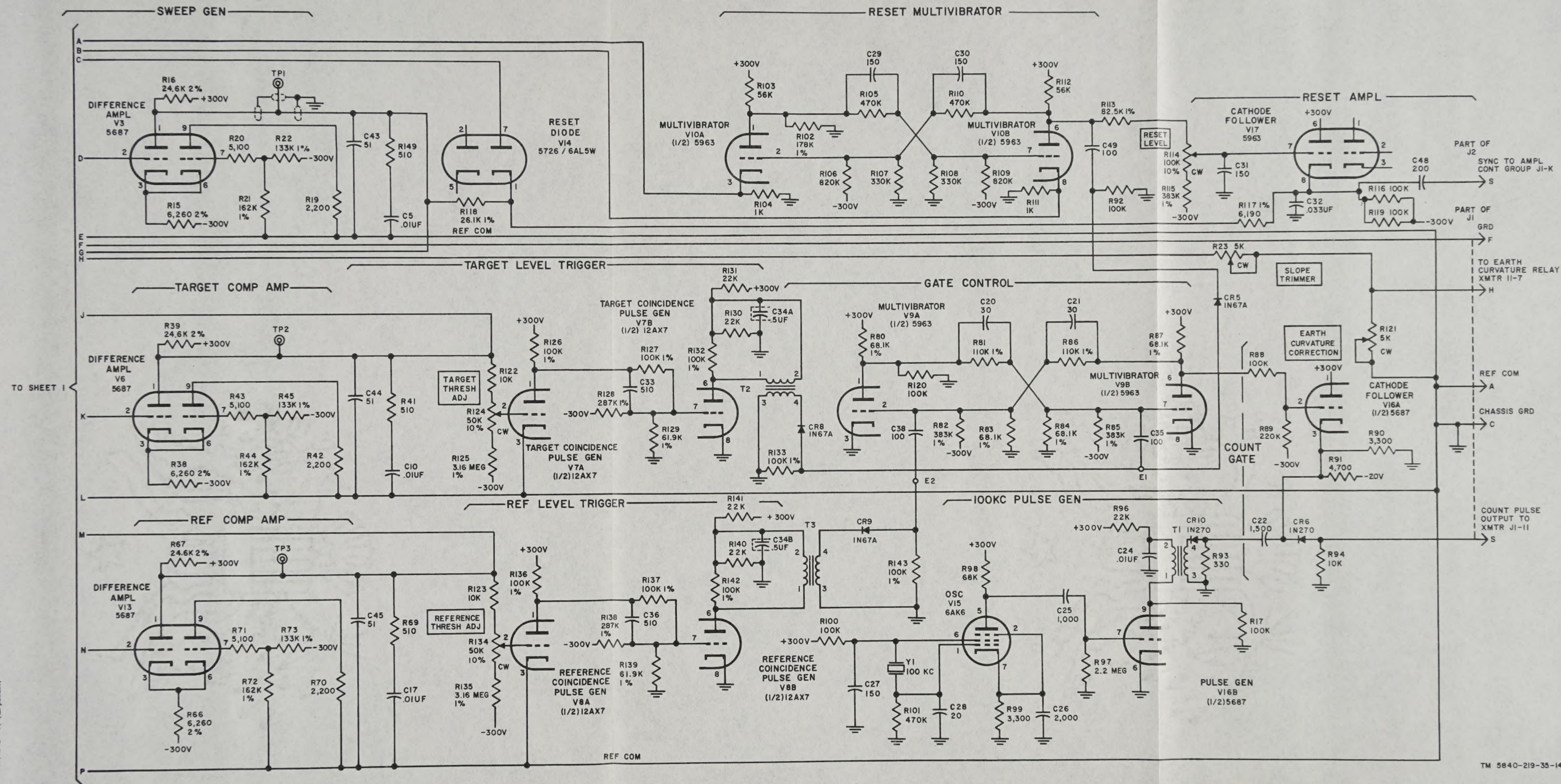
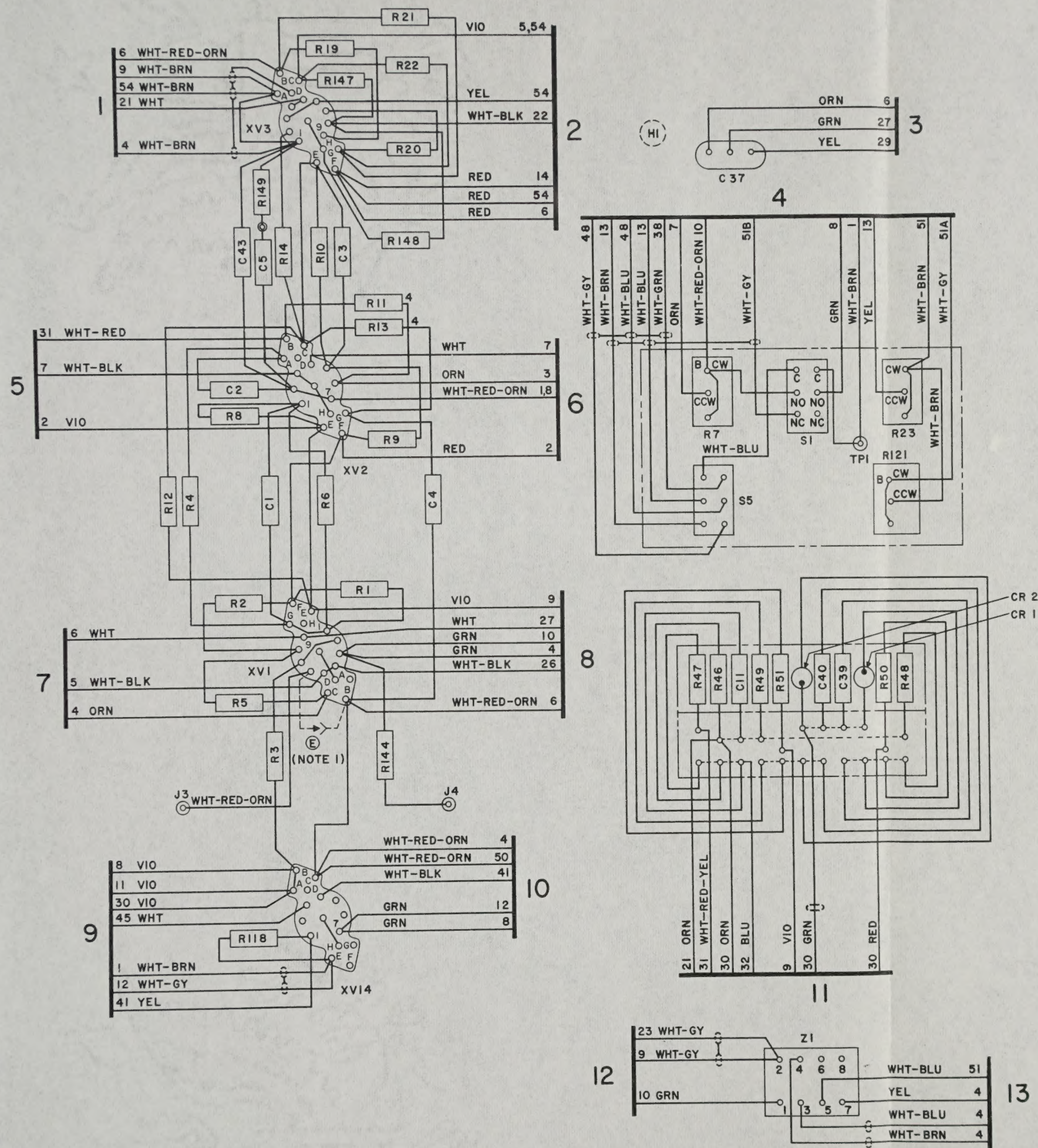


Figure 164—Continued.



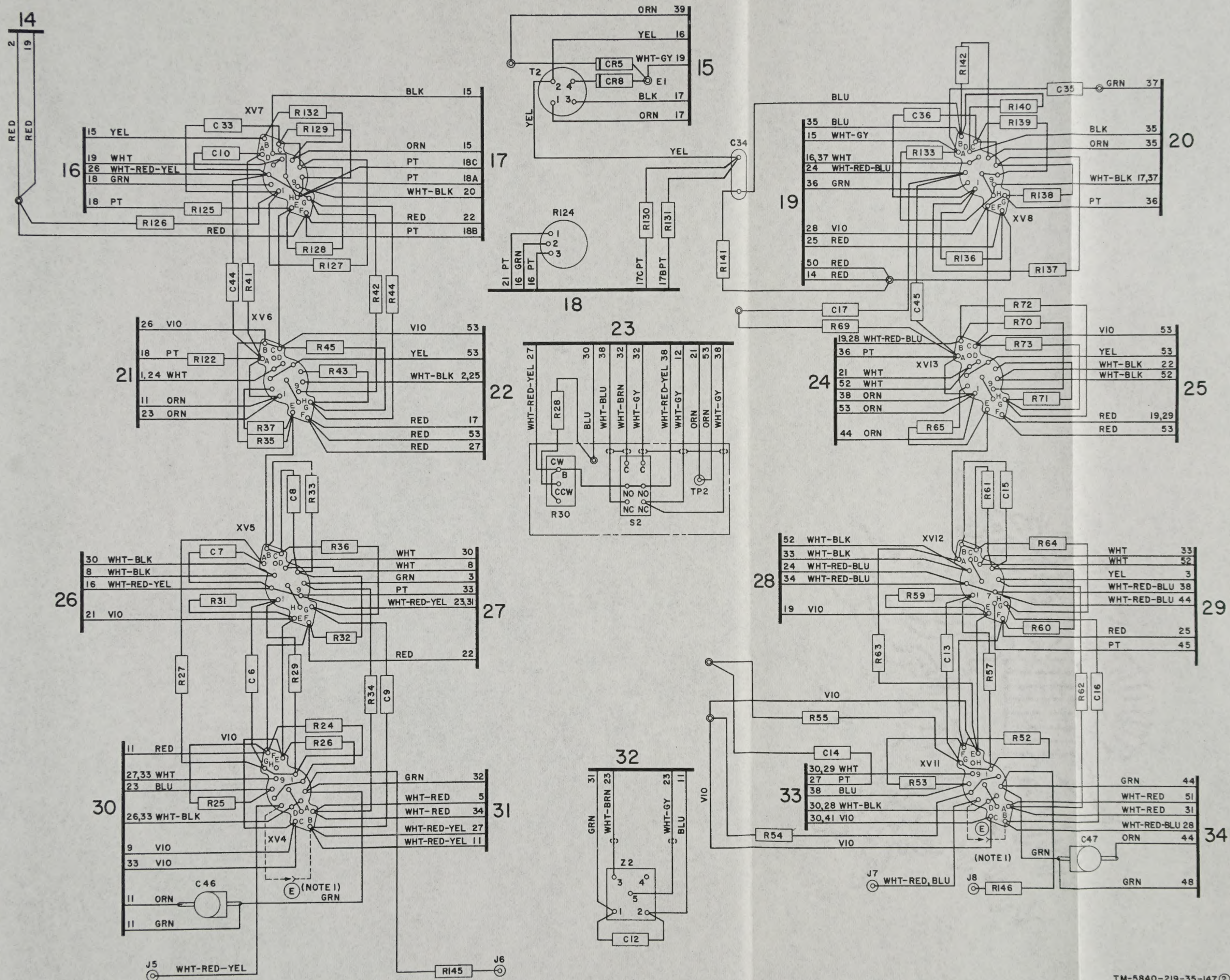


Figure 165—Continued.

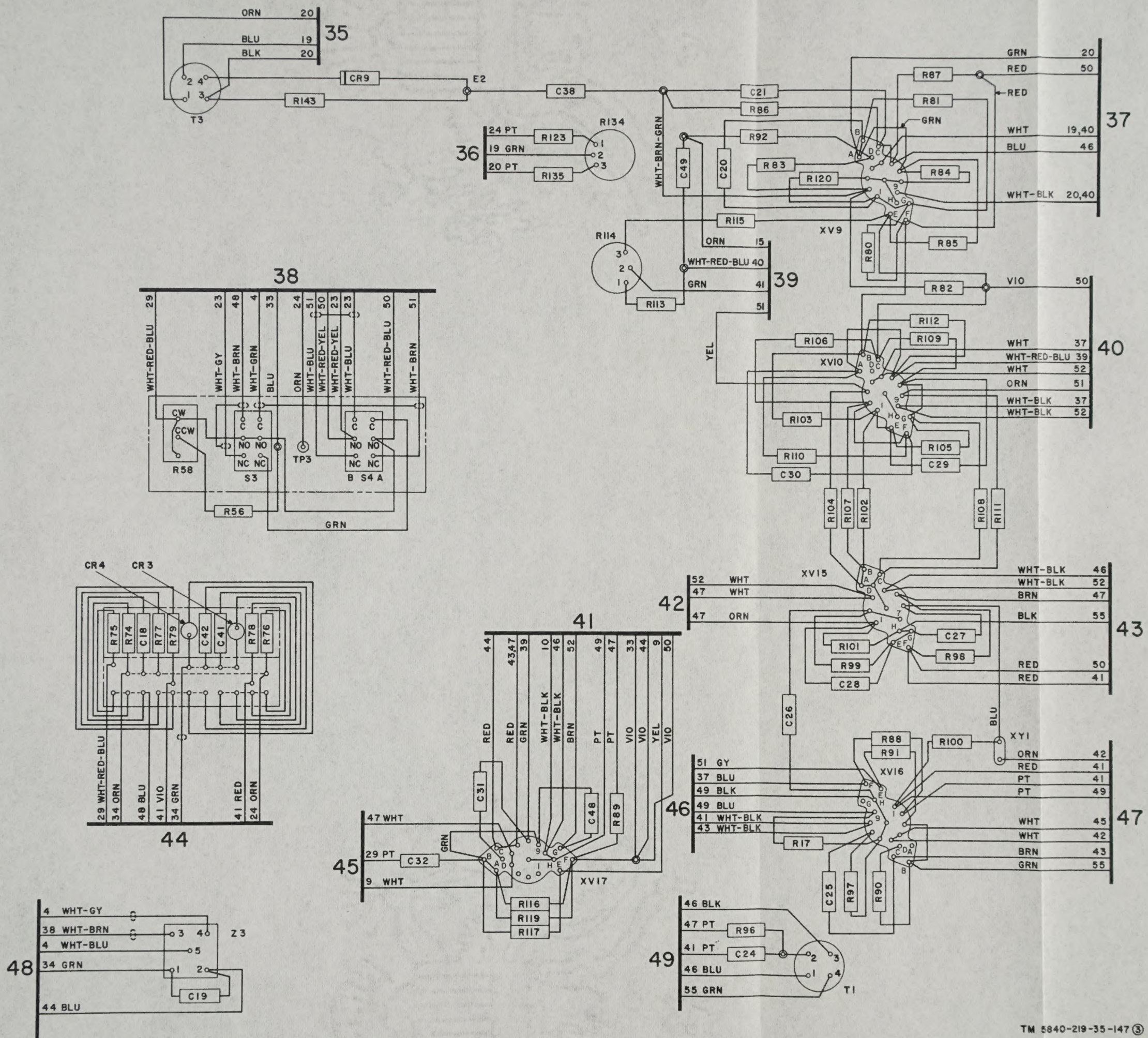


Figure 165—Continued.

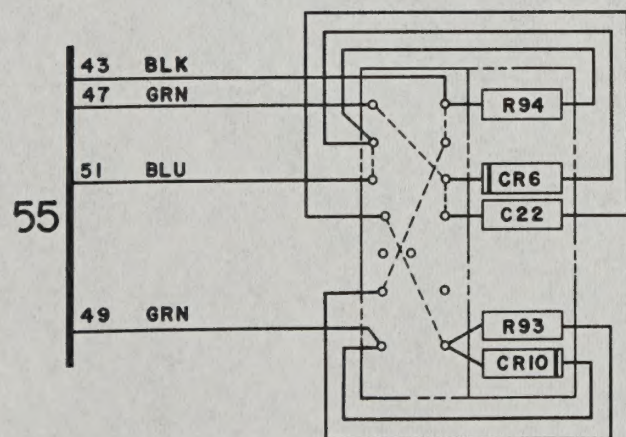
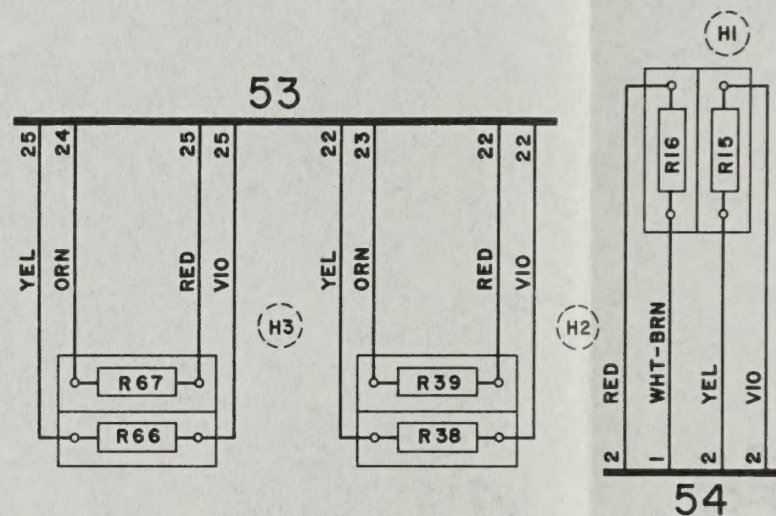
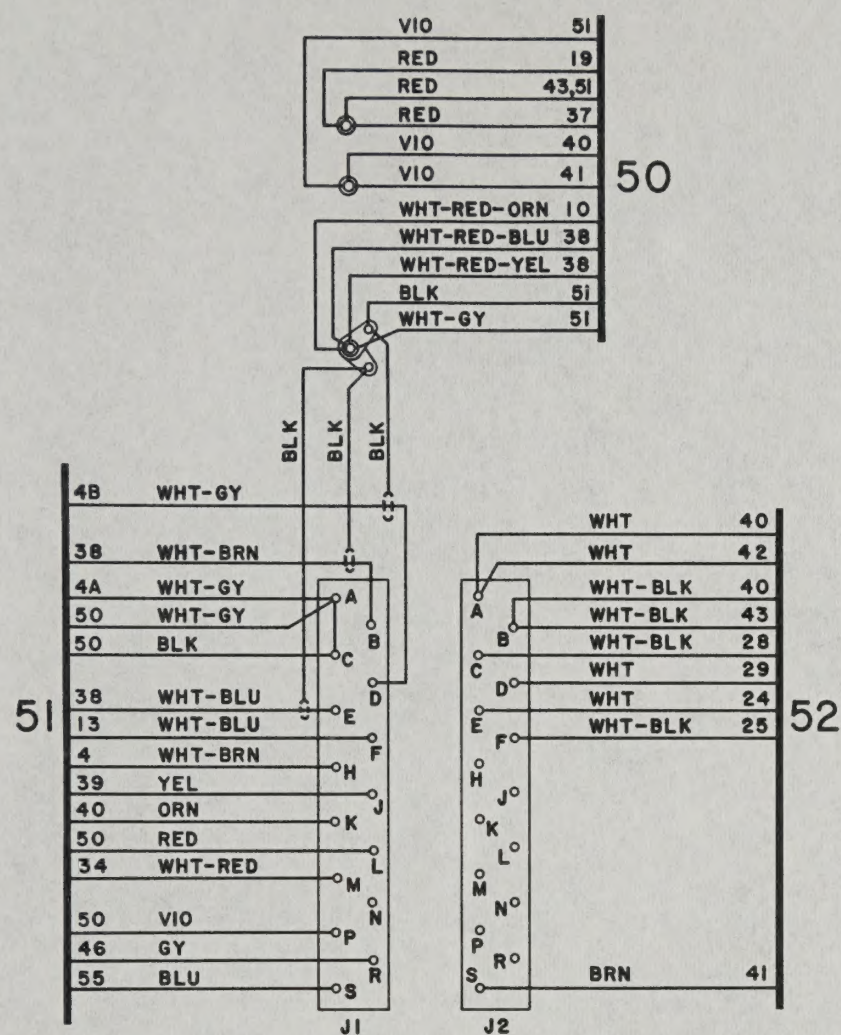


Figure 165—Continued.

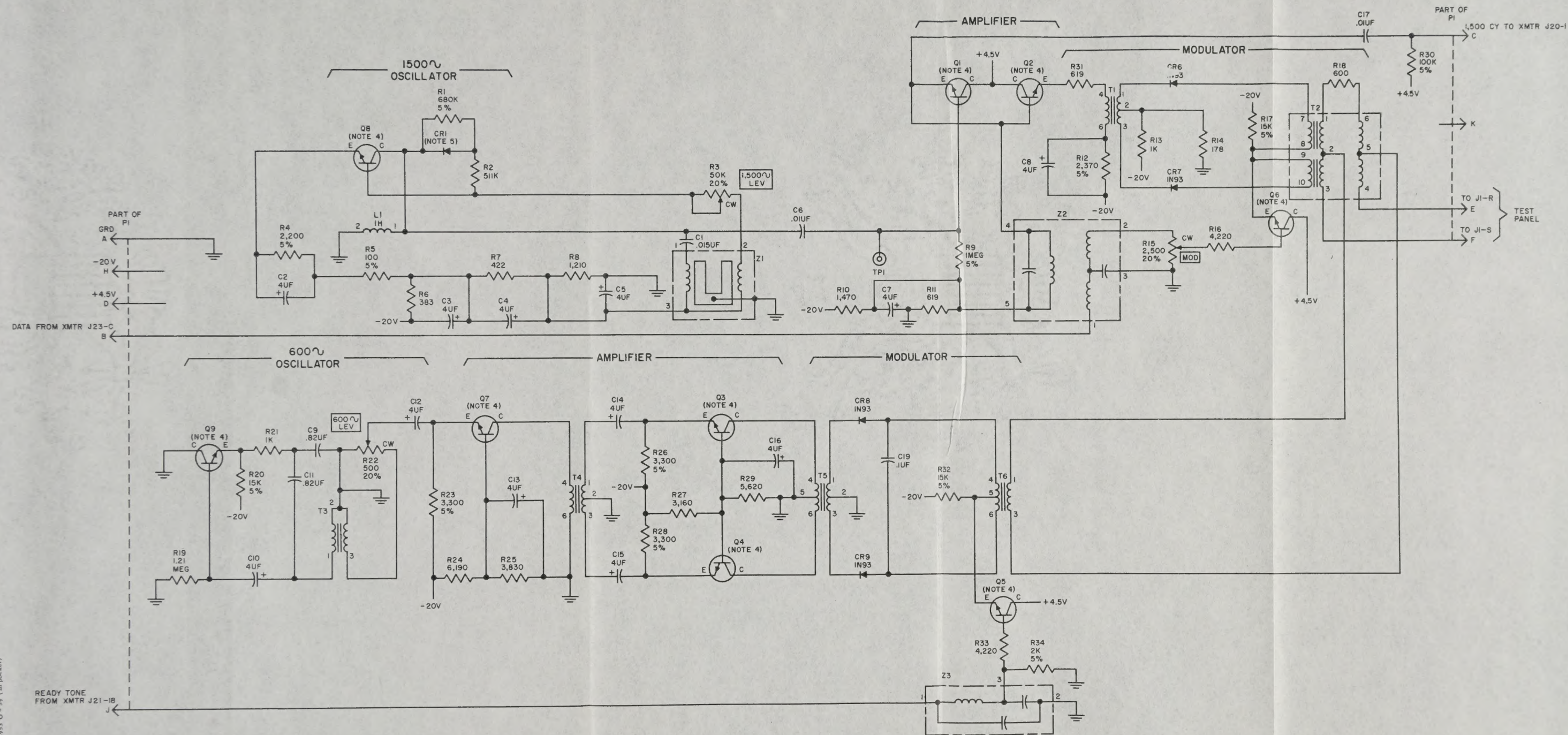
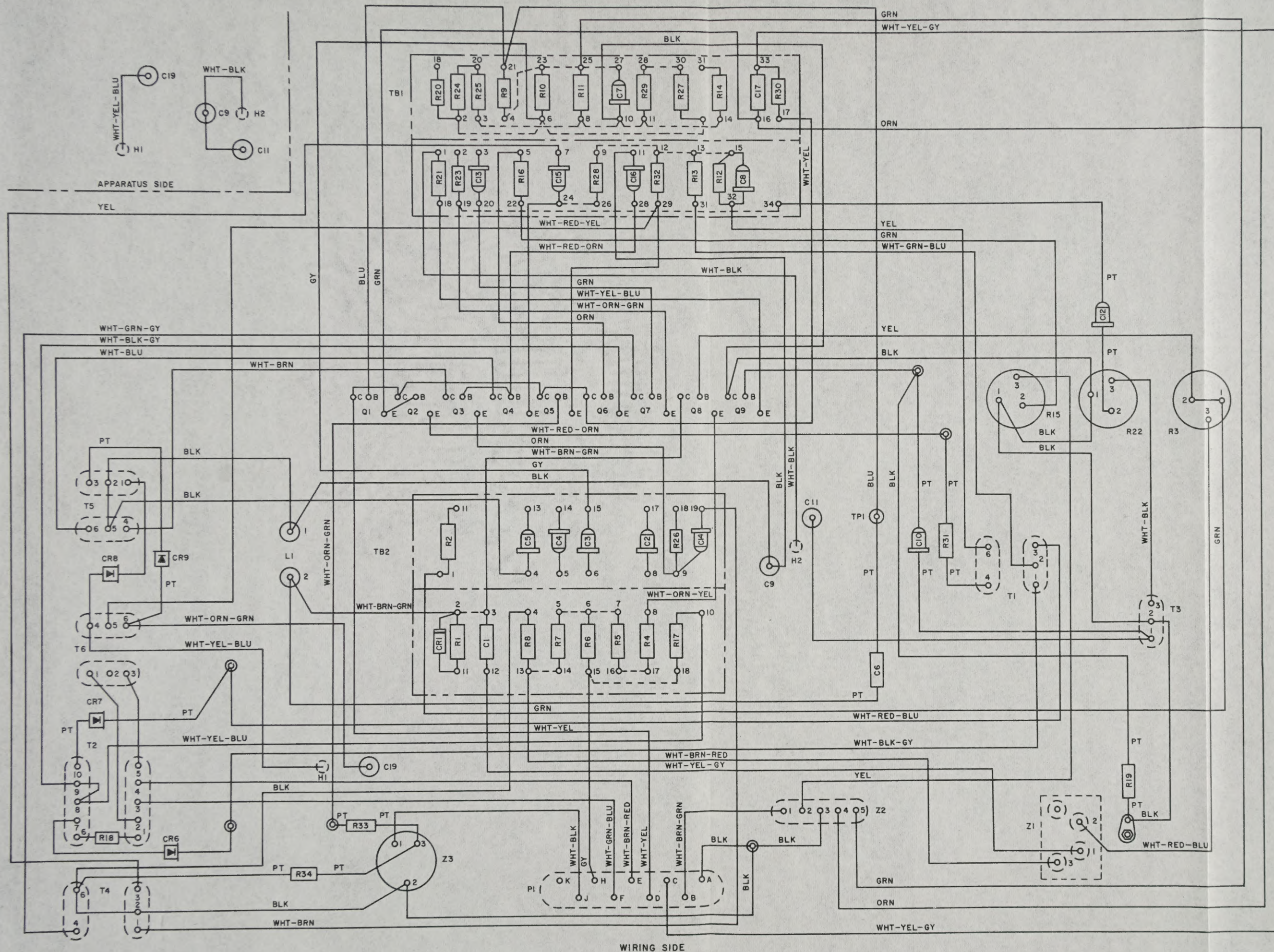


Figure 168. Coordinate data modulator MD-323A/G, schematic.



NOTE:
TERMINAL NUMBERS SHOWN ON APPARATUS
MOUNTING BOARDS ARE FOR REFERENCE ONLY.
LIKE NUMBERS ARE OPPOSITE ENDS OF SAME TERMINAL.

Figure 169. Coordinate data modulator MD-323A/G, wiring diagram.

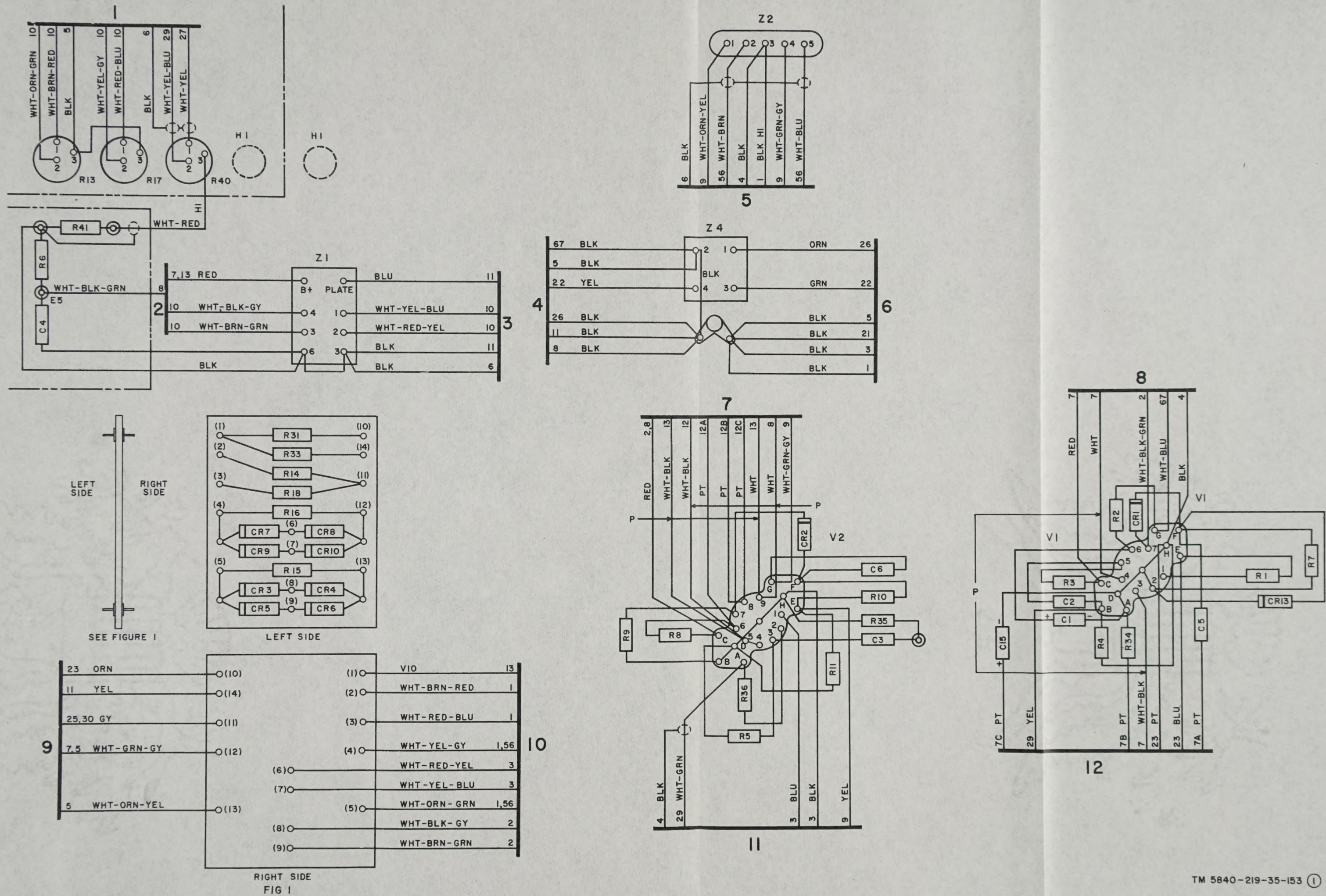


Figure 171. Amplifier-synchronizer unit AM-2126/TSQ-36, wiring diagram.

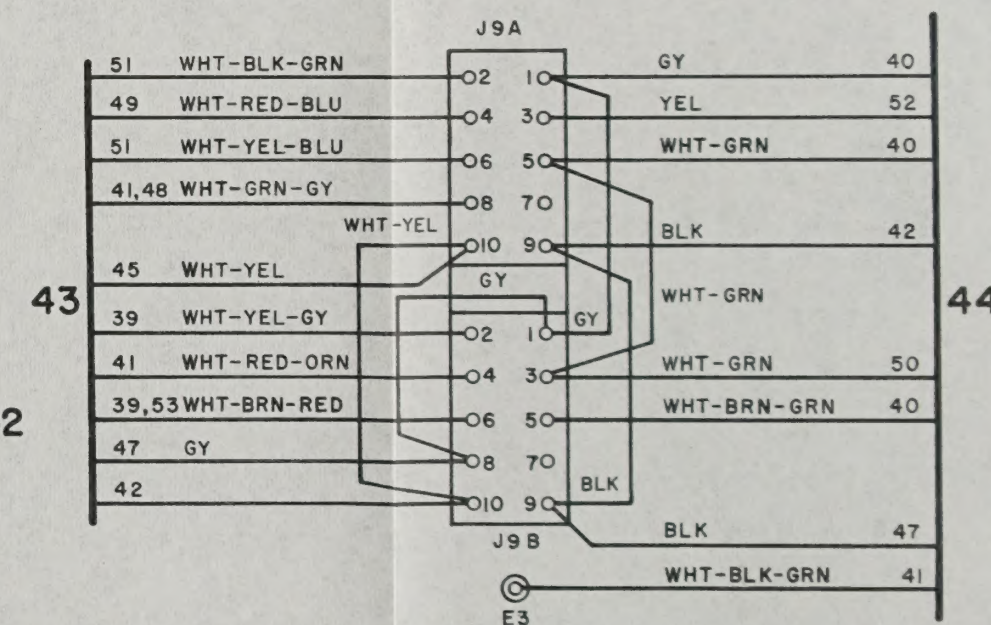
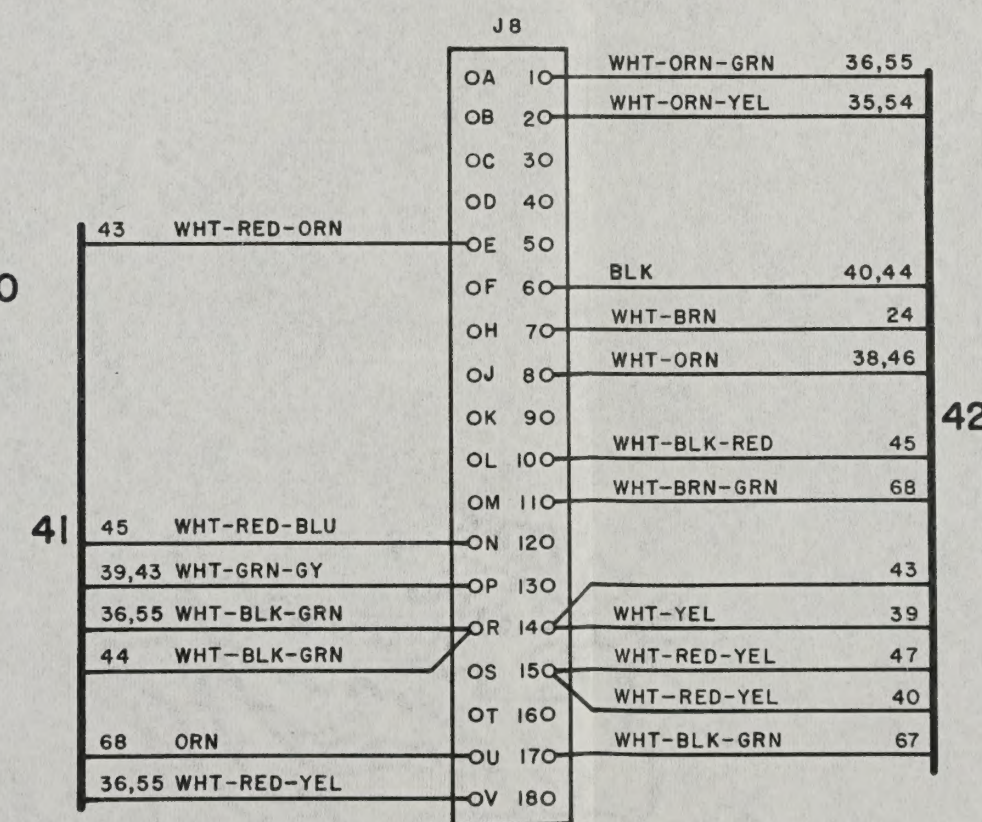
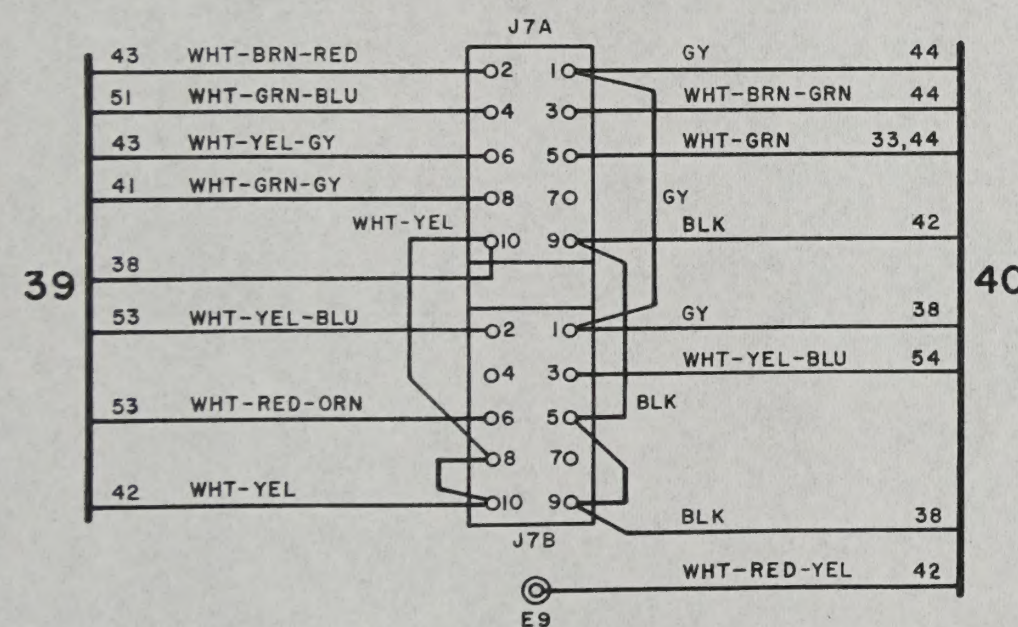
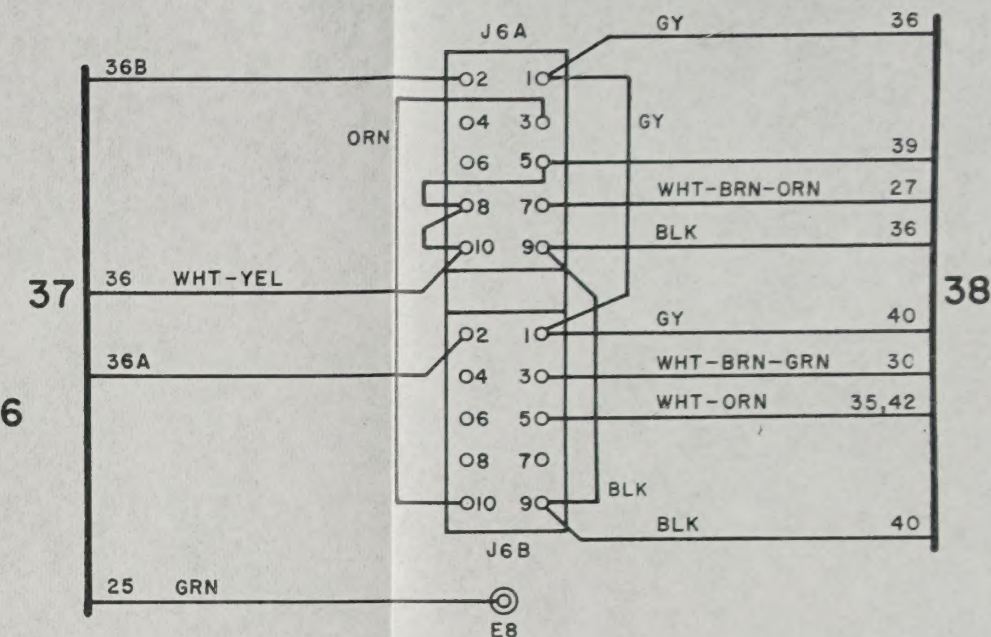
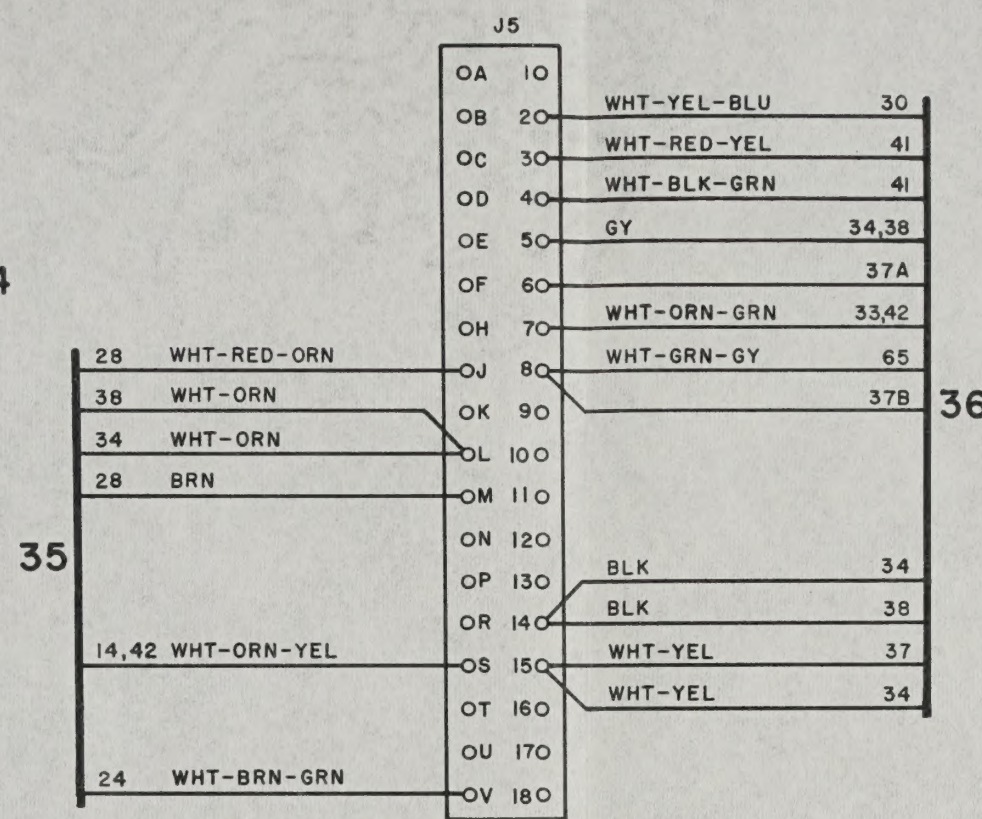
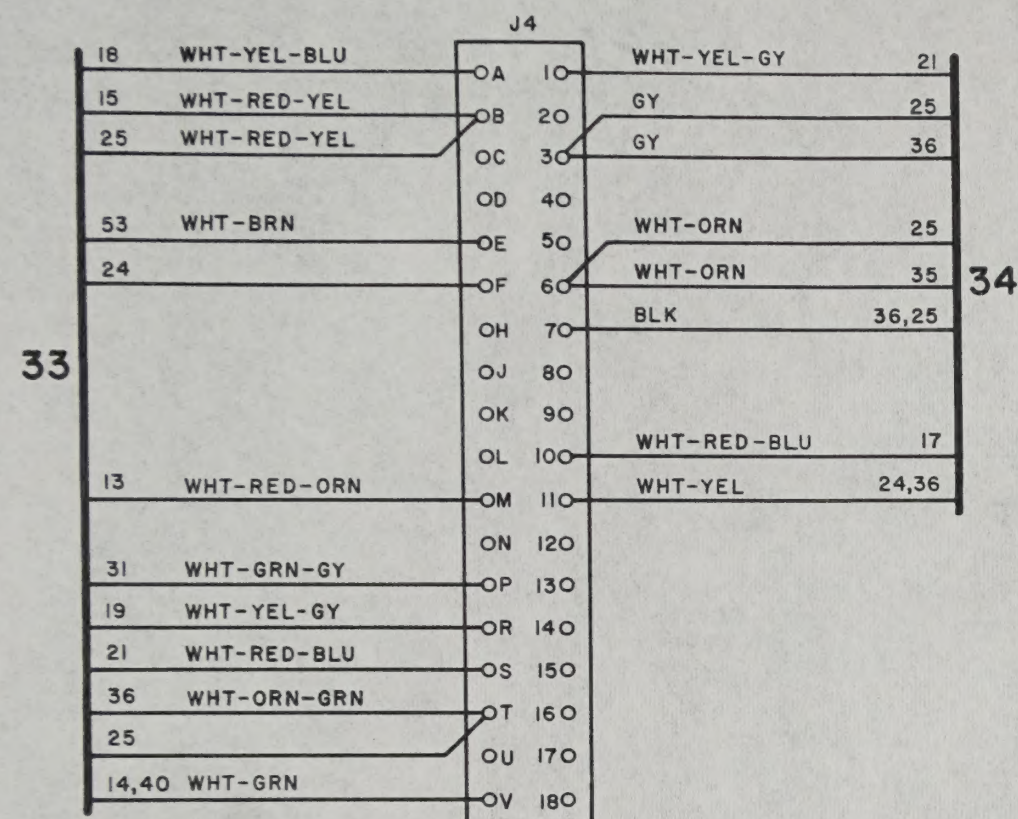
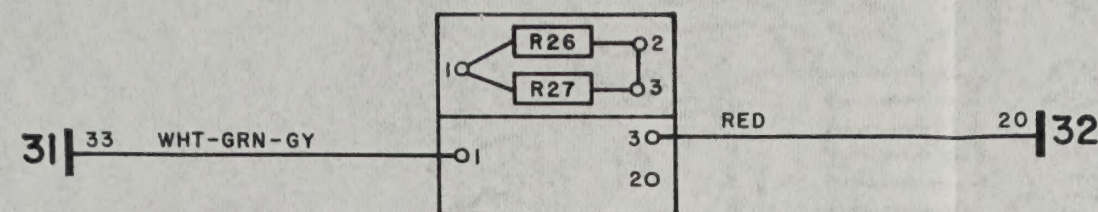
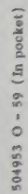


Figure 171—Continued.



TM 5840-219-35-153 (4)

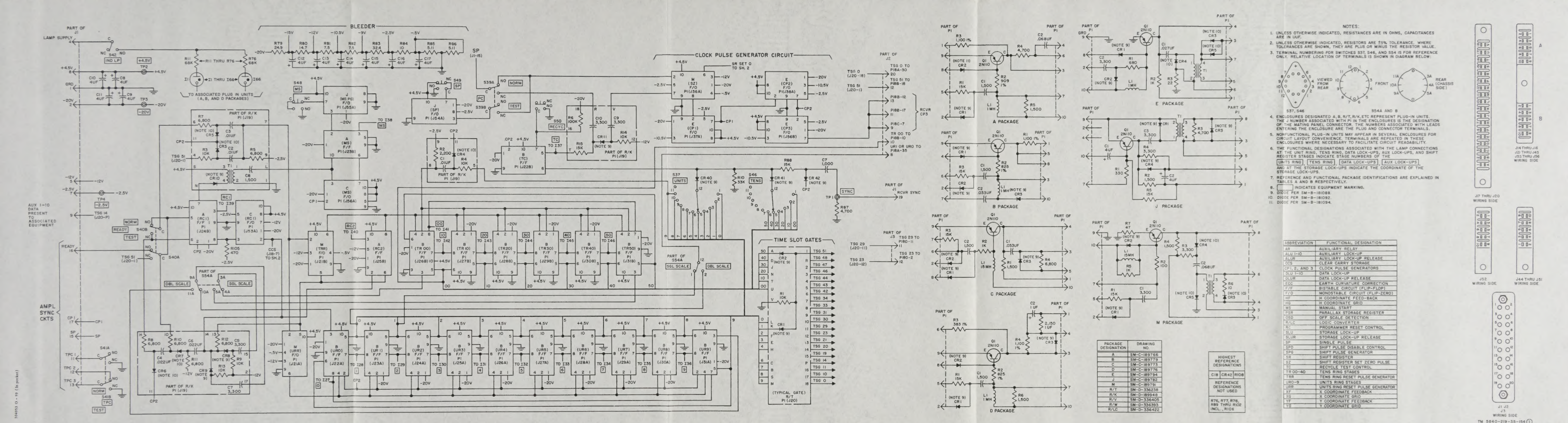


Figure 172. Coordinate data receiver unit R-930/TSQ-36, schematic.

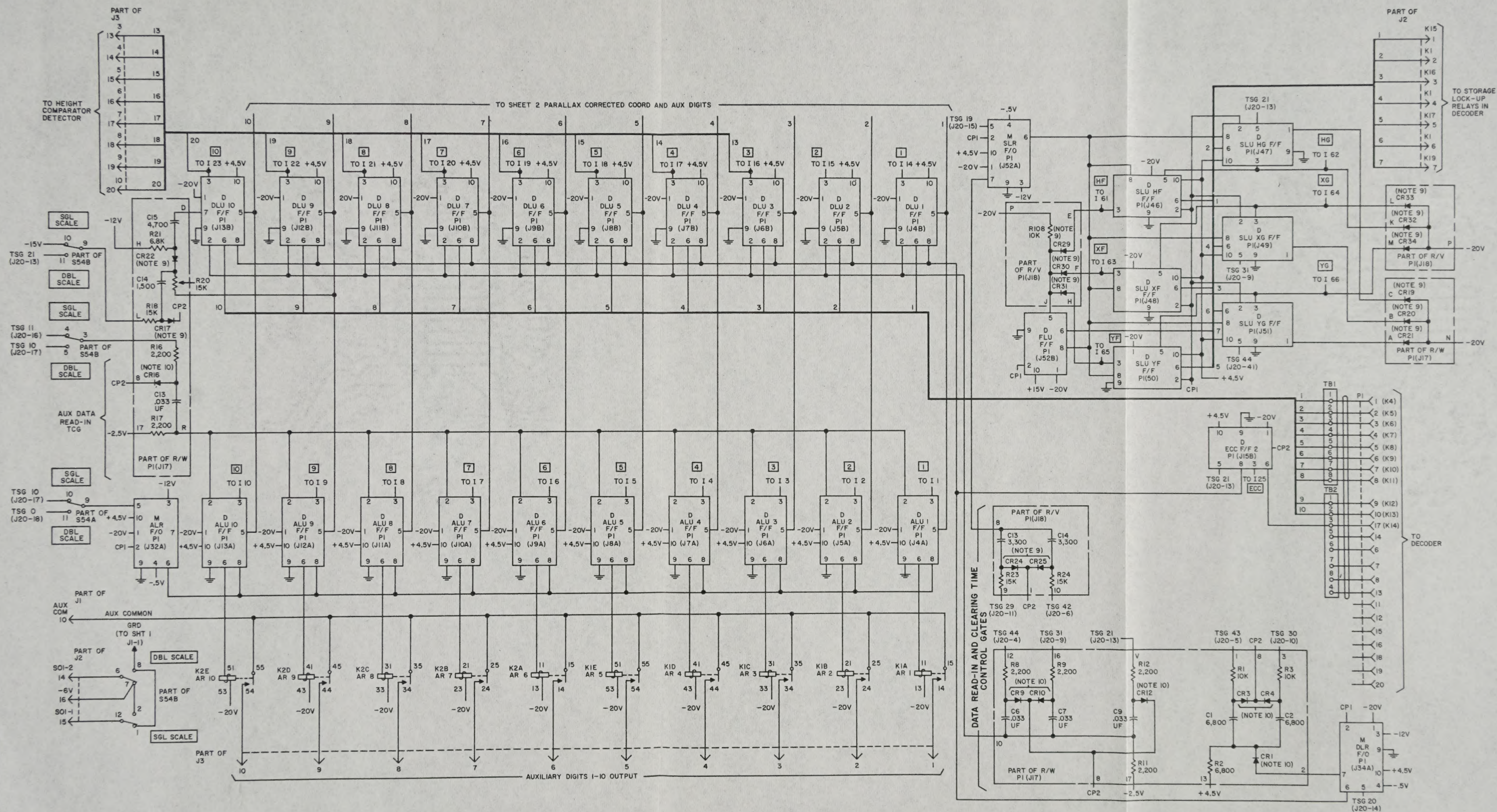


Figure 172-Continued.

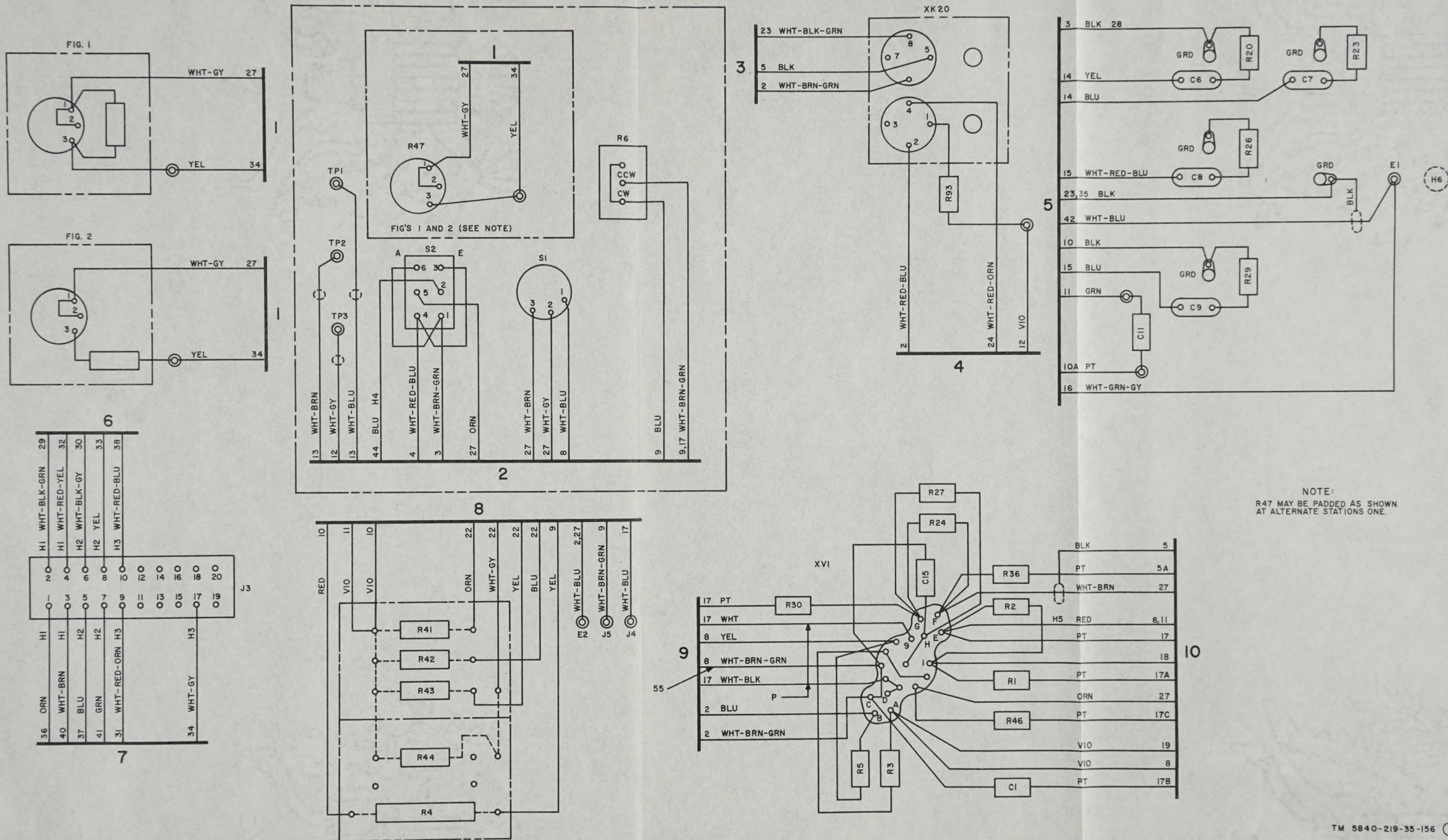


Figure 174. Coordinate data decoder KY-277/TSQ-36, wiring diagram.

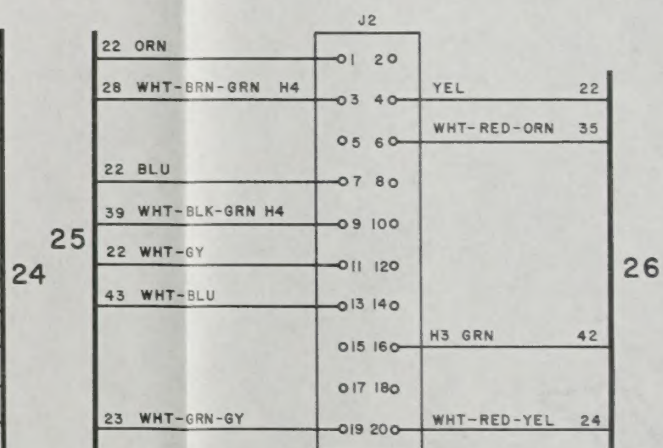
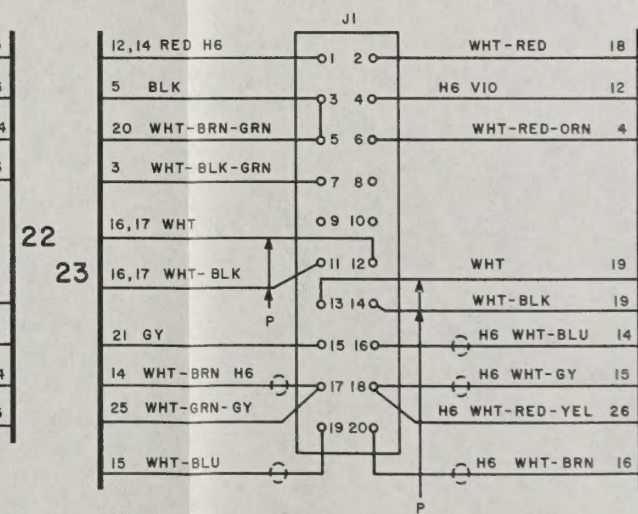
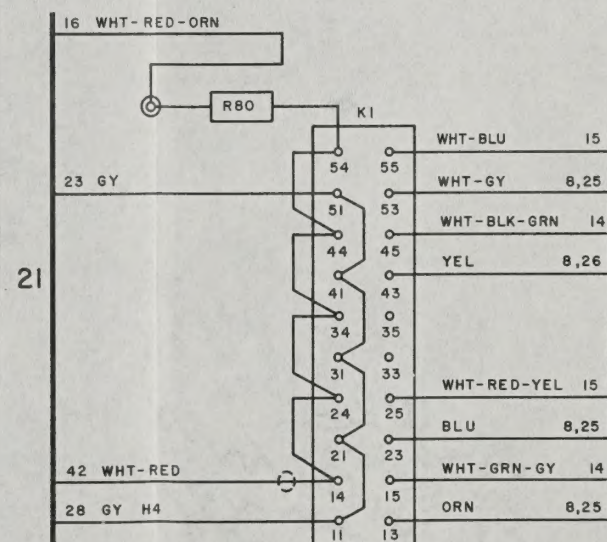
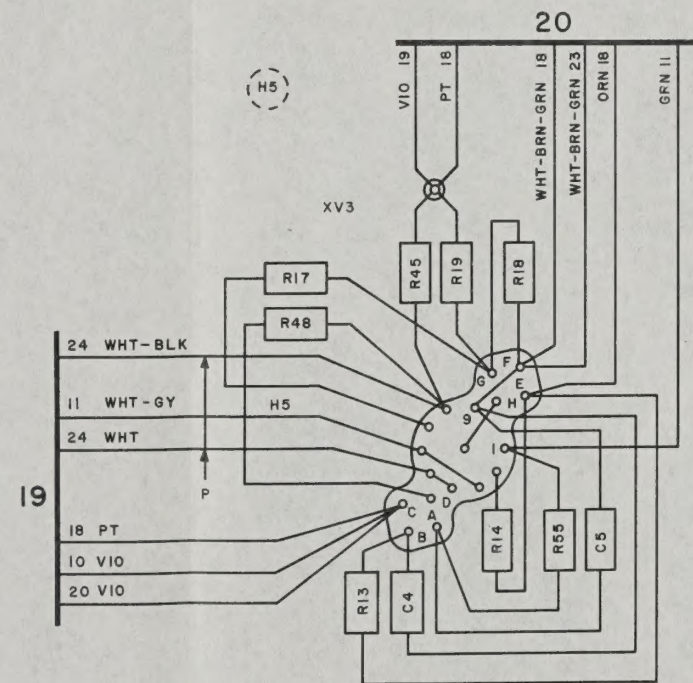
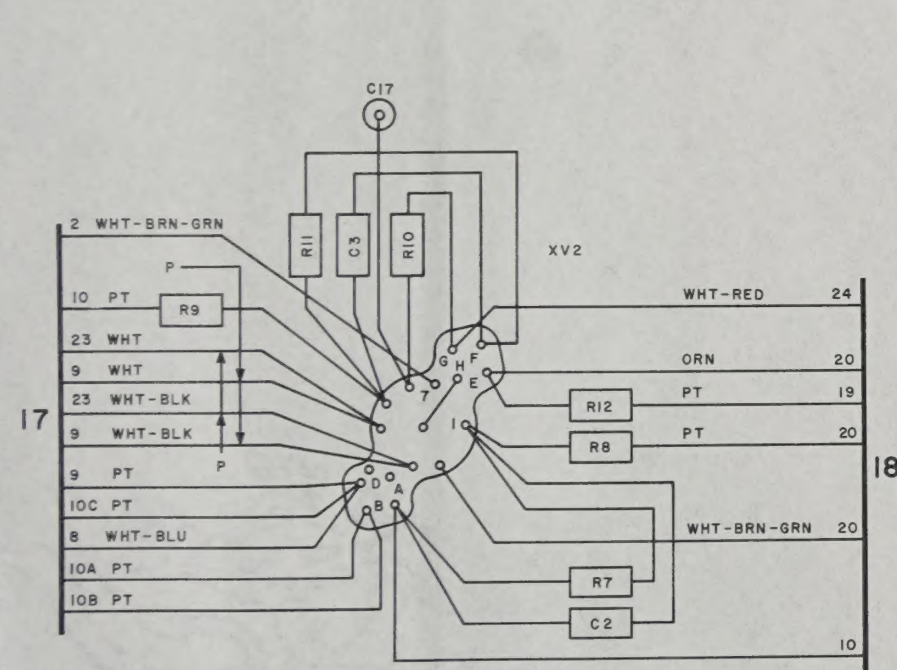
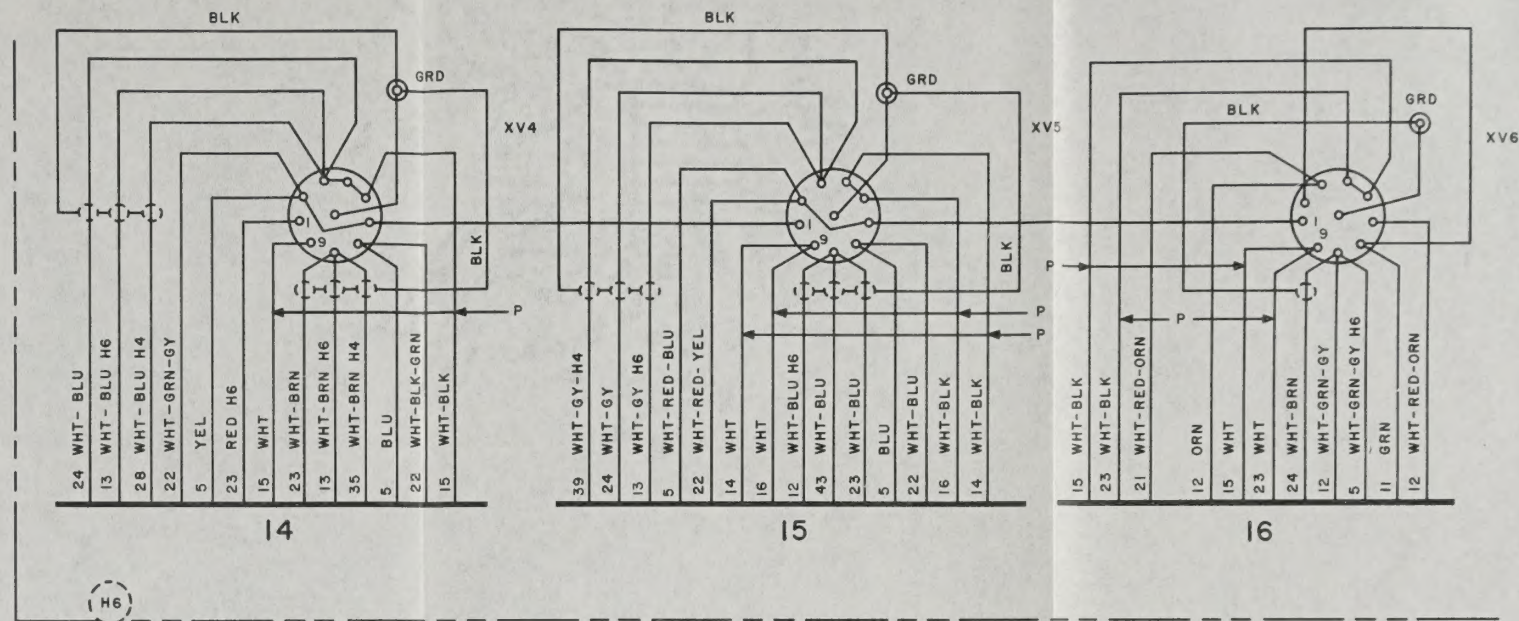


Figure 174—Continued.

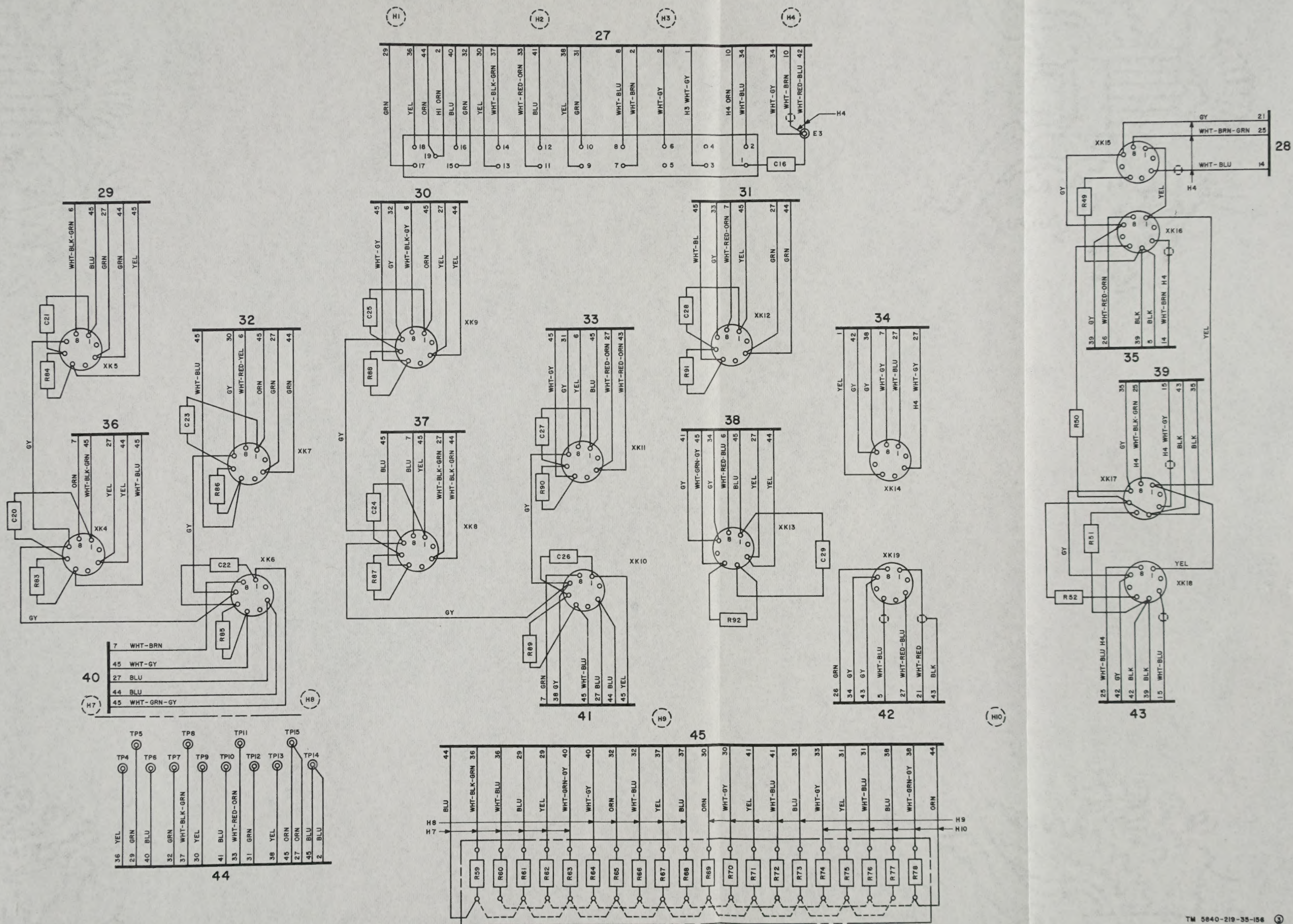


Figure 174-Continued.

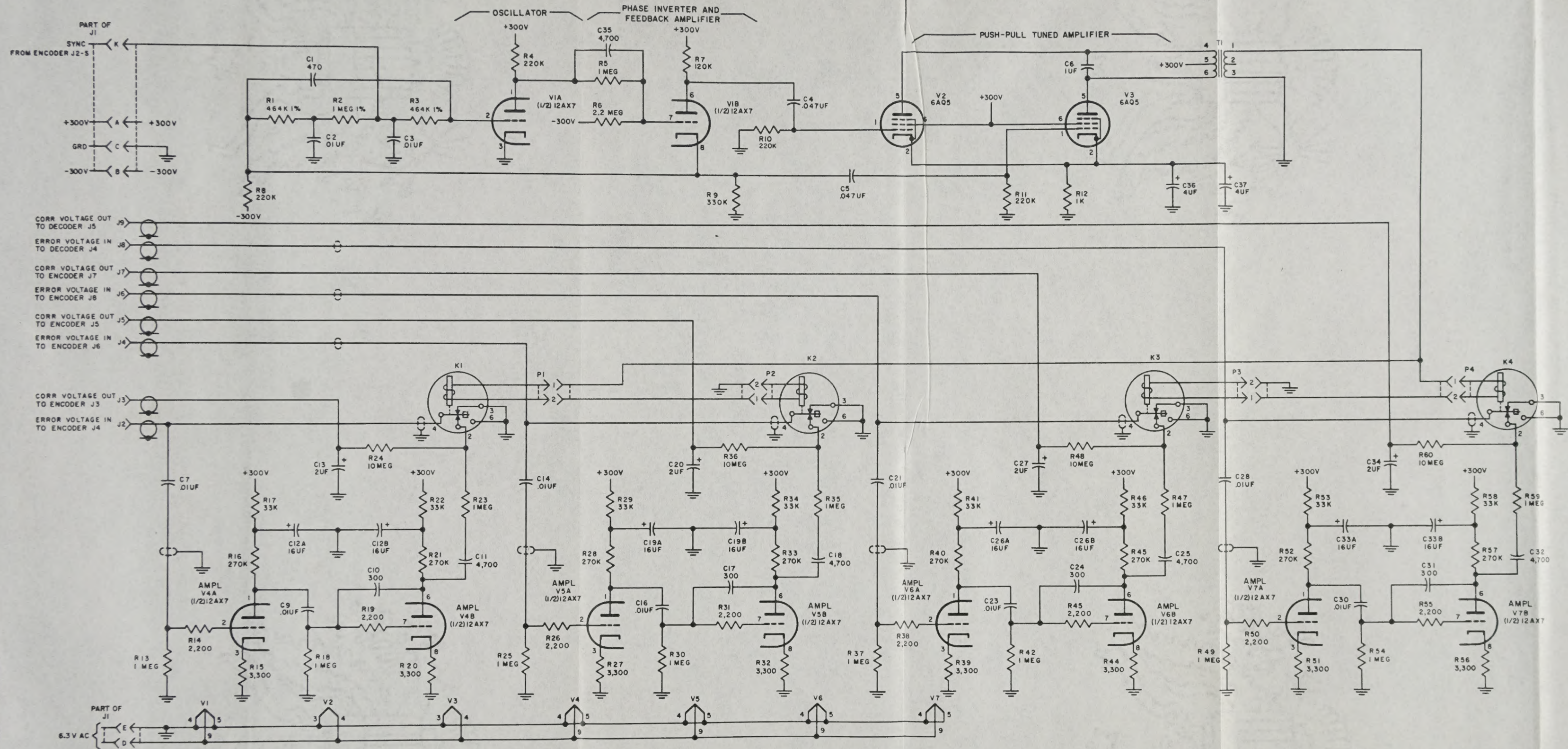


Figure 176. Direct current amplifier AM-2125/TSQ-36, schematic.

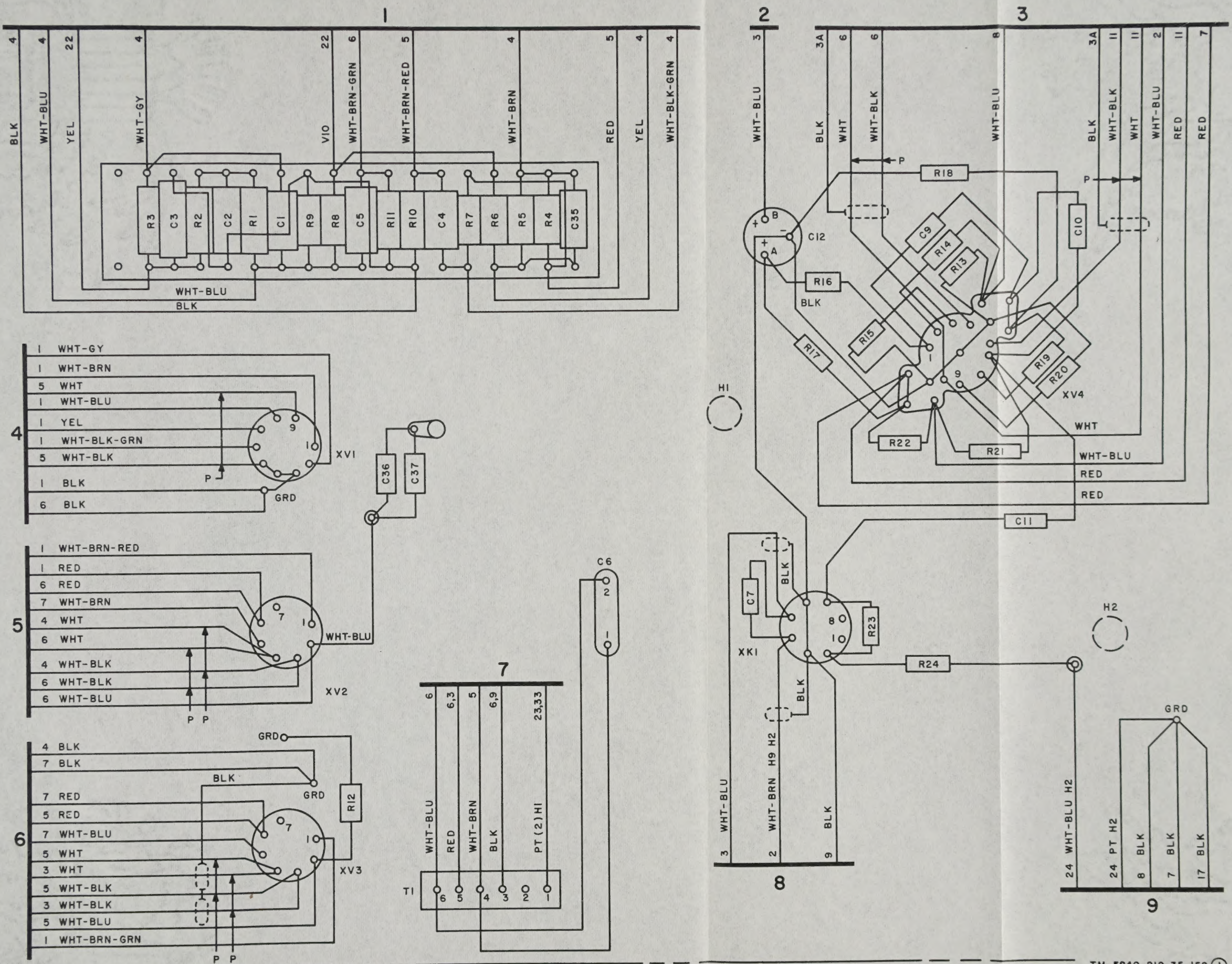


Figure 177. Direct current amplifier AM-2125/TSQ-36, wiring diagram.

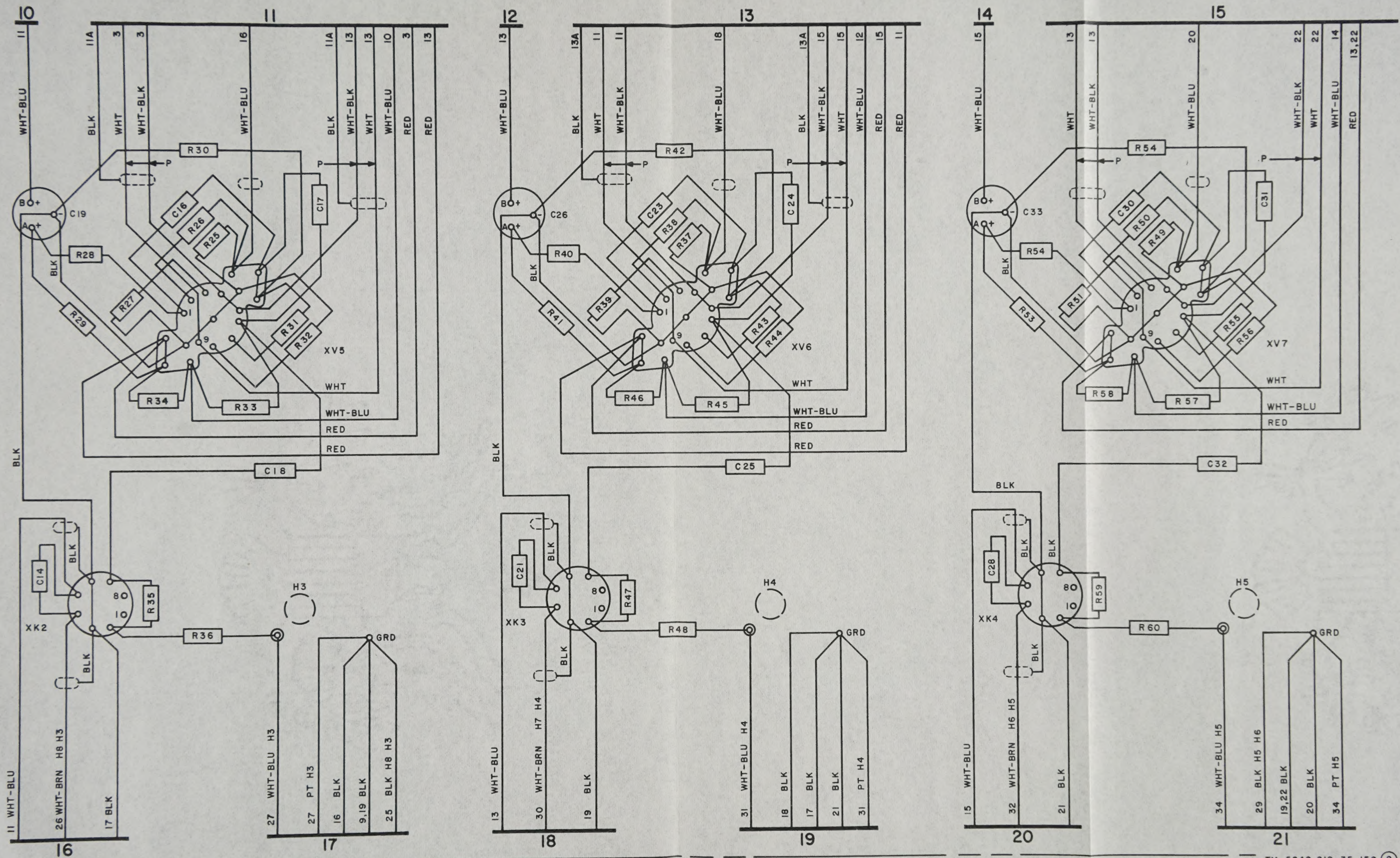


Figure 177—Continued.

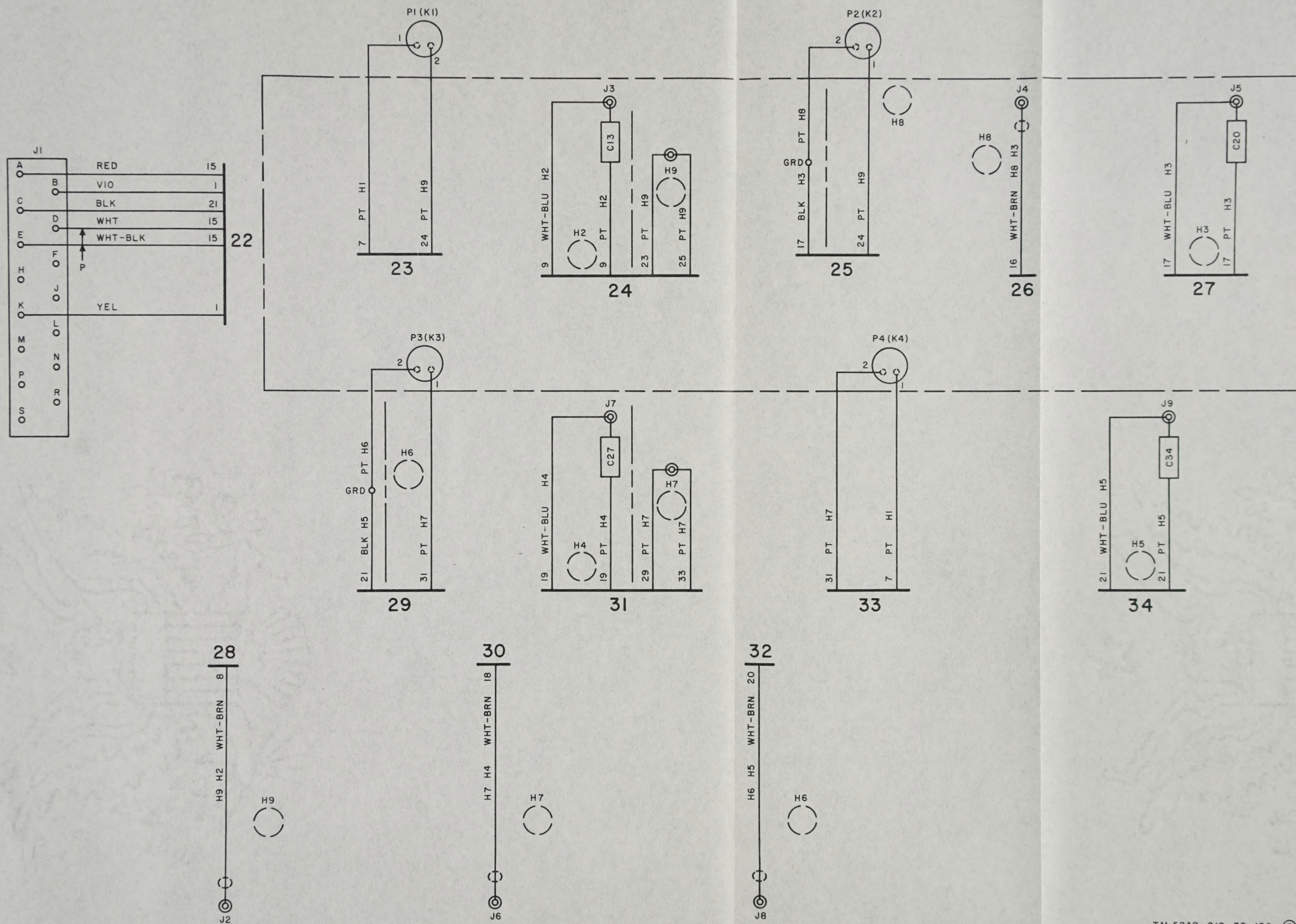
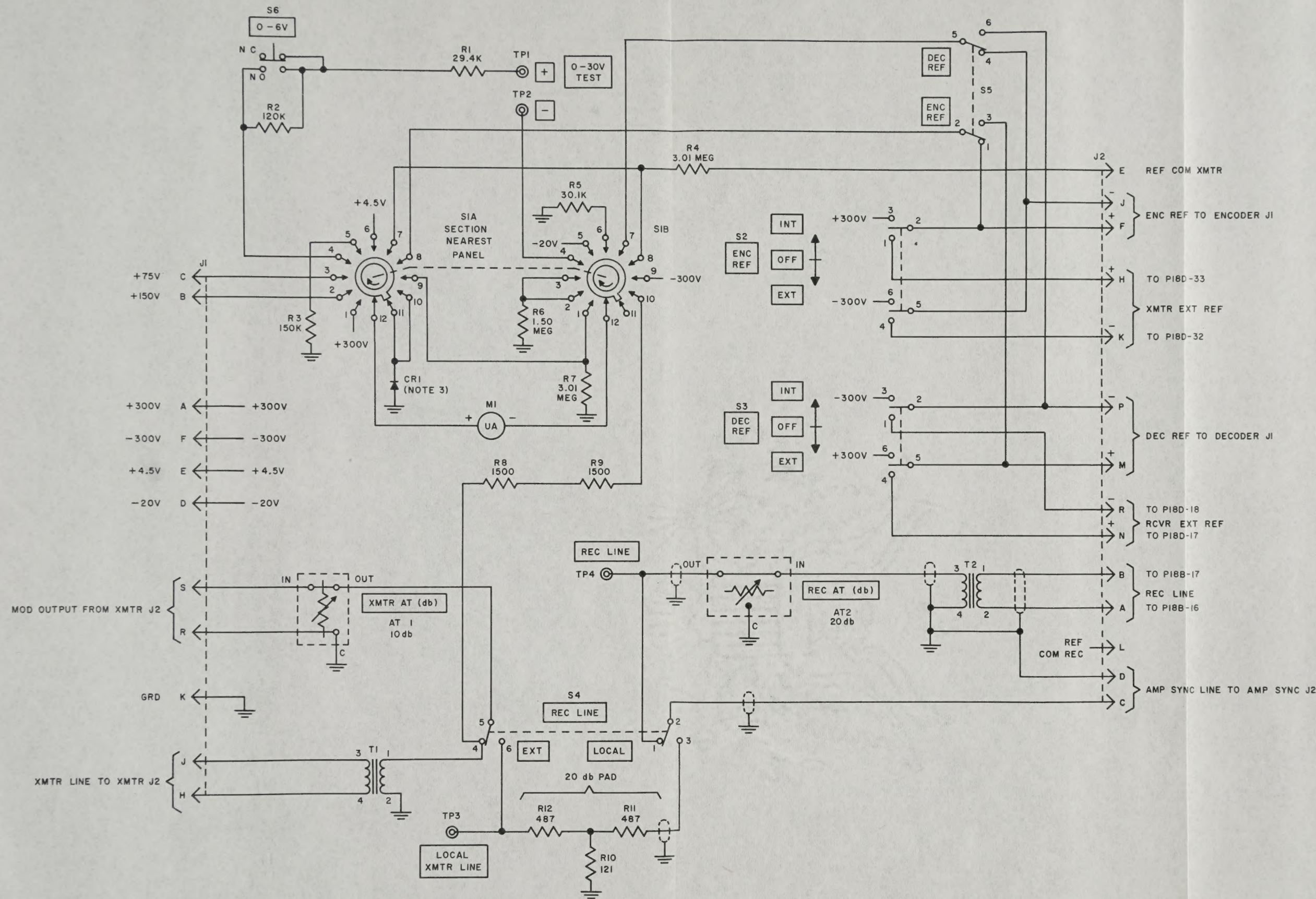
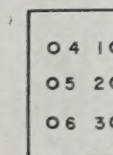


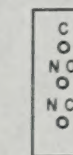
Figure 177—Continued.



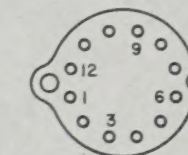
- NOTES:
1. UNLESS OTHERWISE INDICATED RESISTANCES ARE IN OHMS.
 2. TERMINAL NUMBERS FOR ALL SWITCHES ARE FOR REFERENCE ONLY. RELATIVE LOCATION OF TERMINALS IS SHOWN BELOW.
 3. DIODE PER SM-B-181092.
 4. INDICATES EQUIPMENT MARKING.



REAR
VIEW
S2-S5



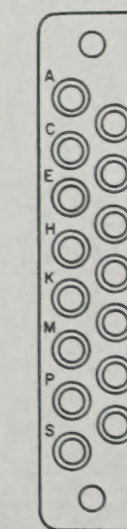
REAR
VIEW
S6



REAR VIEW
SIA AND SIB

S1		
POS	CONTACT	FUNCTION
1	1-12	+300V
2	2-12	+150V
3	3-12	+75V
4	4-12	0-30V TEST
5	5-12	-20V
6	6-12	+4.5V
7	7-12	-REF
8	8-12	+REF
9	9-12	-300V
10	10-12	XMTR SIG LVL
11	11-12	

HIGHEST REFERENCE DESIGNATION	
R12	CR1



J1 AND J2
WIRING SIDE

Figure 179. Electrical test panel SB-976/TSQ-36, schematic.

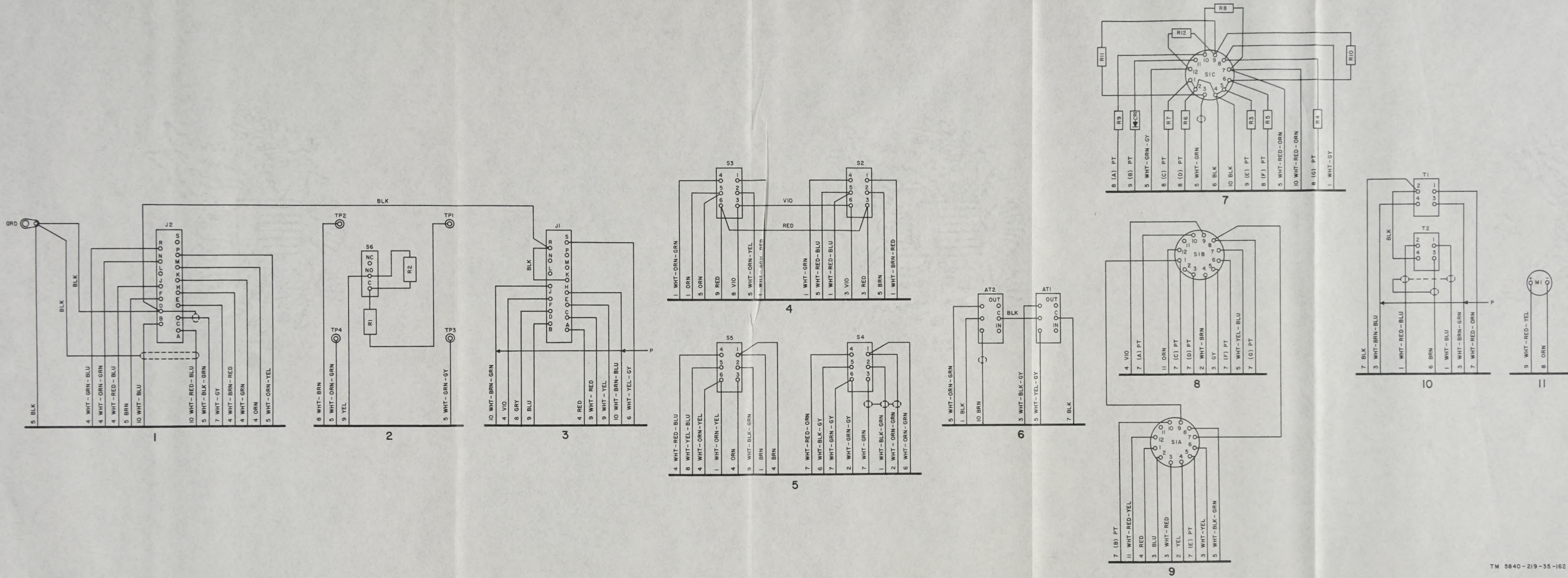
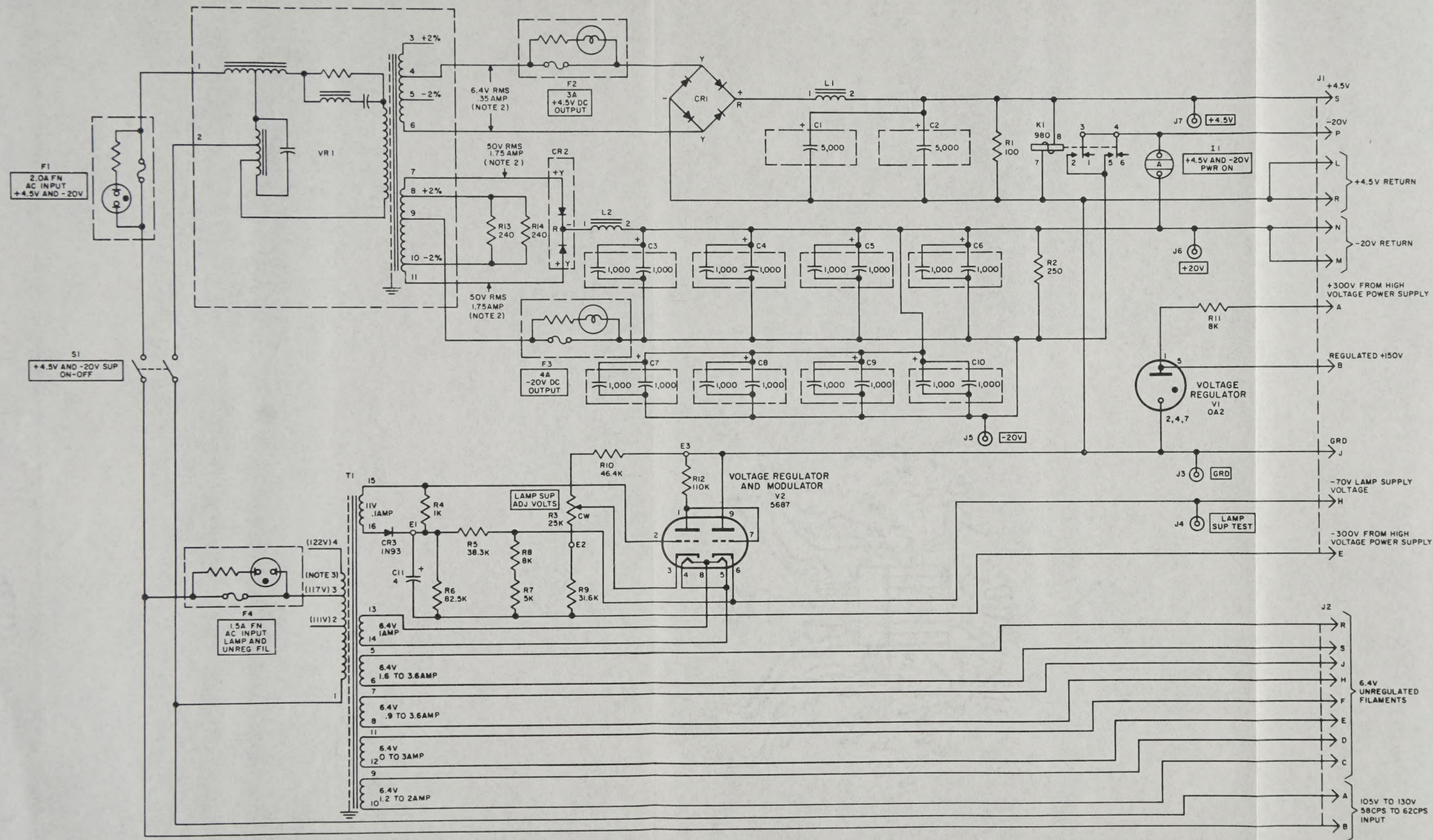
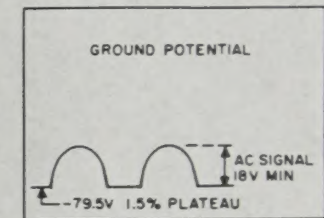


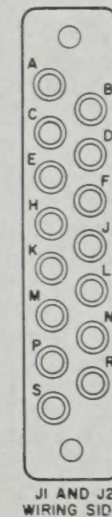
Figure 180. Electrical test panel SB-976/TSQ-36, wiring diagram.



- NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF.
 2. TAPS 3 AND 5 ON (VR1) PROVIDE $\pm 2\%$ ADJUSTMENTS FOR THE +4.5V OUTPUT. TAPS 8 AND 10 PROVIDE A $\pm 2\%$ ADJUSTMENT FOR THE -20V OUTPUT. THESE TAPS ARE SELECTED DURING MANUFACTURE TO MAKE THE -20V TO +4.5V RATIO AS CLOSE TO 4.44 AS POSSIBLE, WHILE MAINTAINING A NOMINAL +4.5V OUTPUT.
 3. SELECT TAPS ON TRANSFORMER (T1) NEAREST TO THE NOMINAL LINE VOLTAGE. UNITS WILL BE FURNISHED WIRED TO TAP 3 (117V).
 4. ON OUTPUT CONNECTOR (J1) PINS C, D, F, AND K ARE SPARES. ON OUTPUT CONNECTOR (J2) PINS K, L, M, N, AND P ARE SPARES.
 5. INDICATES EQUIPMENT MARKING.
 6. ALL RESISTORS ARE $\pm 2\%$ TOLERANCE.



LAMP SUPPLY VOLTAGE CHARACTERISTIC AS VIEWED ON A CALIBRATED OSCILLOSCOPE.



HIGHEST REFERENCE DESIGNATIONS		
C11	CR3	R14

Figure 181. Power supply PP-2235/G, schematic.

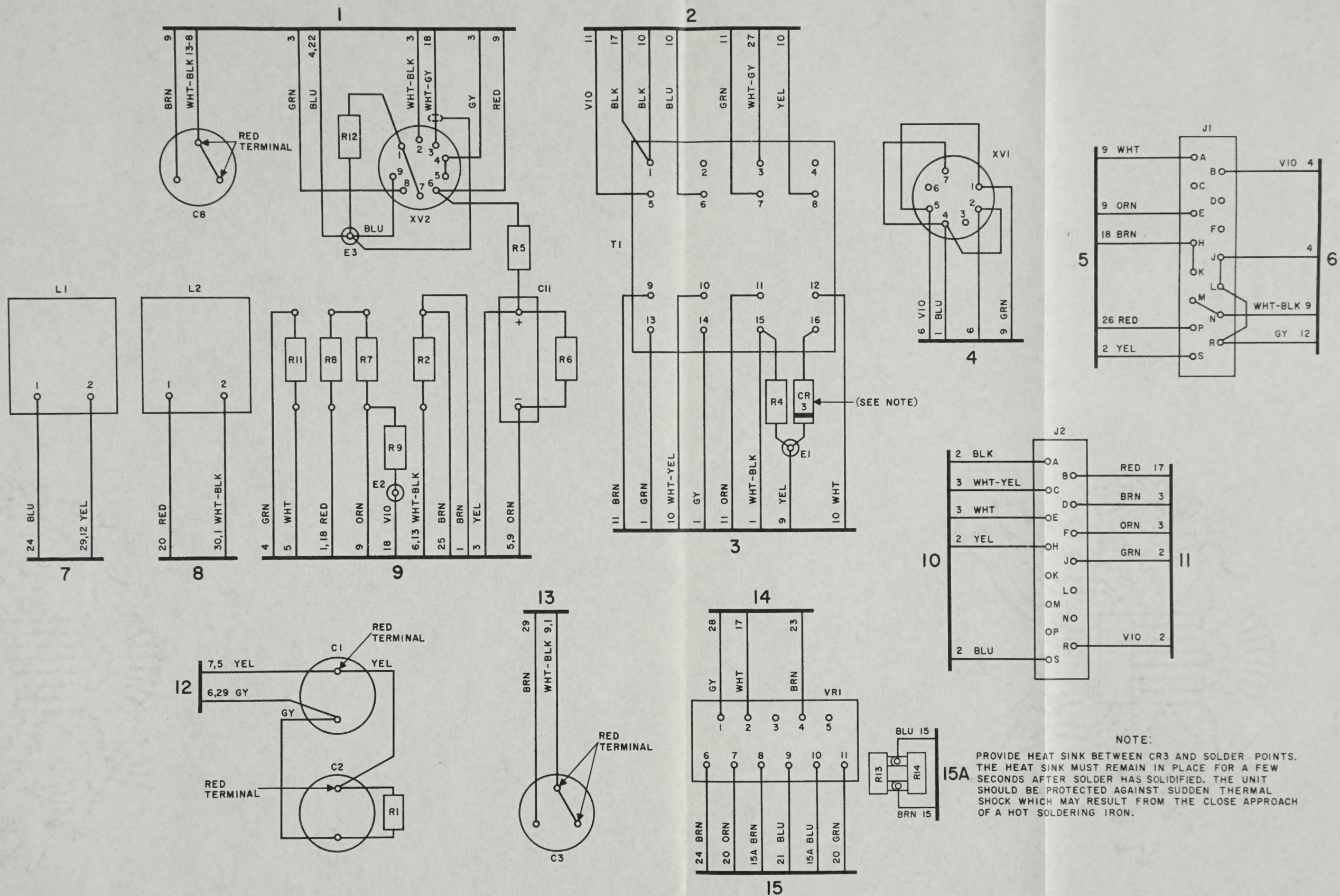


Figure 182. Power supply PP-2235/G, wiring diagram.

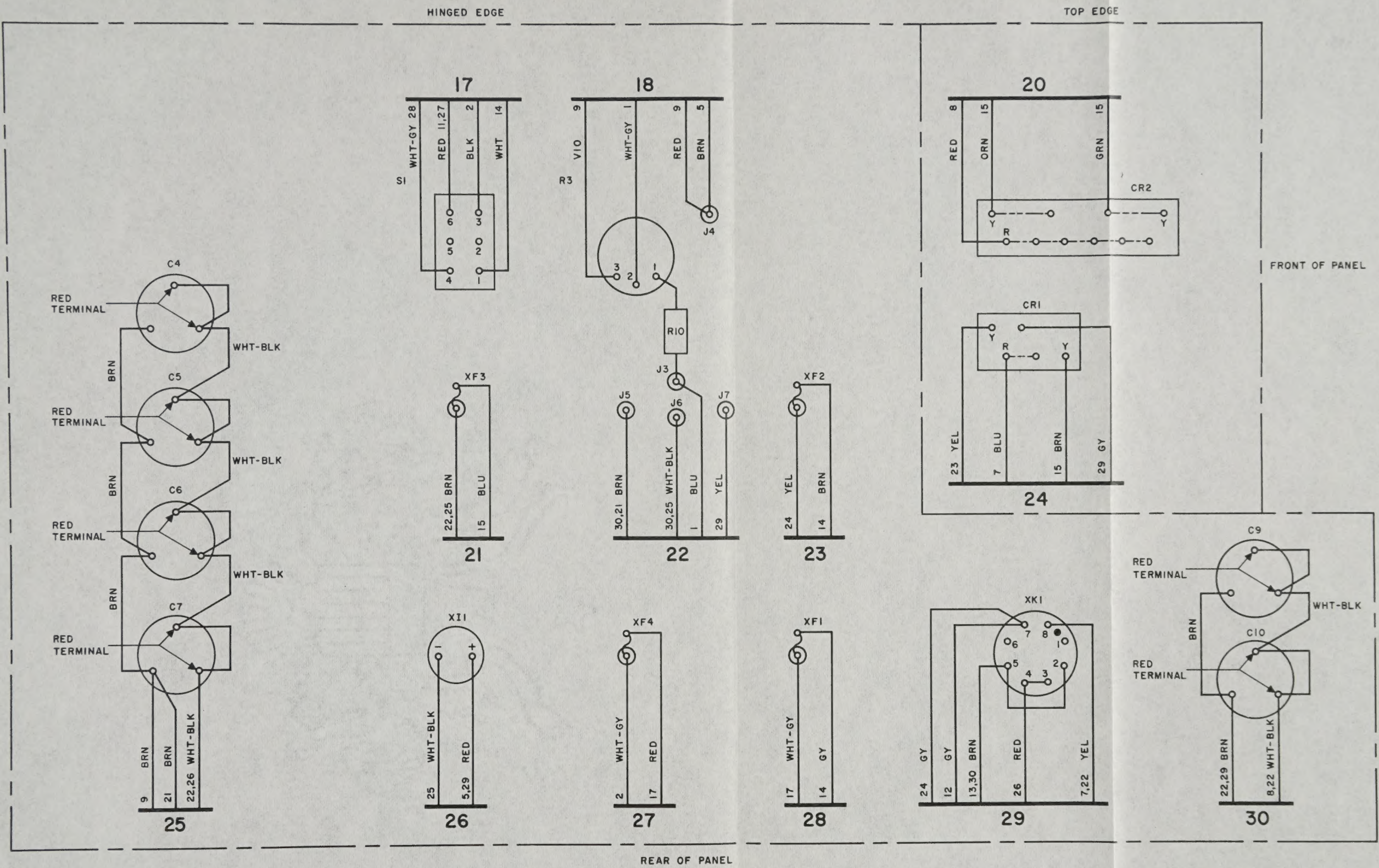


Figure 182—Continued.

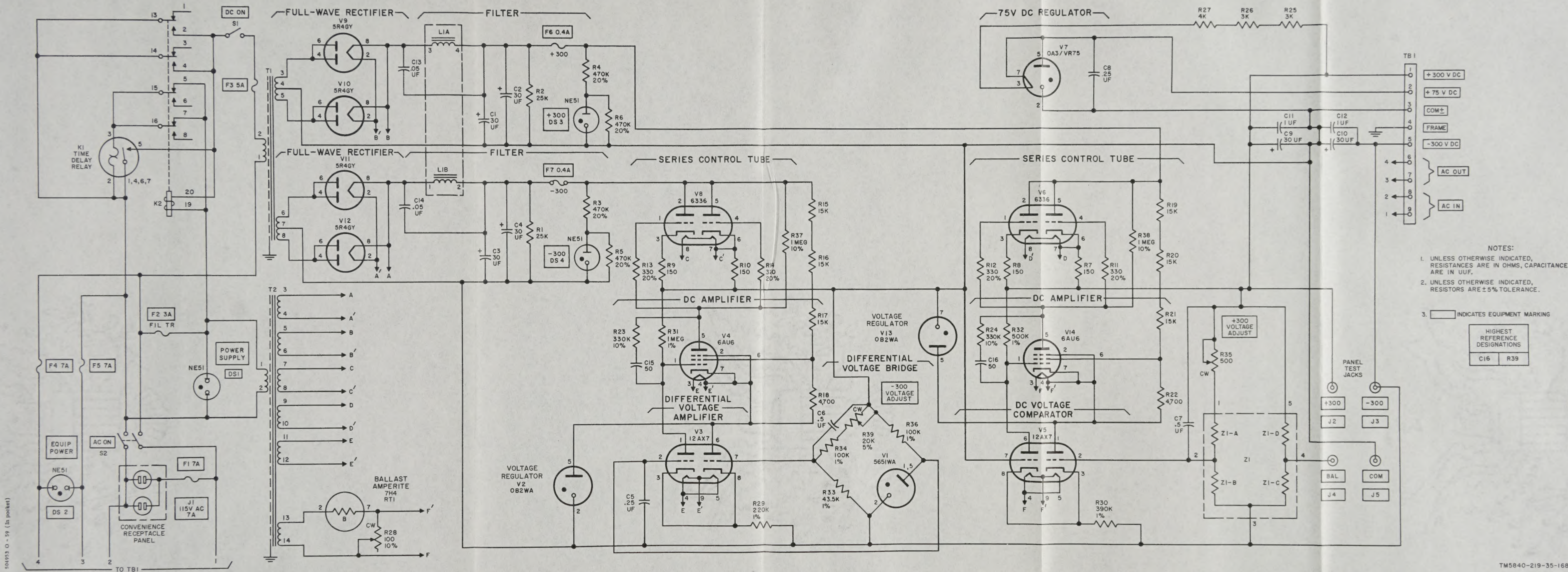
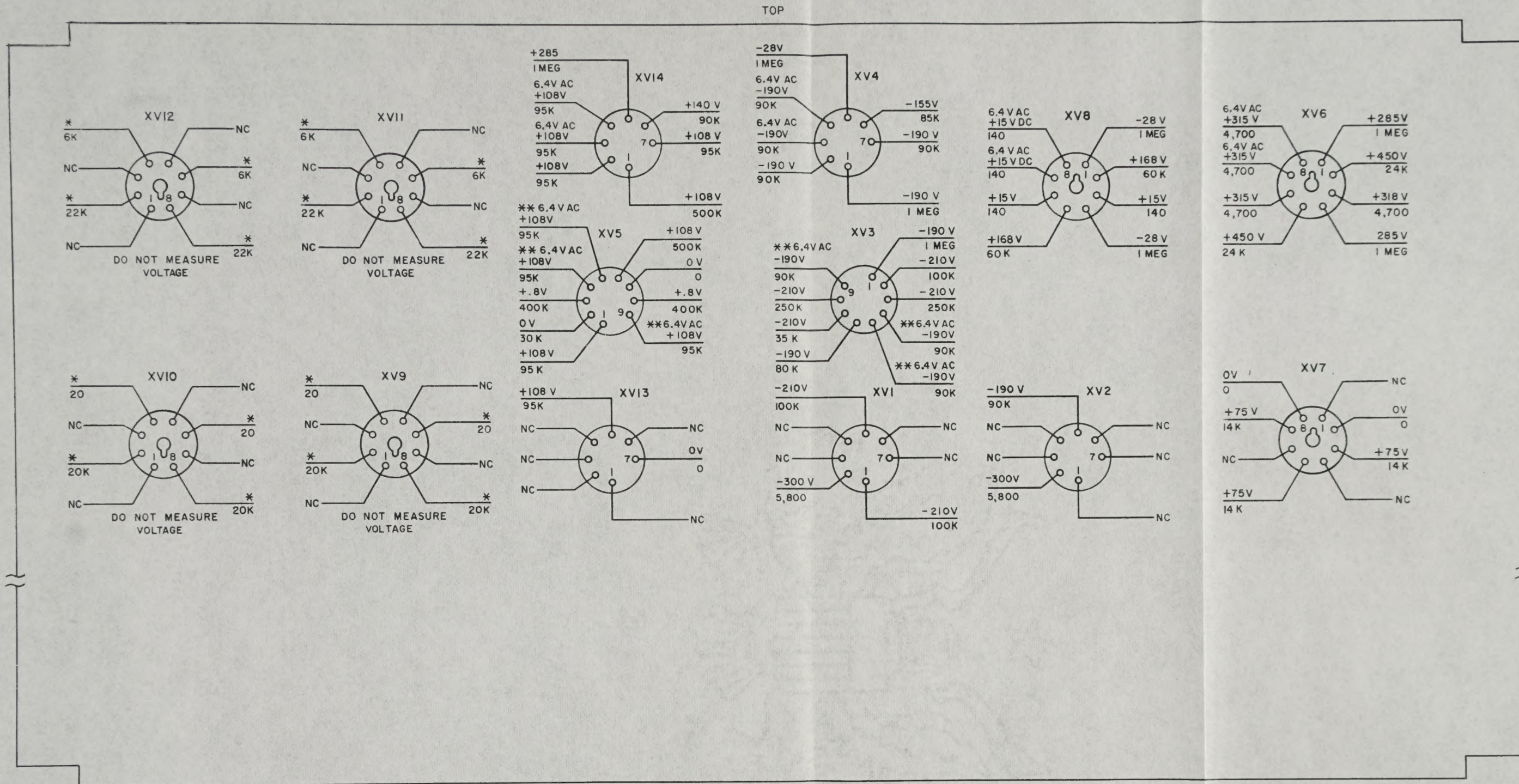


Figure 184. Power supply PP-2236/G, schematic.

TM 5840-219-35-169

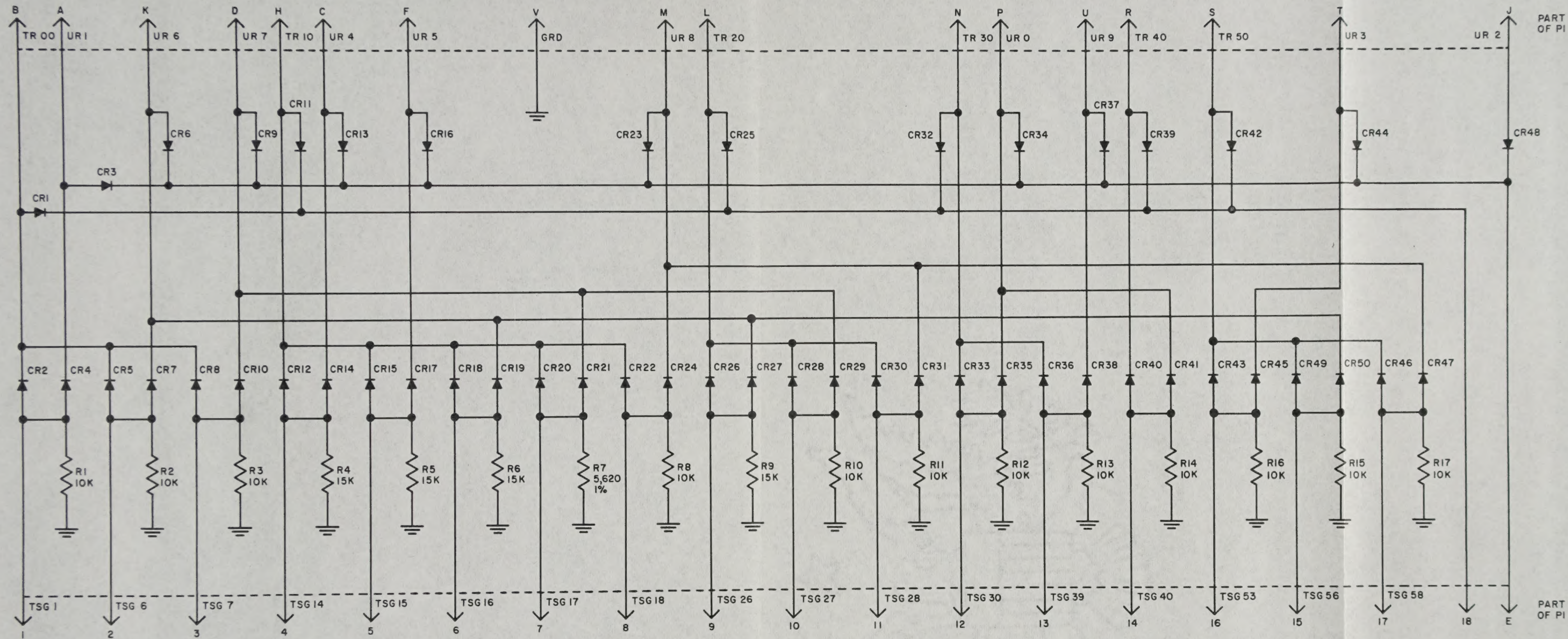


BOTTOM

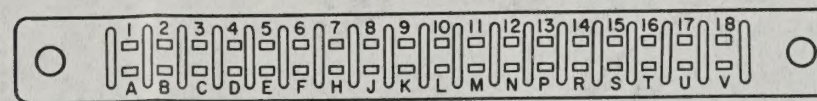
NOTES:

1. DC VOLTAGE MEASUREMENTS MADE WITH 20,000 OHMS PER VOLT METER.
2. RESISTANCES ARE IN OHMS AND ARE MEASURED TO CHASSIS GROUND UNLESS OTHERWISE SPECIFIED.
3. * DO NOT MEASURE VOLTAGE.

Figure 186. Power supply PP-2236/G, voltage and resistance diagram.



T/R PACKAGE

PI
WIRING SIDE

NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
2. ALL DIODES ARE SM-B-181088.
3. UNLESS OTHERWISE INDICATED, RESISTORS ARE $\pm 5\%$ TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.

ABBREVIATIONS:

TR- TENS RING STAGE
TSG-TIME SLOT GATE
UR- UNITS RING STAGE

HIGHEST
REFERENCE
DESIGNATIONS

CR50 R17

Figure 187. Transmitter unit subassembly MX-2688/G, schematic.

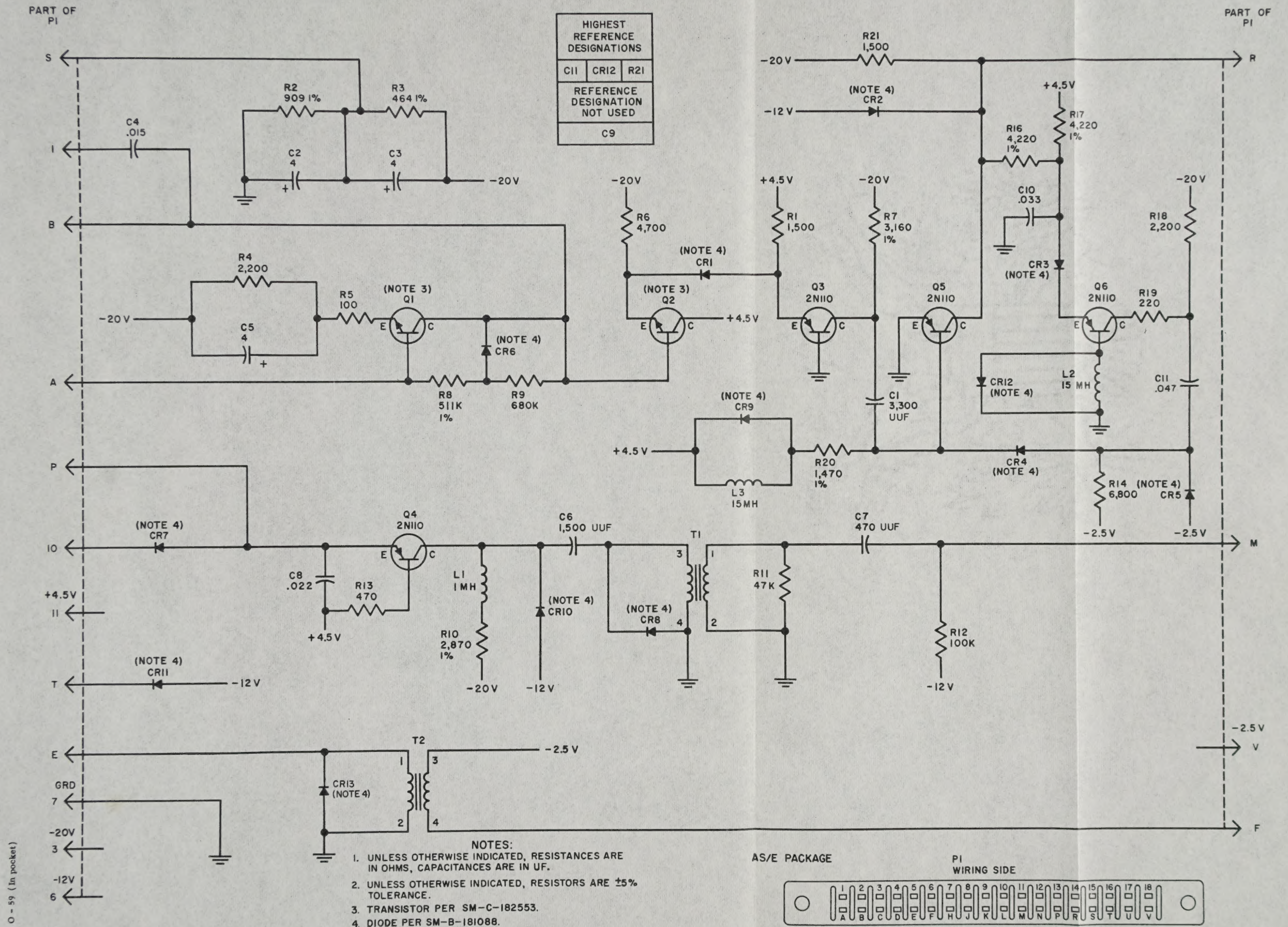
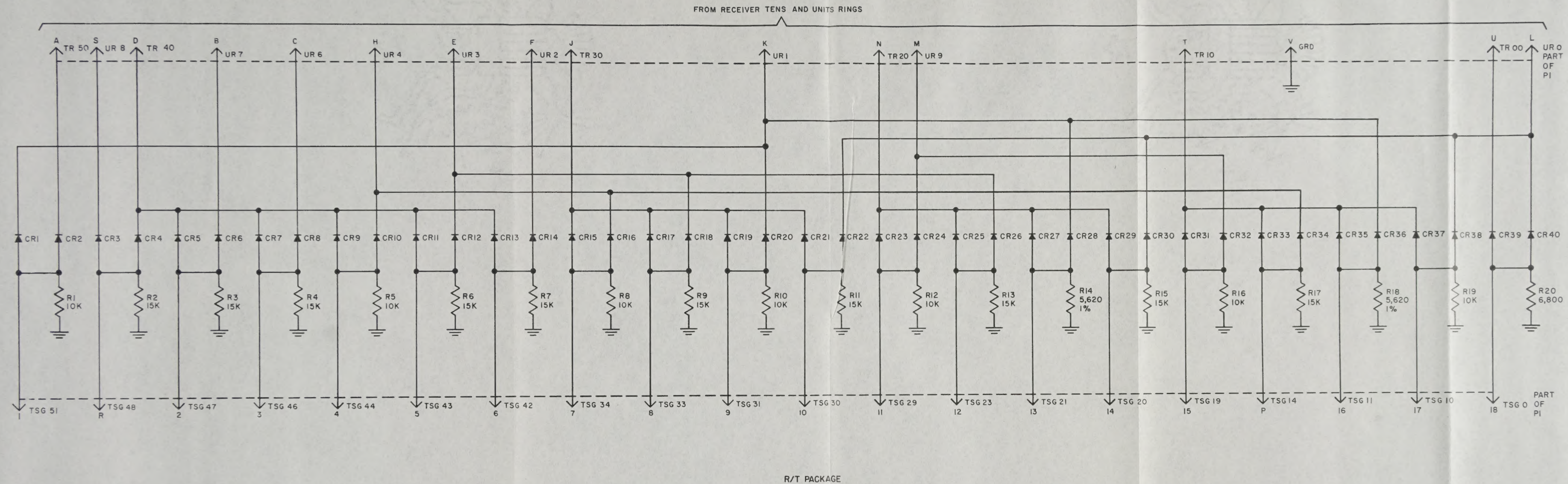
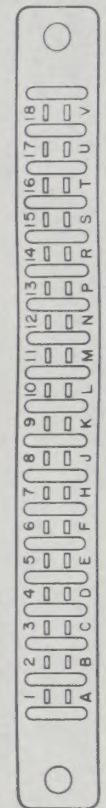


Figure 196. Amplifier-synchronizer unit subassembly MX-2349A/G, schematic.

504933 O - 59 (in pocket)



- NOTES:
1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
 2. UNLESS OTHERWISE INDICATED, RESISTORS ARE $\pm 5\%$ TOLERANCE. WHERE TOLERANCES ARE SHOWN, THEY ARE PLUS OR MINUS THE RESISTOR VALUE.
 3. ALL DIODES ARE SM-8-181088.



P1

ABBREVIATIONS:
TR - TENS RING STAGE
TSG - TIME SLOT GATE
UR - UNITS RING STAGE

HIGHEST REFERENCE DESIGNATIONS	
CR40	R20

Figure 197. Receiver unit subassembly MX-2685/G, schematic.

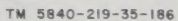
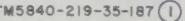
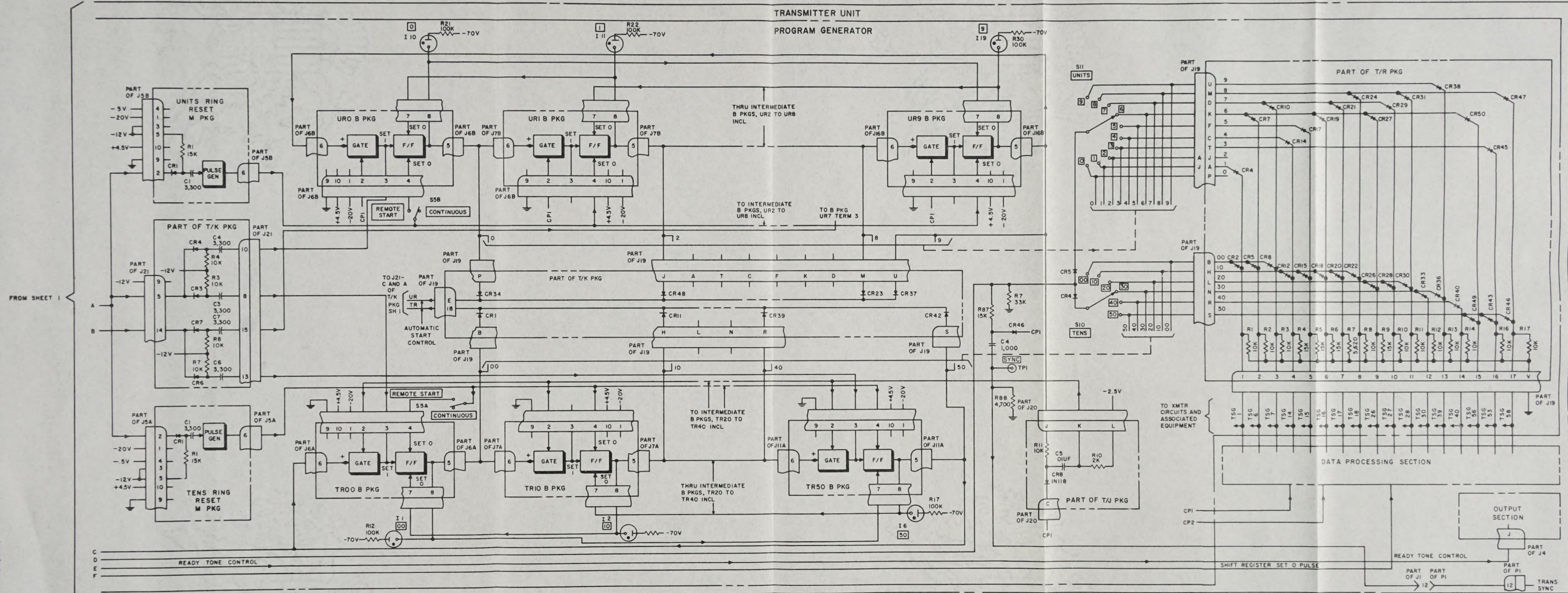
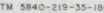


Figure 202. Coordinate multiplexing and encoding, functional schematic.



504953 O - 59 (In pocket)





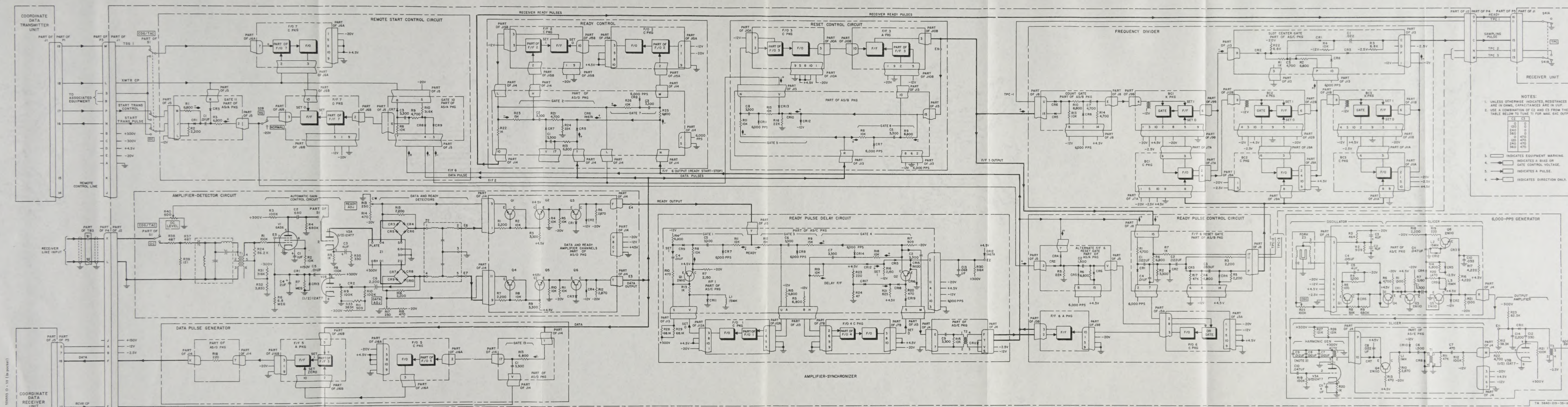


Figure 205. Receiver input and synchronizing, functional schematic.

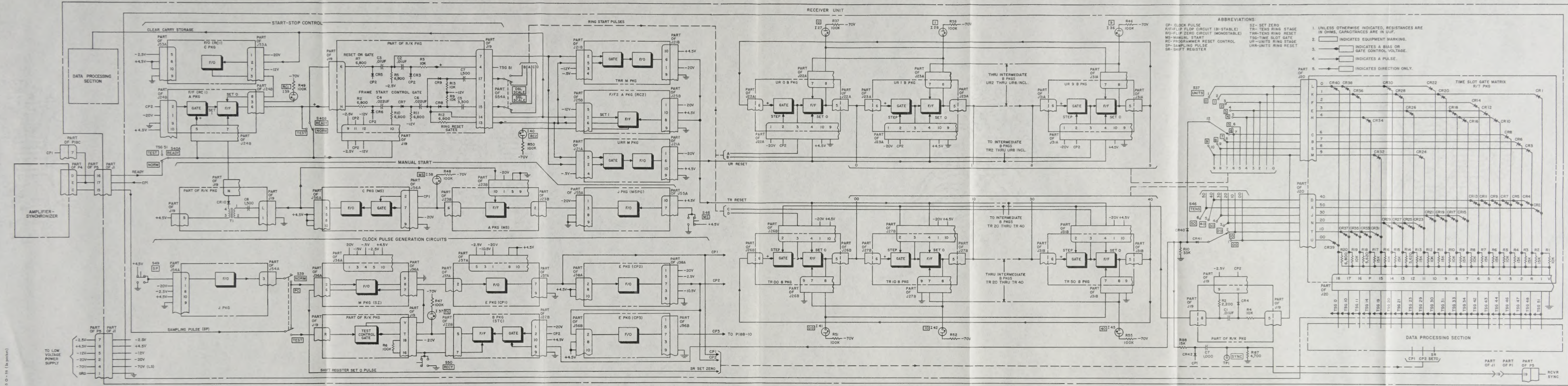


Figure 206. Receiver program generator, functional schematic.

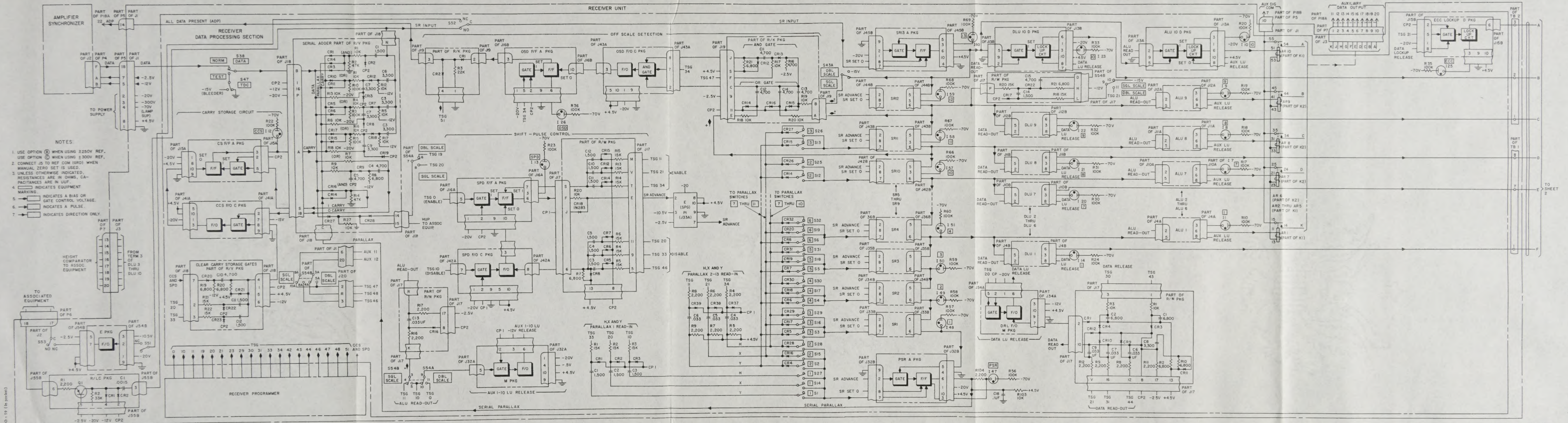


Figure 207. Receiver data processing, functional schematic.

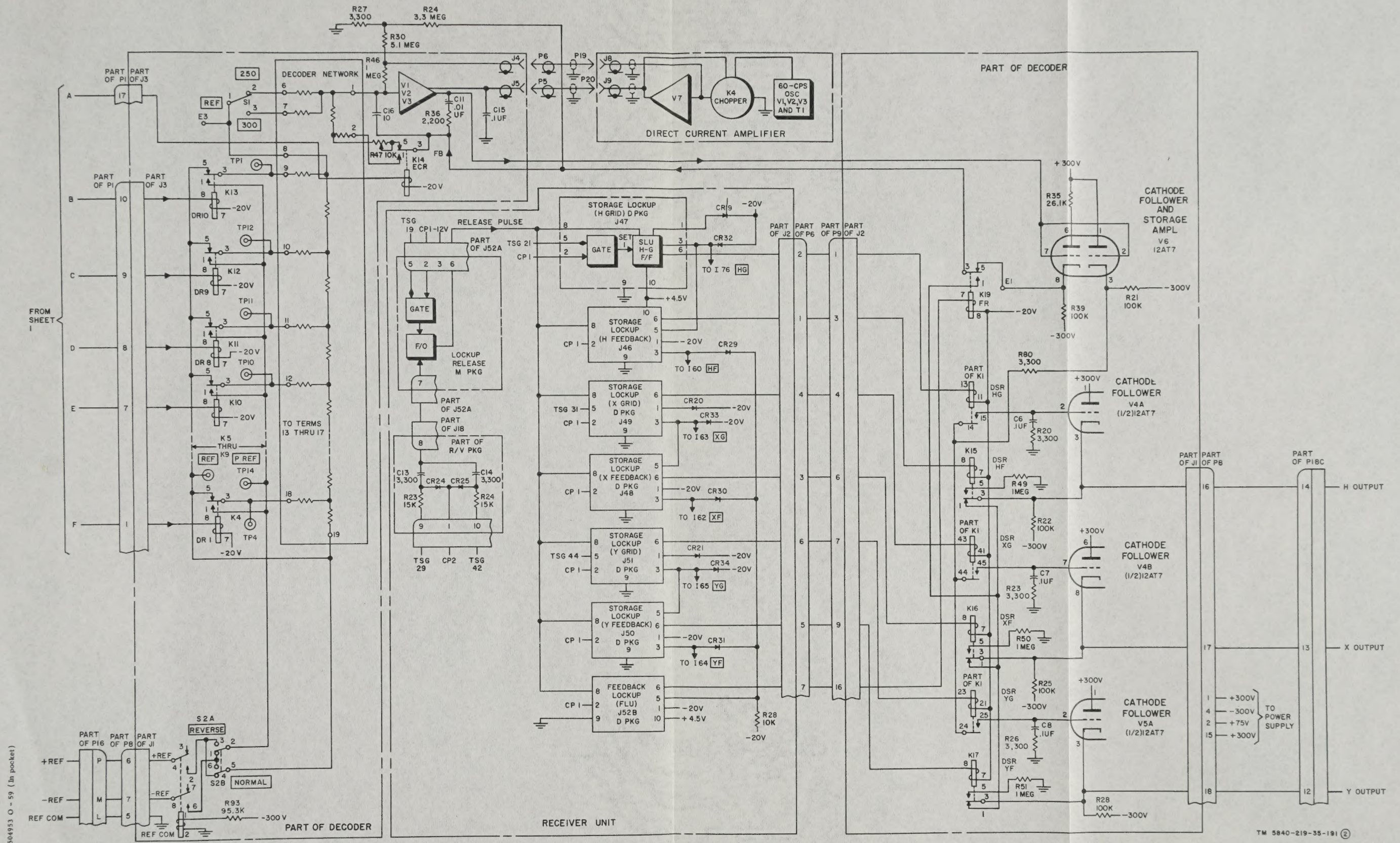


Figure 207—Continued.

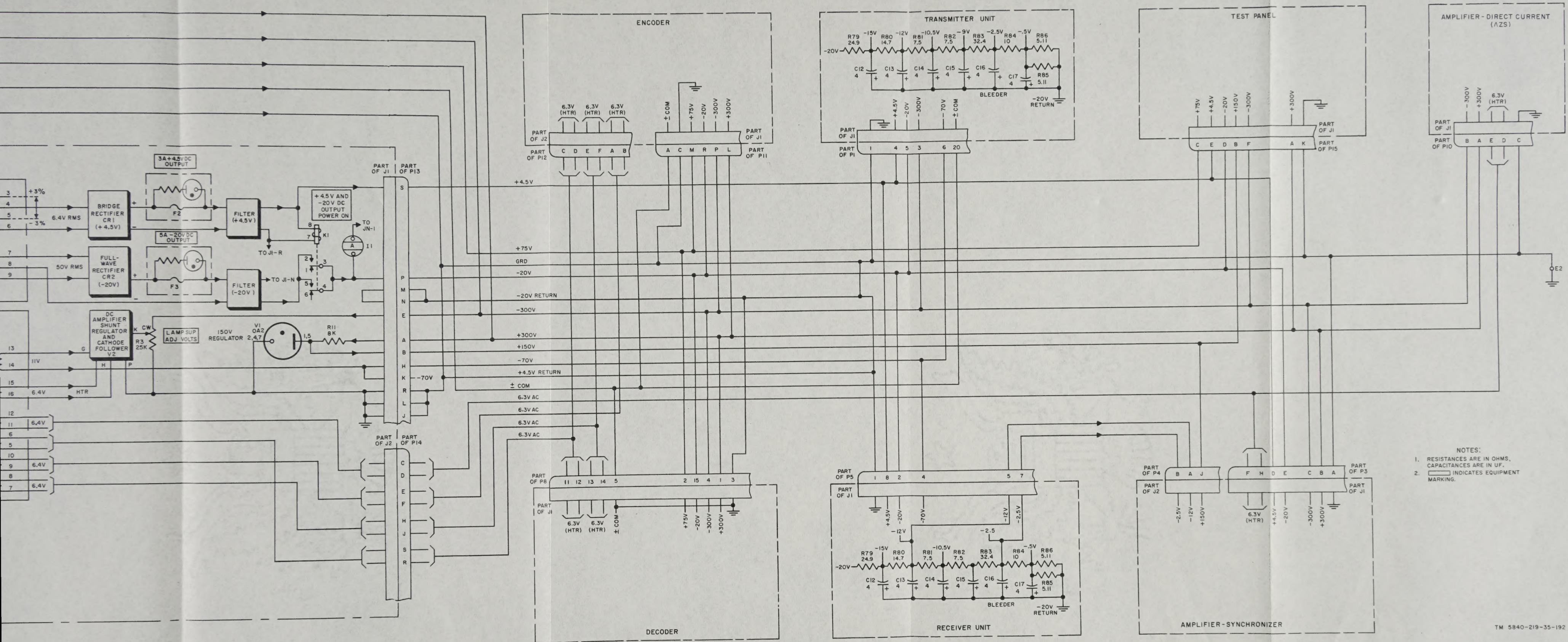


Figure 208. Power supply distribution, functional schematic.

